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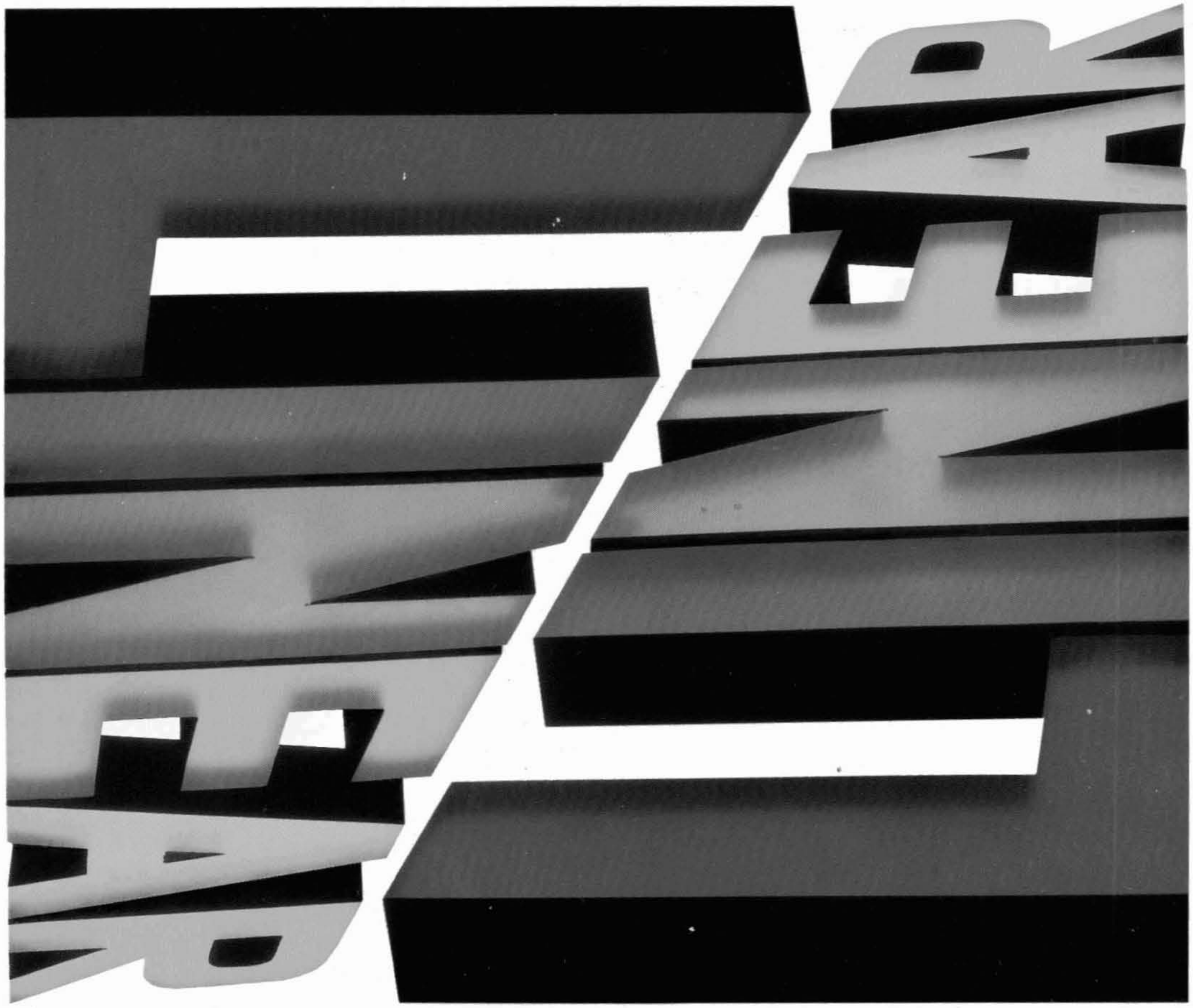
LINEAR TECHNOLOGY

1993
Linear Applications Handbook
Volume II
A Guide to Linear Circuit Design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INTRODUCTION

Quality, Efficiency and Style

The title above describes characteristics we seek in our application publications. This third* edition of the Linear Applications Handbook includes our latest attempts at instilling these traits into LTC literature. The 1990 edition's introduction described the justification and approach for LTC's application effort in significant detail. It is recommended as a guide to using all LTC application notes, regardless of publication date. As such, it is included in this edition. The trio of descriptives forming this section's title heavily abbreviates what has been said, while adding additional perspective.

Quality, in particular good quality, is obviously desirable in any publication. A high quality application note requires attentive circuit design, thorough laboratory technique, and completeness in its description. Text and figures should be thoughtfully organized and presented, visually pleasing, and easy to read. The artwork and printing should maintain this care in the form of clean text appearance and easily readable graphics.

Application notes should also be efficient. An efficiently written note permits the reader to access desired information quickly, and in readily understandable form. There should be enough depth to satisfy intellectual rigor, but the reader should not need an academic bathyscaphe to get to the bottom of things. Above all, the purpose is to communicate useful information clearly and quickly.

Finally, style should always show. Too much technical literature is dull reading. We enjoy our work, and we want to share our enthusiasm. Quite simply, we want our publications to be fun to read. An LTC author's ultimate fantasy features the reader at home in the living room; relaxed, smiling, and reading (while writing down LTC part numbers to buy). Style provides psychological lubrication, helping the mind to run smoothly. Clearly, style must only assist the serious purposes of publication and should not be abused; we do our best to maintain the appropriate balance.

As noted in previous editions a number of people besides authors make this work possible. As always, the final acknowledgement must go to our customers, who define our work, products, and company. We hope they are pleased with our latest efforts.

James M. Williams
April, 1993
Milpitas, California

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* Previous editions appeared in 1987 and 1990. This edition includes only material generated since the 1990 edition. As such, don't throw that 1990 book away!

1990 INTRODUCTION

Why Write Applications?

This is seemingly an odd and unlikely way to begin an applications publication, but it is a valid question. As such, the components of the decision to produce this book are worth reviewing.

Producing linear application material requires an intensive, extended effort. Development costs for worthwhile material are extraordinarily high, absorbing substantial amounts of engineering time and money. Further, these same resources could be directed towards product development, the contribution of which is much more easily measured at the corporate coffers. These are serious issues in any environment, but are particularly critical in a rapidly growing company, where resources must be thoughtfully allocated.

Linear Technology Corporation's commitment to a concerted applications effort was made despite these concerns. Specifically, the nature of linear circuit design is so diverse, the devices so sophisticated, and user requirements so demanding that designers require (or at least welcome) assistance. Ultimately, the procurement and use of linear ICs is tied to the user's ability to solve the problems confronting them. Anything which enhances this ability, in both specific and general cases, obviously benefits user and vendor.

This is a very simple but powerful argument, and is the basis of LTC's commitment to applications. Additional benefits include occasional new product concepts and a way to test products under "real world" conditions, but the basic justification is as described.

Traditionally, application work has involved reviewing considerations for successful use of a specific product. Additionally, basic circuit suggestions or concepts are sometimes offered. Although this approach is useful and necessary, some expansion is possible. LTC's applications are centered on detailed, systems-oriented circuits, (hopefully) similar to the types of designs users are working with. There is a broad tutorial content, reflected in the form of frequent text digressions and liberal use of graphics. Discussions of tradeoffs, options and techniques are emphasized, as opposed to brief descriptions of circuit operation. Many of the application notes contain appended sections which examine related or pertinent topics in detail. Ideally, this treatment provides enough background to allow readers to modify the circuits presented into solutions to their specific problems.

Some comment about the circuit examples is appropriate. They range from relatively simple to quite complex and sophisticated. Emphasis is on high performance, in keeping with the capabilities of LTC's products and the market we serve. The circuit's primary function is to serve as a catalyst—once the reader has started thinking, the material has accomplished its mission.

Substantial effort has been expended in working out and documenting these circuits, but they are not finessed to the highest possible degree. All of the circuits have been breadboarded and bench-tested at the prototype level. Specifications and performance levels quoted in the text represent measured and extrapolated data derived from the breadboard prototype. The volume of material generated prohibits formal worst-case review or tolerances analysis for production. Additionally, despite our best efforts, errors of various sorts do occasionally creep in along the way to publication. Because of these considerations, readers should contact LTC when preparing to use a circuit in a production situation. This allows us to advise on specific areas of the circuit which may require a "second look" before going to production. Updates, suggested modifications and just plain mistakes can also be discussed at this time.

We have received numerous comments and questions since this book's first (1987) edition. The most frequent query concerns topic selection. The topics presented are survivors of a selection process involving a number of disparate considerations. These include reader needs, suitability for magazine publication, LTC's short and long term commercial aspirations, time constraints and author interest in doing the work. Additionally, we seek a 10 year useful lifetime for application notes. This generally precludes narrowly focused effort towards individual ICs. Topics are broad, with a tutorial and design emphasis that (ideally) reflects the reader's long term interests. While the circuits presented unabashedly favor our products, they must be conceptually applicable to succeeding generations of devices (hopefully ours). Similarly, the circuits should represent a relatively complete and interdisciplinary approach to solving the problem at hand. Solving a problem is usually the reader's/customer's overwhelming motivation. The selection and integration of tools and methods towards this end is *the* priority. For this reason the examples and accompanying text are as complete and practical as possible. This may necessitate effort in areas where we have no direct economic stake, e.g., the software presented in AN28 or the magnetics developed for AN25, AN29, and AN35. In some circumstances this policy necessitates use of competitor's products (horrors!) where appropriate. Such gallant objectivity is not without calculation; the goal is to have readers associate LTC with realistic advice, useful products and satisfactory results, regardless of the problem encountered. The long term task is establishing and maintaining credibility and customer loyalty. If unabused, these are powerful sales tools. Maintaining this stance involves a significant amount of negotiation and compromise with issues and individuals, but the results are usually favorable for everyone.

A second common question addresses the time required to produce an individual application note. The work invested varies considerably. AN29 required a year to complete. It involved endless laboratory hours, close coordination with our magnetics supplier and over 300 changes, corrections, band-aids and tweaks before the manuscript was finally released. Conversely, AN31 and AN32 were finished (perhaps therapeutically) within three weeks. In all cases the actual writing time is a miniscule percentage of the total work time. AN29's year of effort was written up in a week. AN31 and AN32 required less than five hours.

Another common question involves our photographic documentation. We have received hundreds of inquiries requesting details on instrumentation, particularly for multi-trace oscilloscope photography. Almost all photographic work is done with four (Tektronix 547 with a four trace 1A4 plug-in) or eight (Tektronix 556 with two 1A4 plug-ins) trace oscilloscopes. Photographs with more than eight traces utilize multiple exposure or splicing techniques. Tektronix C-12 and C-27 cameras are used on both instruments, with modified graticule illumination on the 556. AN29's Appendix F provides additional discussion.

A final recurring question concerns use of this book as text in university level courses. We certainly welcome this, and find it rewarding. However, we cannot develop, or collaborate in the development of, supplementary material for problem sets and laboratory manuals. This simply strays too far from our charter.

Some significant additions since the 1987 edition are the "Design Notes" and the open format used in AN26, AN27 and AN36. "Design Notes" provide a way to cover a specific topic in concise form and get the material to the reader quickly. Most of these notes are stand-alone efforts. In some cases they are excerpted from application note work in progress and fed directly to print. When the application note becomes available, the material appears in unabbreviated form. Another change is the format used for AN26, AN27 and AN36. The segmented approach allows convenient updating and additions at some sacrifice in text flow. Subjects amenable to this treatment avoid the disruptive surgery required to revise a conventional manuscript.

In response to reader requests we have included macromodels of components. The present list includes 28 ICs, all amplifiers. This inventory will grow and diversity into other part types. Significant effort has gone towards making these models realistic and usable. They are intended as powerful adjunct tools in the design process, and should not be abused. More specifically, they are meant to augment actual breadboards, not eliminate them. Bypassing breadboarding is an extraordinarily hazardous process with a high fatality rate, even among veteran designers. Although these macromodels cannot eliminate the cold realities involved in making something work, they ease the task and save time. As such, we encourage readers to use them and invite your comments.

Also new is the inclusion of application notes from other sources. These notes, found in the "Reference Reading" section, have proven particularly useful to readers. The information they contain is pertinent to problem areas that concern our readers. As such, they merit inclusion. If this approach is well received this section will be enlarged in succeeding editions. The cooperation of the contributors is appreciated.

Finally, the appearance of new authors is applauded, particularly by the undersigned. There is plenty of work to do and many pens (and probes) ease the task while broadening perspective.

Acknowledgements

A number of people with a wide variety of talents contributed to this book. LTC's senior management, most notably R. Swanson, B. Dobkin, and B. Ehrsam, provided continuous support and encouragement. M.J. Yuhas showed special skill in converting the worst form of "chicken tracks" into legible, expertly prepared and edited manuscripts and is due special recognition.

B. Essaff prepared some beautiful breadboards (until I corrupted his construction technique) and was a major contributor to the lab work. C. Nelson, T. Redfern, G. Erdi, W. Rempfer, D. O'Neill, N. Sevastopoulos, and B. Huffman contributed useful comments, most of which were not diluted by tact.

In the final analysis, however, the ultimate acknowledgement must be reserved for our customers, who are both the beneficiaries and benefactors of this book. Their requests and requirements define our work, and hence this book. If we have listened carefully, they should be pleased.

James M. Williams
November, 1989
Milpitas, California

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1990 EDITION APPLICATION NOTE ABSTRACTS

AN1 **Understanding and Applying the LT1005 Multifunction Regulator**

This application note describes the unique operating characteristics of the LT1005 and describes a number of useful applications which take advantage of the regulator's ability to control the output with a logic control signal.

AN2 **Performance Enhancement Techniques for 3-Terminal Regulators**

This application note describes a number of enhancement circuit techniques used with existing 3-terminal regulators which extend current capability, limit power dissipation, provide high voltage output, operate from 110VAC or 220VAC without the need to switch transformer windings, and many other useful application ideas.

AN3 **Applications for a Switched-Capacitor Instrumentation Building Block**

This application note describes a wide range of useful applications for the LTC1043 dual precision instrumentation switched-capacitor building block. Some of the applications described are ultra high performance instrumentation amplifier, lock-in amplifier, wide range digitally controlled variable gain amplifier, relative humidity sensor signal conditioner, LVDT signal conditioner, charge pump F/V and V/F converters, 12-bit A/D converter and more.

AN4 **Application for a New Power Buffer**

The LT1010 150mA power buffer is described in a number of useful applications such as boosted op amp, a feed-forward, wide-band DC stabilized buffer, a video line driver amplifier, a fast sample-hold with hold step compensation, an overload protected motor speed controller, and a piezoelectric fan servo.

AN5 **Thermal Techniques in Measurement and Control Circuitry**

6 applications utilizing thermally based circuits are detailed. Included are a 50MHz RMS to DC converter, and anemometer, a liquid flowmeter and others. A general discussion of thermodynamic considerations involved in circuitry is also presented.

AN6 **Applications of New Precision Op Amps**

Application considerations and circuits for the LT1001 and LT1002 single and dual precision amplifiers are illustrated in a number of circuits, including strain gauge signal conditioners, linearized platinum RTD circuits, an ultra precision dead zone circuit for motor servos and other examples.

AN7 **Some Techniques for Direct Digitization of Transducer Outputs**

Analog-to-digital conversion circuits which directly digitize low level transducer outputs, without DC preamplification, are presented. Covered are circuits which operate with thermocouples, strain gauges, humidity sensors, level transducers and other sensors.

AN8 **Power Conditioning Techniques for Batteries**

A variety of approaches for power conditioning batteries is given. Switching and linear regulators and converters are shown, with attention to efficiency and low power operation. 14 circuits are presented with performance data.

AN9 **Application Considerations and Circuits for a New Chopper-Stabilized Op Amp**

A discussion of circuit, layout and construction considerations for low level DC circuits includes error analysis of solder, wire and connector junctions. Applications include sub-microvolt instrumentation and isolation amplifiers, stabilized buffers and comparators and precision data converters.

AN10 **Methods for Measuring Op Amp Settling Time**

The AN10 begins with a survey of methods for measuring op amp settling time. This commentary develops into circuits for measuring settling time to 0.0005%. Construction details and results are presented. Appended sections cover oscilloscope overload limitations and amplifier frequency compensation.

AN11 **Designing Linear Circuits for 5V Operation**

This note covers the considerations for designing precision linear circuits which must operate from a single 5V supply. Applications include various transducer signal conditioners, instrumentation amplifiers, controllers and isolated data converters.

AN12 **Circuit Techniques for Clock Sources**

Circuits for clock sources are presented. Special attention is given to crystal-based designs including TXCOs and VXCOs.

AN13 **High Speed Comparator Techniques**

The AN13 is an extensive discussion of the causes and cures of problems in very high speed comparator circuits. A separate applications section presents circuits, including a 0.025% accurate 1Hz to 30MHz V/F converter, a 200ns 0.01% sample-hold and a 10MHz fiber-optic receiver. Five appendices covering related topics complete this note.

AN14 **Designs for High Frequency Voltage-to-Frequency Converters**

A variety of high performance V/F circuits is presented. Included are a 1Hz to 100MHz design, a quartz-stabilized type and a 0.0007% linear unit. Other circuits feature 1.5V operation, sine wave output an nonlinear transfer functions. A separate section examines the trade-offs and advantages of various approaches to V/F conversion.

AN15 **Circuitry for Single Cell Operation**

1.5V powered circuits for complex linear functions are detailed. Designs include a V/F converter, a 10-bit A/D, sample-hold amplifiers, a switching regulator and other circuits. Also included is a section of component considerations for 1.5V powered linear circuits.

AN16 **Unique IC Buffer Enhances Op Amp Designs, Tames Fast Amplifiers**

This note describes some of the unique IC design techniques incorporated into a fast, monolithic power buffer, the LT1010. Also, some application ideas are described such as capacitive load driving, boosting fast op amp output current and power supply circuits.

AN17 **Consideration for Successive Approximation A/D Converters**

A tutorial on SAR type A/D converters, this note contains detailed information on several 12-bit circuits. Comparator, clocking, and preamplifier designs are discussed. A final circuit gives a 12-bit conversion in 1.8µs. Appended sections explain the basic SAR technique and explore D/A considerations.

AN18 **Power Gain Stages for Monolithic Amplifiers**

This note presents output state circuits which provide power gain for monolithic amplifiers. The circuits feature voltage gain, current gain, or both. Eleven designs are shown, and performance is summarized. A generalized method for frequency compensation appears in a separate section.

AN19 **LT1070 Design Manual**

This design manual is an extensive discussion of all standard switching configurations for the LT1070; including buck, boost, flyback, forward, inverting and "Cuk." The manual includes comprehensive information on the LT1070, the external components used with it, and complete formulas for calculating component values.

AN20 **Applications for a DC Accurate Lowpass Switched-Capacitor Filter**

Discusses the principles of operation of the LTC1062 and helpful hints for its application. Various application circuits are explained in detail with focus on how to cascade two LTC1062s and how to obtain notches. Noise and distortion performance are fully illustrated.

AN21 **Composite Amplifiers**

Applications often require an amplifier that has extremely high performance in several areas. For example, high speed and DC precision are often needed. If a single device cannot simultaneously achieve the desired characteristics, a composite amplifier made up of two (or more) devices can be configured to do the job. AN21 shows examples of composite approaches in designs combining speed, precision, low noise and high power.

AN22 **A Monolithic IC for 100MHz RMS/DC Conversion**

AN22 details the theoretical and application aspects of the LT1088 thermal RMS/DC converter. The basic theory behind thermal RMS/DC conversion is discussed and design details of the LT1088 are presented. Circuitry for RMS/DC converters, wide-band input buffers and heater protection is shown.

AN23 **Micropower Circuits for Signal Conditioning**

Low power operation of electronic apparatus has become increasingly desirable. AN23 describes a variety of low power circuits for transducer signal conditioning. Also included are designs for data converters and switching regulators. Three appended sections discuss guidelines for micropower design, strobed power operation and effects of test equipment on micropower circuits.

AN24 **Unique Applications for the LTC1062 Lowpass Filter**

Highlights the LTC1062 as a lowpass filter in a phase lock loop. Describes how the loop's bandwidth can be increased and the VCO output jitter reduced when the LTC1062 is the loop filter. Compares it with a passive RC loop filter.

Also discussed is the use of LTC1062 as simple bandpass and bandstop filter.

AN25 **Switching Regulators for Poets**

Subtitled "A Gentle Guide for the Trepidatious," this is a tutorial on switching regulator design. The text assumes no switching regulator design experience, contains no equations, and requires no inductor construction to build the circuits described.

Designs detailed include flyback, isolated telecom, off-line, and others. Appended sections cover component considerations, measurement techniques and steps involved in developing a working circuit.

AN26 A collection of interface applications between various microprocessors/controllers and the LTC1090 family of data acquisition systems. The note is divided into sections specific to each interface. The following sections are available:

Number	A/D	Microprocessor/ Microcontroller
AN26A	LTC1090	8051
AN26B	LTC1090	68HC05
AN26C	LTC1090	63705
AN26D	LTC1090	COP820
AN26E	LTC1090	TMS7742
AN26F	LTC1090	COP402N
AN26G	LTC1091	8051
AN26H	LTC1091	68HC05
AN26I	LTC1091	COP820
AN26J	LTC1091	TMS7742
AN26K	LTC1091	COP402N
AN26L	LTC1091	HD63705VO
AN26M	LTC1090	TMS320C25
AN26N	LTC1091/92	TMS320C25
AN26O	LTC1090	Z-80
AN26P	LTC1090	HD64180
AN26Q	LTC1091	HD64180
AN26R	LTC1094	TMS320C25

These interface notes demonstrate the ease with which the LTC1090 family can be interfaced to microprocessors/controllers having either parallel or serial ports. A complete hardware and software description of the interface is included.

AN27A **A Simple Method of Designing Multiple Order All Pole Bandpass Filters by Cascading 2nd Order Sections**

Presents two methods of designing high quality switched-capacitor bandpass filters. Both methods are intended to vastly simplify the mathematics involved in filter design by using tabular methods. The text assumed no filter design experience but allows high quality filters to be implemented by techniques not presented before in the literature. The designs are implemented by numerous examples using devices from LTC's Switched-Capacitor filter family: LTC1060, LTC1061, and LATC1064. Butterworth and Chebyshev bandpass filters are discussed.

AN28 **Thermocouple Measurement**

Considerations for thermocouple-based temperature measurement are discussed. A tutorial on temperature sensors summarizes performance of various types, establishing a perspective on thermocouples. Thermocouples are then focused on. Included are sections covering cold-junction compensation, amplifier selection, differential/isolation techniques, protection, and linearization. Complete schematics are given for all circuits. Processor-based linearization is also presented with the necessary software detailed.

AN29 **Some Thoughts on DC/DC Converters**

This note examines a wide range of DC/DC converter applications. Single inductor, transformer, and switched-capacitor converter designs are shown. Special topics like low noise, high efficiency, low quiescent current, high voltage, and wide-input voltage range converters are covered. Appended sections explain some fundamental properties of different types of converters.

AN30 **Switching Regulator Circuit Collection**

Switching regulators are of universal interest. Linear Technology has made a major effort to address this topic. A catalog of circuits has been compiled so that a design engineer can swiftly determine which converter type is best. This catalog serves as a visual index to be browsed through for a specific or general interest.

AN31 **Linear Circuits for Digital Systems**

Subtitled "Some Affable Analogs for Digital Devotees," discusses a number of analog circuits useful in predominantly digital systems. V_{PP} generators for flash memories receive extensive treatment. Other examples include a current loop transmitter, dropout detectors, power management circuits, and clocks.

AN32 **High Efficiency Linear Regulators**

Presents circuit techniques permitting high efficiency to be obtained with linear regulation. Particular attention is given to the problem of maintaining high efficiency with widely varying inputs, outputs and loading. Appendix sections review component characteristics and measurement methods.

AN33 **Converting Light to Digits: LTC1099 Half-Flash 8-Bit A/D Converter Digitizes Photodiode Array**

This application note describes a Linear Technology "Half-Flash" A/D converter, the LTC1099, being connected to a 256 element line scan photodiode array. This technology adapts itself to hand-held (i.e., low power) bar code readers, as well as high resolution automated machine inspection applications.

AN34 **LTC1099 Enables PC-Based Data Acquisition Board to Operate DC-20kHz**

A complete design for a data acquisition card for the IBM PC is detailed in this application note. Additionally, C language code is provided to allow sampling of data at speed of more than 20kHz. The speed limitation is strictly based on the execution speed of the "C" data acquisition loop. A "Turbo" XT can acquire data at speeds greater than 20kHz. Machines with 80286 and 80386 processors can go faster than 20kHz. The computer that was used as a test bed in this application was an XT running at 4.77MHz and therefore all system timing and acquisition time measurements are based on a 4.77MHz clock speed.

AN35 **Step-Down Switching Regulators**

Discusses the LT1074, an easily applied step-down regulator IC. Basic concepts and circuits are described along with more sophisticated applications. Six appended sections cover LT1074 circuitry detail, inductor and discrete component selection, current measuring techniques, efficiency considerations and other topics.

AN36 A collection of interface applications between various microprocessors/controllers and the LTC1290 family of data acquisition systems. The note is divided into sections specific to each interface. The following sections are available:

Number	A/D	Microprocessor/ Microcontroller
AN36A	LTC1290	8051
AN36B	LTC1290	MC68HC05
AN36C	LTC1290/LTC1090	TMS370
AN36D	LTC1290	COP820C
AN36E	LTC1290	TMS7742
AN36F	LTC1290	COP402N
AN36O	LTC1290	Z-80
AN36P	LTC1290	HD64180

These interface notes demonstrate the ease with which the LTC1290 can be interfaced to microprocessors/controllers having either parallel or serial ports. A complete hardware and software description of the interface is included.

AN37 **Fast Charge Circuits for NiCad Batteries**

Safe, fast charging of NiCad batteries is attractive in many applications. This note details simple, thermally-based fast charge circuitry for NiCads. Performance data is summarized and compared to other charging methods.

AN38 **FilterCAD User's Manual, Version 1.00**

This note is the manual for FCAD, a computer-aided design program for designing filters with LTC's switched-capacitor filter family. FCAD helps users design good filters with a minimum amount of effort. The experienced filter designer can use the program to achieve better results by providing the ability to play "what if" with the values and configuration of various components.

AN39 **Parasitic Capacitance Effects in Step-Up Transformer Design**

This note explores the causes of the large resonating current spikes on the leading edge of the switch current waveform. These anomalies are exacerbated in very high voltage designs.

AN40 **Take the Mystery Out of the Switched-Capacitor Filter: The System Designer's Filter Compendium**

This note presents guidelines for circuits utilizing LTC's switched-capacitor filters. The discussion focuses on how to optimize filter performance by optimizing the printed wiring board, the power supply, and the output buffering of the filter. Many additional topics are discussed such as how to select the proper filter response for the application and how to characterize a filter's THD for DSP applications.

A GUIDE TO THE INDEX

Linear Technology has made a major effort to address a wide variety of circuit topics. The number of application problems solvable with innovative circuit techniques or new linear integrated circuits continues to grow at a impressive rate. This comprehensive index includes Application Notes (AN1-AN55), Design Notes (DN1-DN68) and Data Sheets circuits (through January 1993).

The category and subject index are organized so that application circuits and subject tutorials are easily found. The major categories are broken up into specialized topics to help isolate a particular application. The subject index works as follows, i.e. AN8, Pg. 8 = Application Note 8, page 8; LTC1044 DS = LTC1044 Data Sheet; DN17, Pg. 1 = Design Note 17, page 1.

NOTE: Application Notes 1 through 40 and Design Notes 1 through 32 are found in 1990 Applications Handbook. All other Application Notes and Design Notes are in this Volume II Book.

LTC LITERATURE SUBJECT INDEX

A-D—See Converter-Data

ACCELEROMETER—See Signal Conditioning

ACOUSTIC THERMOMETER—See Signal Conditioning-Temperature

AMPLIFIER

Absolute Value

Precision Absolute Value Circuit: LT1001 DS; LT1002 DS
Wide Bandwidth Absolute Value Circuit: LT1022 DS; LT1122 DS
Precision Absolute Value Circuit: OP05 DS

Additional Feature Circuits

DC and AC Zeroing: LF198 DS
Inverting Amplifier with High Input Resistance: LM108 DS
Constant Gain Amplifier Over Temperature: LT1004 DS
Ammeter with Six Decade Range: LT1008 DS; LT1012 DS
Five Decade Kelvin-Varley Divider: LT1008 DS
Input Amplifier For 4-1/2 Digit Voltmeter: LT1008 DS; LT1012 DS
DC Stabilized FET Probe: LTC1052 DS

Artifical Ground

Synthetic Ground: AN50, Pg. 5

Audio

Very Low Distortion Buffered Pre-Amplifier: AN52, Pg. 15, LT1010 DS
Balanced Transformerless Microphone Preamp: LT1115 DS
High Performance Transformer Coupled Microphone Pre-Amp: LT1115 DS
Low Noise DC Accurate X 10 Buffered Line Amplifier: LT1115 DS
Moving Coil Passive RIAA Phonograph Pre-Amp: LT1115 DS
RIAA Moving Coil "Pre-Pre" Amplifier: LT1115 DS
RIAA Phonograph Preamplifier (40dB/60dB Gain): LT1115 DS

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Basic Boosted Op Amp (150mA): AN4, Pg. 1
Increasing Output Current (10mA-20mA): AN9, Pg. 18
Increasing Output Current and Voltage (±12V at 20mA): AN9, Pg. 18
1.5V Voltage Boosted Output Op Amp (0V-10V): AN15, Pg. 6
LT1010, Paralleling: AN16, Pg. 17
Fast Power Buffer (10MHz): AN16, Pg. 20
High Current Booster (3A): AN18, Pg. 2
Output Stage (150mA): AN18, Pg. 2
Ultra Fast Feed Forward Current Booster (1000V/µs, 14MHz, 200mA): AN18, Pg. 3

- Low Output Saturation: AN18, Pg. 4; AN50, Pg. 2; LTC1052 DS
- High Current Rail to Rail Output Stage (100mA): AN18, Pg. 5
- Output Stage (±120V Swing): AN18, Pg. 7; LT1055 DS
- Output Stage (±150V Swing): AN18, Pg. 8
- Unipolar Output, Gain Stage (1000V Swing): AN18, Pg. 9
- ±15V Powered, Bipolar Output, Voltage Gain Stage, (±100V Swing): AN18, Pg. 11
- Paralleling for High Current: AN21, Pg. 12
- Fast-200mA: AN47, Pg. 46; LT1220 DS
- Fast, 1A Booster Stage: AN47, Pg. 47; LT1220 DS
- Precision Amplifier Drives 500Ω Load to ±10V: LT1002 DS
- Precision Amplifier Drives 300Ω Load to ±10V: LT1007 DS; OP227 DS
- High Output Current Op Amp: LT1022 DS; AN16, Pg. 15; LTC1052 DS
- Instrumentation Amplifier with ±150mA Output Current: LT1101 DS; LT1102 DS
- Increasing Output Current and Voltage: LTC1052 DS

Buffer

- Fast, Stabilized FET Buffer (FET Probe): AN9, Pg. 9
- Input Buffer for the LT1088: AN22, Pg. 12
- Large Signal Voltage Follower: LT1001 DS
- Fast ±150mA Power Buffer: LT1010 DS

Clamping Techniques

- Precision Adjustable Dead Zone Generator: AN6, Pg. 5; LT1001 DS; LT1002 DS
- Precision Clamp: LM129 DS

Composite

- DC Stabilized Fast Amplifier (23V/µs, 300kHz FPB): AN21, Pg. 1
- Fast DC Stabilized FET Amplifier (100V/µs, 1MHz FPB): AN21, Pg. 2
- DC Stabilized-Summing Point Correction: AN47, Pg. 33
- DC Stabilized-Input Stage Current Correction: AN47, Pg. 34
- DC Stabilized-Offset Pin Correction: AN47, Pg. 34
- DC Stabilized-Full Differential, Parallel Path: AN47, Pg. 35
- DC Stabilized-Full Differential, Parallel Path, A = 1000: AN47, Pg. 36
- Fast Summing Amplifier; LM108 DS; LTC1052 DS; LH2108 DS

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- "Current Mode Feedback" Amplifier (1MHz FPB): AN21, Pg. 7; AN22, Pg. 12; LT1088 DS
- "Current Mode Feedback" (Son of Godzilla Amplifier) (3000V/µs, 25MHz FPB): AN21, Pg. 8; AN22, Pg. 13; LT1088 DS

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- Simple Pre-Amplifier for the Comparator: AN17, Pg. 4
- "No Trims" 12-Bit Multiplying DAC Output Amplifier: AN47, Pg 32; LT1022 DS; LT1122 DS
- Fast Settling 12-Bit DAC Buffer: LT1220 DS
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- Chopper Stabilized Op Amps: AN9, Pg. 19
- Amplifier Compensation: AN10, Pg. 8
- LT1010, Performance Summary: AN16, Pg. 7
- Frequency Compensation: AN18, Pg. 12
- Perspectives on High Speed Design: AN47, Pg. 7
- Perspectives on Speed: AN47, Pg. 7
- Typical High Speed Amplifier Problem: AN47, Pg. 7
- High Speed Effects in Cable, Connectors and Termination: AN47, Pg. 15
- High Frequency Amplifier Evaluation Board: AN47, Pg. 127
- Operational Amplifier Selection Guide for Optimum Noise Performance: DN3, Pg. 1
- Chopper vs Bipolar Op Amps: DN42, Pg. 1
- Demo DC009 High Frequency Amplifier: DN50, Pg. 1
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- Input Protection: LM108 DS
- Advantages of Matched Dual Op Amps: LT1002 DS; OP227 DS; LT1024 DS
- Gain of 1000 Amplifier with 0.01% DC Accuracy: LT1007 DS
- Achieving Picoampere/Microvolt Performance: LT1008 DS; LT1012 DS; LTC1052 DS
- Frequency Compensation: LT1008 DS
- Isolating Capacitive Loads: LT1010 DS
- High Speed Operation: LT1055 DS
- Phase Reversal Protection: LT1055 DS

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Divide by 4: LTC1043 DS
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- Obtaining Ultra Low V_{OS} Drift and Low Noise: LTC1051 DS
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- 150mA Output Current Video Amp: LT1223 DS

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BYPASSING—See Capacitors

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Switcher

Contact Factory to Get SwitcherCAD

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CHRISTIE, S. H.

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Driving Ground Referred Load: LT1011 DS; LT311A DS

Driving Load Referenced to Negative Supply: LT1011 DS; LT311A DS

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Fast Current Comparator (16-Bit): LT1055 DS

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Discussion

High Speed Comparator Problems: AN13, Pg. 4

Input Protection: LT1011 DS

Input Signal Range: LT1011 DS

Input Slew Rate Limitations: LT1011 DS

Preventing Oscillation Problems: LT1011 DS

Strobing: LT1011 DS

High Speed Design Techniques: LT1016 DS

Input Impedance and Bias Current: LT1016 DS

Measuring Response Time: LT1016 DS

Hysteresis
  - Comparator with Hysteresis: LT1011 DS; LT685 DS
  - Low Power Comparator with <10µV Hysteresis: LT1012 DS; LT1097 DS

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  - Fully Isolated Limit Comparator (500V Iso.): AN11, Pg. 10; LT1017 DS

Level Shift
  - Output Level Shifting: AN13, Pg. 31

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  - Dual Limit Microvolt Comparator: OP227 DS

One Shot
  - Voltage Controlled High Speed One Shot: LT319A DS

Precision
  - Offset Stabilized Comparator: AN9, Pg. 11; LTC1052 DS
  - Microvolt Comparator with TTL Output: LT1001 DS
  - Dual Limit Microvolt Comparator: LT1002 DS
  - Microvolt Comparator with Hysteresis: LT1007 DS

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Ultra Fast
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  - Window Detector: LT1011 DS: LT311A DS
  - 1.5V Powered Refrigerator Alarm: LT1017 DS
  - Window Comparator with Symmetric Window Limits: LTC1040 DS
  - Window Comparator: LTC1042 DS
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Zero Crossing
  - Fast Zero Crossing Detector: LT1116 DS

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Cooler
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AC-F
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  - Bipolar Input (AC) V-F Converter: LT1058 DS
  - Bipolar (AC) Input V-F Converter: LTC203 DS

Capacitance-Frequency
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Capacitance-Pulse Width
  - Capacitance to Pulse Width Converter: LT1011 DS

DC-AC
  - Sine Wave Output Converter (115VAC): AN8, Pg. 11
  - LT1074 Based 400Hz Sine Wave Output (28V to 110V_{AC}): AN35, Pg. 15

DC-DC—See Regulator-Switching

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  - V-F, Techniques: AN14, Pg. 18
  - Successive Approximation Techniques: AN17, Pg. 8
  - Thermal RMS-DC Converters: AN22, Pg. 1; LT1088 DS
  - Analog Considerations for Interfacing the LTC1090 10-Bit DA System: LTC1090 DS
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F-V
  - Frequency to Voltage: AN3, Pg. 11

Pulse Width-Voltage
  - Fast Time to Height Converter: AN47, Pg. 60; LT1220 DS
  - Pulse Width to Voltage Converter: LF198 DS

RMS-DC
  - 50MHz Thermal RMS to DC Converter: AN5, Pg. 4; LT1013 DS
  - Thermal RMS-DC Converter (100MHz): AN22, Pg. 5; LT1088 DS
  - Fast Settling RMS-DC Converter: AN22, Pg. 9; LT1088 DS
  - Servo-Sensed Heater Protection Circuit: AN22, Pg. 10
  - 50MHz Thermal RMS-DC Converter: LTC1043 DS

V-F

Voltage to Frequency (0kHz-30kHz, 0V-3V): AN3, Pg. 11; LTC1043 DS
Offset Stabilizing a V-F Converter: AN9, Pg. 12
Voltage to Frequency (1Hz-1.25MHz, 0V-5V): AN9, Pg. 13
Voltage to Frequency (1Hz-10MHz, 0V-10V): AN13, Pg. 9; LT1016 DS
Quartz Stabilized, Voltage to Frequency (1Hz-30MHz, 0V-10V): AN13, Pg. 11
Voltage to Frequency (1Hz-100MHz, 0V-10V: King Kong V-F): AN14, Pg. 2
Fast Response Voltage to Frequency (1Hz-2.5MHz, 0V-5V): AN14, Pg. 4
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Charge Pump 1/V_{IN} to Frequency (0V-5V to 10kHz-50Hz): AN14, Pg. 13
Exponential to Frequency (0V-10V to 20Hz-20kHz): AN14, Pg. 15
1.5V Voltage to Frequency Converter (0V-1V to 25Hz-10kHz): AN15, Pg. 1
Micropower V-F Converter (0V-5V to 0kHz-10kHz): AN23, Pg. 11
Micropower V-F Converter, 0.02% Linearity (0V-5V to 0MHz-1MHz): AN23, Pg. 13; LT1006 DS
90µA Supply Current V-F, 0.05% Linearity (0V-5V to 0kHz-10kHz): AN45, Pg. 15
Voltage to Frequency Converter (1Hz-10MHz): AN47, Pg. 54
Single Supply (0V-5V to 0kHz-5kHz): AN50, Pg. 7
Micropower V-F Converter (0V-5V to 100Hz-1MHz): DN38, Pg. 1; LTC201 DS
Extended Range Charge Pump V-F (0V-10V to 0.01Hz-10kHz): LT1008 DS
Voltage to Frequency Converter (10Hz-100kHz): LT1011 DS
Voltage to Frequency Converter (1Hz-1MHz): LT1012 DS
Low Power V-F Converter (0V-1V to 0kHz-1kHz): LT1018 DS
Voltage to Frequency Converter (10Hz-1MHz): LT1022 DS
Exponential Voltage to Frequency Converter: LT1055 DS
Voltage to Frequency Converter (0Hz-10kHz): LT1055 DS
Voltage to Frequency Converter (5kHz-2MHz): LT119A DS
Single 5V Voltage to Frequency Converter: LTC1040 DS
Voltage to Frequency Converter (1Hz-1.25MHz): LTC1052 DS
Voltage to Frequency Converter (1Hz-30MHz): LTC1052 DS

Voltage-Pulse Width

Voltage Controlled Pulse Width Generator: LT1016 DS

CONVERTER—DATA

A-D

Extending Resolution: AN50, Pg. 6
4 Digit (10,000 Count) A-D Converter: LT1011 DS

A-D 8-Bits

Half Flash 8-Bit A/D Digitizes Photodiodes: AN33, Pg.1
Data Acquisition Board: AN34, Pg. 1
Floating 8-Bit Data Acquistion System: AN52, Pg. 4; LTC1096 DS
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3V Battery Powered, 10µW, 8-Bit A-D, Samples at 200Hz: LTC1096 DS
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A-D 10-Bits

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Micropower A-D (10-Bit, 100µs): AN23, Pg. 9
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Interfacing LTC1090 to MC68HC05: AN26B, Pg. 1
Interfacing LTC1090 to MC68HC11: AN26B, Pg. 1
Interfacing LTC1090 to HD63705V0: AN26C, Pg. 1
Interfacing LTC1090 to COP800: AN26D, Pg. 1
Interfacing LTC1090 to TMS7000: AN26E, Pg. 1
Interfacing LTC1090 to COP400: AN26F, Pg. 1
Interfacing LTC1091 to 8051: AN26G, Pg. 1
Interfacing LTC1091 to 68HC05: AN26H, Pg. 1
Interfacing LTC1091 to 68HC11: AN26H, Pg. 1
Interfacing LTC1091 to COP800: AN26I, Pg. 1
Interfacing LTC1091 to HD6305VO: AN26L, Pg. 1
Interfacing LTC1091 to HD63705V0: AN26L, Pg. 1
Interfacing LTC1091/2 to TMS320C25: AN26N, Pg. 1

Data Acq. Syst. Uses 4 Wires: DN1, Pg. 1
Auto-Zeroing A/D Offset Voltage: DN26, Pg. 1
RS232 Compatible 10-Bit A-D Converter: LT1080 DS
10-Bit Serial Output A/D Converter: LT119A DS
A Quick Look Circuit for the LTC1090 10-Bit A/D System: LTC1090 DS
Hitachi Synchronous SCI (HD63705) Interface: LTC1090 DS
Intel 8051 Interface: LTC1090 DS
Motorola SPI (MC68HC05C4) Interface: LTC1090 DS
National Microwire (COP420) Interface: LTC1090 DS
Single Chip 8 Input Data Acquisition System: LTC1090 DS
Sneak-A-Bit Code for 10-Bits Plus Sign: LTC1090 DS
2-Channel, 10-Bit Serial A-D: LTC1091 DS
A Quick Look Circuit for the LTC1091: LTC1091 DS
Intel 8051 Interface: LTC1091 DS
Motorola SPI (MC68HC05C4, MC68HC11) Interface: LTC1091 DS
Auto Ranging an 8-Channel, 10-Bit A/D Converter: LTC221/222 DS

A-D 12-Bits

12-Bit A-D: AN3, Pg. 12
SAR Converter (12-Bit, 5μs): AN13, Pg. 19
Successive Approximation A-D Converter (12-Bits, 12μs): AN17, Pg. 1; LT1011 DS
A-D Converter (12-Bits, 7.5μs): AN17, Pg. 3
Successive Approximation A-D Converter (12-Bits, 1.8μs): AN17, Pg. 6
Micropower A-D (12-Bit, 300μs): AN23, Pg. 7
Interfacing LTC1290 to 8051: AN36A, Pg. 1
Interfacing LTC1290 to MC68HC05: AN36B, Pg. 1
Interfacing LTC1290 to MC68HC11: AN36B, Pg. 1
Interfacing LTC1290 to COP800: AN36D, Pg. 1
Interfacing the LTC1290 to the TMS7742 MCU: AN36E, Pg. 1
Interfacing LTC1290 to COP400: AN36F, Pg. 1
Interfacing the LTC1290 to the Z-80 MPU: AN36O, Pg. 1
Floating, 12-Bit Data Acquistion System: AN52, Pg. 3
LTC1290 to IBM PC Serial Port Interface: DN35, Pg. 1
High Speed Sampling: DN66, Pg. 1
4μs, 12-Bit SAR Converter: LT1016 DS
12-Bit Charge Balance Analog to Digital Converter: LT1055 DS
12-Bit A-D Converter: LT1058 DS
Plugging the LTC1272 into an AD7572 Socket: LTC1272 DS
Single 5V Supply, 3μs, 12-Bit Sampling ADC: LTC1272 DS
3V Powered, 12-Bit A-D: LTC1289 DS
A “Quick Look” Circuit for the LTC1290: LTC1290 DS
Several LTC1290s Sharing One 3-Wire Serial Interface: LTC1290 DS
Single Chip Data Acq. System: LTC1290 DS
Sneak-A-Bit Circuit: LTC1290 DS
Two-Channel, 12-Bit, Self Calibrating Data Acquisition System: LTC221/222 DS

A-D 14-Bits

8-Channel, 14-Bit A/D Converter: LTC221/222 DS

A-D 16-Bits

Analog to Digital (16-Bits): AN9, Pg. 16
16-Bit Analog to Digital Converter: LTC1052 DS

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PC Based Data Acquisition: AN34, Pg. 1
New Data Acquisition System Communicates with Microprocessors Over 4 Wires: DN1, Pg. 1
Data Acquisition System Showing Sample and Hold Synchronizing Circuitry: DN2, Pg. 1
Opto Isolated, Multi-Channel Data Acquisition System (10-Bit, 500V Iso.): DN10, Pg. 2
Closed Loop Control with the LTC 1090: DN13, Pg. 1
Two-Wire Isolated and Powered 10-Bit Data Acquisition System: DN19, Pg. 1
12-Bit Data Acquisition Systems Communicate with Microprocessors Over 4 Wires: DN22, Pg. 1
Multiplexed Input Data Acquisition: LT1102 DS

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Overvoltage Protection for MUX: LTC1290 DS

Low Power

3V Powered, 12-Bit A-D: LT1289 DS

Micropower

3V Battery Powered, 10μW, 8-Bit A-D, Sample at 200Hz: LTC1096 DS

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Equation

9 Isn’t 10: AN22, Pg. 4

CURRENT

Sensing

Circuit Breaker (700ns): AN1, Pg. 3
Precision Current Sensing in Supply Rails: AN3, Pg. 13; LTC1043 DS
Circuit Breaker (12ns): AN13, Pg. 24
Fast High Side, High Current Limit: AN30, Pg. 44
18ns Circuit Breaker with Voltage Programmable Trip Point: AN47, Pg. 66
5V/1A Electronic Circuit Breaker with 1ms Trip Delay: AN53, Pg. 15; LTC1153 DS
In Line Current Limiter: LM134 DS
Dual 5A Circuit Breaker with Auto-Reset: LTC1155 DS
Over-Temperature Circuit Breaker: LTC1155 DS
Precision Current Sensing in Supply Rails: LTC203 DS

Sink

Precision Current Sink: LT1001 DS

Source

Voltage Controlled Current Source with Ground Referred Input and Output: AN3, Pg. 13; LT1013 DS
Bidirectional Current Source: AN16, Pg. 19
Voltage Controlled Current Source: AN16, Pg. 20
Voltage Programmable Current Source: AN45, Pg. 5; LT1101 DS; LT1102 DS
Fast, Precise, Voltage Controlled Current Source with Grounded Load: AN47, Pg. 65
High Power, Wideband Voltage Controlled Current Source: AN47, Pg. 65
Voltage Programmable Current Source is Simple and Precise: DN40
2-Terminal Current Regulator: LM10 DS
Bilateral Current Source: LM108 DS
20mA Positive Current Source: LM129 DS
Basic 2-Terminal Current Source: LM134 DS
Better Temperature Coefficient Current Source: LM134 DS
FET Cascoding for Low Capacitance and/or Ultra High Output Impedance: LM134 DS
High Precision Low TC Current Source: LM134 DS
Higher Output Current: LM134 DS
Micropower Bias: LM134 DS
Precision 10nA Current Source: LM134 DS
Precision Current Source: LT1001 DS
Ground Reference Current Source: LT1004 DS
Low Temperature Coefficient 2-Terminal Current Source: LT1004 DS
Precision Current Source (1μA): LT1019 DS; LT1021 DS
Fast, Differential Input Current Source: LT1022 DS
Current Regulator: LT1033 DS; LT137 DS
2-Terminal Current Source: LT1077 DS
Differential Voltage to Current Converter: LTC1053 DS

CURRENT LOOP

Receiver

4mA-20mA Loop Receiver: LT1101 DS

Transmitter

4mA-20mA Current Loop Transmitter: AN11, Pg. 9; LT1013 DS
4mA-20mA Floating Output for Current Loop Transmitter: AN11, Pg. 10; LT1013 DS
Digitally Controlled 4mA-20mA Current Loop Generator: AN31, Pg. 6
Fully Floating 4mA-20mA Current Loop Transmitter: AN45, Pg. 6
2-Wire 0°C to 100°C Temperature Transducer with 4mA-20mA Output: LTC1040 DS

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DC-DC—See Regulator-Switching

DEFOREST, LEE

Amplifier: AN18, Pg. 8; AN43, Pg. 41; AN43, Pg. 43

DETECTORS—See Signal Conditioning

DIGITAL HELP CIRCUITS

Additional Feature Circuits

Battery Detectors Sense Removal of Main Battery: AN51, Pg. 16
Logic System DC Isolation: LTC1045 DS
Battery Discharge Monitor: LTC1150 DS
Ground Force Reference: LTC1150 DS

EEPROM

EEPROM V_{PP} Pulse Generator: AN31, Pg. 5
EEPROM Pulse Generator: LT1013 DS

EPROMs

V_{PP} Generator for EPROMs-No Trim Required: LT1004 DS

Flash Memory

Basic Flash Memory V_{PP} Programming Voltage Supply: AN31, Pg. 1; DN17, Pg. 1

High Repetition Rate V_{PP} Programming Supply: AN31, Pg. 2; DN17, Pg. 2

High Power, High Repetition Rate V_{PP} Pulse Generator: AN31, Pg. 3

V_{PP} Handshake Circuit: AN31, Pg. 4

Flash Memory V_{PP} Generator Delivers 12V: AN51, Pg. 15

All Surface Mount Flash Memory V_{PP} Generator: AN52, Pg. 13; DN58, Pg. 1; LT1109 DS

All Surface Mount Flash Memory V_{PP} Generator: LT1110 DS

Notebook Computer

Bi-Directional Battery Switch: AN53, Pg. 3

A 4-Cell NiCad Computer Power Management System: AN53, Pg. 11; LTC1156 DS

Logic Controlled Battery Switch: LTC1153 DS; LTC1157 DS; LTC1255 DS

Slow Turn On Power Switch: LTC1154 DS; LTC1157 DS

Supply Monitor

AC-DC Dropout Detector: AN31, Pg. 7

Power Supply Monitor: DN20, Pg. 2

6V Battery Level Indicator: LM10 DS

Lead Acid Low Battery Detector: LT1004 DS

Battery Voltage Sensing Circuit: LT1005 DS; LT1035 DS

5V Powered Supply Monitor: LT1017 DS

Delay on Power Up: LT1017 DS

Power Supply Monitor: LT1018 DS

TTL Power Supply Monitor: LTC1042 DS

Microprocessor Supervisory Circuit: LTC1232 DS; LTC690 DS

Watchdog Timer

Watchdog Timer: AN31, Pg. 10

Microprocessor Supervisory Circuit: LTC1232DS; LTC690 DS

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Discussion

Understanding Distortion Measurements: AN43, Pg. 44

DRAWER

Inductor

Inductor Selection: AN35, Pg. 22

DRIFT

Discussion

Minimizing Thermal EMFs: AN9, Pg. 2

DRIVER

Automotive

High Side Driver with Reverse Battery Protection: AN53, Pg. 9

Capacitor

Slew Rate Reduction for Large Capacitive Loads: AN53, Pg. 3

HIGH SIDE

18V-28V High Side Driver: AN53, Pg. 4; LTC1154 DS; LTC1153 DS

Dual High Side 3.3V Switch: AN53, Pg. 12; LTC1157 DS

Lamp

12V Lamp Driver/Circuit Breaker with Auto-Reset: AN53, Pg. 8; LTC1154 DS

High Current Lamp Driver with Short-Circuit Protection: LT1158 DS

Relay

High Side Relay Driver with Over-Current Protection: LTC1153 DS; LTC1154 DS

Solenoid

Driving Inductive Loads: LT1188 DS

High Side Solenoid Driver with Over-Current Protection: LTC1153 DS; LTC1154 DS; LTC1255 DS

DRIVERS/RECEIVERS—See Interface Circuits

EINSTEIN, ALBERT

$E = MC^2$

High Speed Effects on Circuits: AN47, Pg. 5

FIBER OPTIC—See Signal Conditioning-Photodiode

FILTER-ACTIVE RC

Lowpass

Precision, Fast Settling, Lowpass Filter: LT1008 DS

2nd Order Butterworth Filter (to 100kHz): LT1200 DS

4th Order Butterworth Filter (to 100kHz): LT1201/LT1202 DS

4th Order Butterworth Filter (to 1MHz): LT1208/LT1209 DS
2nd Order Lowpass Filter: LT1220 DS
1MHz, 2nd Order Butterworth Filter: LT1224 DS
DC Accurate 18-Bit 4th Order Antialiasing Bessel (Linear Phase), 100Hz, Low: LTC1051 DS
DC Accurate, 3rd Order, 100Hz, Butterworth Antialiasing Filter: LTC1051 DS

FILTER—RESONANT ELEMENT

Crystal Filter: AN47, Pg. 48
Piezo-Ceramic Based Filter: AN47, Pg. 48

FILTER—SWITCHED CAPACITOR

Clock Sweepable Pseudo Bandpass Filters: AN24, Pg. 4
4th Order Butterworth BPF, f_O = 2kHz: AN27A, Pg. 1
Cascading Identical Sections 4th Order BPF at 150 Hz: AN27A, Pg. 4
Mode 24th Order BPF at 150Hz: AN27A, Pg. 5
8th Order Chebychev BPF at 10.2kHz: AN27A, Pg. 13
Wideband DC Accurate BPF: DN9, Pg. 1
10Hz-1000Hz BPF: DN24, Pg. 1
10Hz-100Hz BPF: DN24, Pg. 1
400Hz-10kHz BPF: DN24, Pg. 1
10kHz-100kHz Bandpass Filter: DN37, Pg. 2
High Frequency Clock-Tunable Bandpass Filter: LTC1043 DS
Wide Range 2nd Order Bandpass/Notch Filter with Q = 10: LTC1059 DS
Single 5V, Gain of 1000 4th Order Bandpass Filter: LTC1060 DS
6th Order Elliptic Bandpass Filter Centered Around 2600Hz: LTC1061 DS
6th Order, Clock-Tunable, 0.5dB Ripple Chebyshev BPF: LTC1061 DS
Bandpass w/2 Notches (–60dB Stopband): LTC1064 DS
C Message Filter: LTC1064 DS
Quad Bandpass Filter: LTC1064 DS
Wideband (2:1) Bandpass: LTC1064 DS
8th Order Bandpass (to 150kHz): LTC1264 DS
8th Order Bandpass (to 250kHz): LTC1264 DS
Dual 4th Order Bandpass (to 250kHz): LTC1264 DS

Bandreject—See Notch

Design

Filter CAD User's Manual: AN38, Pg. 1

Discussion

Application Considerations for an Instrumentation Lowpass Filter: AN20, Pg. 1
Cascading Identical BPF Sections: AN27A, Pg. 5
Simple 2nd Order BP Filters: AN27A, Pg. 6
Bandpass Filters: AN27A, Pg. 1
Chebyshev or Butterworth (BPF)?: AN27A, Pg. 13
Take the Mystery Out of the SCF: AN40, Pg. 1
Circuit Board Layout Considerations: AN40, Pg. 2
Power Supplies: AN40, Pg. 5
Offset Voltage Nulling Techniques: AN40, Pg. 7
Aliasing: AN40, Pg. 9
Slew Limiting: AN40, Pg. 9
What Kind of Filter to Use: AN40, Pg. 12
Step Response of Various Filters: AN40, Pg. 13
Frequency Response of Various Filters: AN40, Pg. 14
How Stable Is My Filter?: AN40, Pg. 16
THD and Dynamic Range: AN40, Pg. 16
THD in Active RC Filters: AN40, Pg. 18
Clock Jitter: AN40, Pg. 20
Clock Feedthru: AN40, Pg. 21
Square Wave to Sine Wave Converter: AN40, Pg. 23
SCF LPF for Antialiasing Applications: DN16, Pg. 1
Complex Data Acq. System, Few Components: DN24, Pg. 1
Comments on Modes of Operation: LTC1060 DS
Definition of Filter Functions: LTC1060 DS
LTC1060 Offsets: LTC1060 DS
Modes of Operation: LTC1060 DS; LTC1061 DS
Analog Considerations: Grounding and Bypassing: LTC1064 DS
Buffering, Offset Nulling and Noise: LTC1064 DS
Level Shifting the Input T2L Clock: LTC1064-1 DS; LTC1064-2 DS
Protecting the IC from Power Supply Reversal: LTC1064-1 DS; LTC1064-2 DS
Using Schottky Diodes to Protect the IC: LTC1064-1 DS

Highpass

- 6th Order Elliptic Highpass Filter with Clock to Cutoff Ratio: 250:1: LTC1061 DS

Linear Phase Lowpass

- Low Noise, 8th Order Group Delay Equalized Filter (to 100KHz): LTC1064-7 DS
- Dual 5th Order Linear Phase Filter with Stopband Notch: LTC1164 DS
- Low Power, 8th Order Group Delay Equalized Filter (to 20kHz): LTC1164-7 DS
- Low Noise, 8th Order Group Delay Equalized Filter (to 250kHz): LTC1264-7 DS

Low Power

- 8th Order Lowpass Butterworth: LTC1164 DS
- 8th Order Lowpass Elliptic Filter: LTC1164 DS
- 8th Order Lowpass Single Supply Elliptic-Bessel Filter: LTC1164 DS
- 9th Order Lowpass Elliptic Filter: LTC1164 DS
- Dual 5th Order Linear Phase Filter with Stopband Notch: LTC1164 DS

Lowpass

- RC to Eliminate Clock Feedthru and Improve HF Attenuation Floor: AN20, Pg. 4
- Single Supply LTC1062: AN20, Pg. 4
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- Cascading Two LTC1062's Using the First LTC1062's Buffered Output: AN20, Pg. 7
- Low Offset, 12th Order, Maximum Flat Lowpass Filter: AN20, Pg. 8
- A Lowpass Filter with a 60Hz Notch: AN20, Pg. 10
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- Using Input Divider to Accommodate High Voltages: AN24, Pg. 7
- Using the LTC1062 with Op Amps Operating from ±15V Power Supply: AN24, Pg. 7
- Using a Multiplexer to Obtain Four Different Cutoff Frequencies: AN24, Pg. 8
- Low Power, 8th Order Butterworth Lowpass: AN52, Pg. 10; LT1164-5 DS
- Programmable Cutoff, Fifth-Order Butterworth Lowpass Filter: AN52, Pg. 11
- 8Hz 5th Order Butterworth LPF: DN7, Pg. 1
- 10Hz DC Accurate Bessel LPF: DN9, Pg. 1
- 8th Order Cauer 40kHz LPF: DN16, Pg. 1
- 6th Order Butterworth Lowpass Filter, Cutoff to 45kHz: LTC1061 DS
- 6th Order Chebyshev Filter Using 3 Different Modes for Speed Optimization: LTC1061 DS
- 7th Order Lowpass Elliptic Filter: LTC1061 DS
- 10Hz 5th Order Butterworth Lowpass Filter: LTC1062 DS
- 100Hz, 50Hz, 25Hz, 5th Order DC Accurate LP Filter: LTC1062 DS
- 5th Order Lowpass Filter: LTC1062 DS
- 5th Order Lowpass Filter with a 60Hz Notch: LTC1062 DS
- 7th Order 100Hz Lowpass Filter with Continuous Filtering, Output Buffering: LTC1062 DS
- Filtering AC Signals from High DC Voltages: LTC1062 DS
- Octave Tuning with a Single Input Clock: LTC1062 DS
- Simple Cascading Technique-LTC1062: LTC1062 DS
- Single 5V Supply 5th Order LP Filter: LTC1062 DS
- DC Accurate Clock-Tunable 10th Order Butterworth: LTC1063 DS
- DC Accurate Clock-Tunable 5th Order Butterworth: LTC1063 DS
- 8th Order Bessel w/65:1 f_{CLK}/f_O: LTC1064 DS
- 8th Order Cauer Cutoff up to 100kHz: LTC1064 DS
- 8th Order Cheby. up to 100kHz, Ripple 0.1dB: LTC1064 DS
- 8th Order Elliptic to 50kHz, 0.1dB Ripple: LTC1064 DS
- Dual 4th Order Bessel to 140kHz: LTC1064 DS
- Dual 5th Order Cheby. 50/100kHz Cutoff: LTC1064 DS
- 8th Order Elliptic Antialiasing Filter: LTC1064-1 DS
- Buffering the Filter Output: LTC1064-1 DS
- Dual 5th Order Elliptic/Bessel: LTC1064-1 DS
- Output Buffer Eliminates Clock Feedthru: LTC1064-1 DS
- Single Supply Operation: LTC1064-1 DS; LTC1064-2 DS
- Transitional Elliptic/Bessel 10th Order: LTC1064-1 DS
- 8th Order Clock Sweepable Lowpass Butterworth Filter: LTC1064-2 DS
- 8th Order Butterworth to 140kHz: LTC1064-2 DS
- 8th Order Bessel to 100kHz: LTC1064-3 DS
- 8th Order Elliptic to 100kHz: LTC1064-4 DS
- 8th Order Lowpass Butterworth: LTC1164 DS
- 8th Order Lowpass Elliptic Filter: LTC1164 DS
- 8th Order Lowpass Single Supply Elliptic-Bessel Filter: LTC1164 DS
- 9th Order Lowpass Elliptic Filter: LTC1164 DS

Single 5V, 5mA 16th Order Butterworth Lowpass: LTC1164-5 DS
Low Power, 8th Order Elliptic Lowpass: LTC1164-6 DS
Single 5V, 5mA 16th Order Elliptic Lowpass: LTC1164-6 DS
8th Order Bessel Lowpass (to 250kHz): LTC1264 DS
8th Order Butterworth (to 200kHz): LTC1264 DS
8th Order Elliptic (to 150kHz): LTC1264 DS
Dual 4th Order Bessel Lowpass (to 400kHz): LTC1264 DS

Noise

Bandpass Filters and Noise: AN40, Pg. 19
Noise in Switched Capacitor Filters: AN40, Pg. 19
LTC1060 Wideband RMS Noise: LTC1060 DS
Wideband RMS Noise: LTC1061 DS

Notch

Using the LTC1062 to Create a Notch: AN20, Pg. 9
A Lowpass Filter with a 60Hz Notch: AN20, Pg. 10
Clock-Tunable Notch Filter: AN24, Pg. 6
Wide Range 2nd Order Bandpass/Notch Filter with Q = 10: LTC1059 DS
6th Order Bandreject Filter with 65dB Notch Depth: LTC1061 DS
6th Order Elliptic Notch Centered at 2600Hz: LTC1061 DS
5th Order Lowpass Filter with a 60Hz Notch: LTC1062 DS
60dB Notch Tunable 30kHz-90kHz: LTC1064 DS
8th Order Notch (to 150kHz): LTC1264 DS
Dual 4th Order Notch and Bandpass (to 150kHz): LTC1264 DS

Output Buffer

Buffering the Filter Output: LTC1064-1 DS; LTC1064-2 DS
Output Buffer Eliminates any Clock Feedthrough: LTC1064-1 DS; LTC1064-2 DS

Output Offsets

LTC1060 Offsets: LTC1060 DS
Equivalent Input Offsets of LTC1061: LTC1061 DS
Table 4 Shows Output Offsets for Mode 1, 1b, 2 and 3: LTC1061 DS
Output DC Offsets, One 2nd Order Section: LTC1064 DS

FLASH MEMORY—See Digital Help Circuits

FLOW MEASUREMENT—See Signal Conditioning

FUNCTION GENERATOR

Pulse

1.5V Powered 350ps Rise Time Pulse Generator: AN45, Pg. 18; LT1073 DS

Ramp

Ramp Generator with Variable Reset Level: LF198 DS
Staircase Generator: LF198 DS

Tri-Wave

Precise Tri-Wave Generator: LT1018 DS

FUSE—ELECTRONIC—See Current-Sensing

GAS SENSOR—See Signal Conditioning

GROUND PLANES

Discussion

About Ground Planes: AN13, Pg. 29; AN47, Pg. 24

HEARTBEAT

Fetal

Life: AN45, Pg. 1

HELP

Linear Technology Corporation—Call Applications 408-432-1900

HEWLETT W. R.

Oscillator

"A New Type Resistance-Capacity Oscillator" M.S. Thesis, Stanford U. 1939: AN 5, Pg. 8; AN43, Pg. 29; AN43, Pg. 43

INDUCTANCE

DC-DC

Inductor Selection for Flyback Converters: AN29, Pg. 38

Equivalent

Generating Negative Output Impedance: LM134 DS

INSTRUMENTATION AMPLIFIER—See Amplifier

INTERFACE CIRCUITS

Coax

Coax Cable Driver/Receiver: LTC1045 DS

High Speed

High Speed Dual Line Driver: LT1015 DS

Level Translator

TTL/CMOS Logic Levels to ±5V Analog Switch Driver: DN20, Pg. 1

ECL to CMOS from Single +5V Supply: LTC1045 DS

ECL to CMOS/TTL Logic: LTC1045 DS

High Voltage CMOS (V_{CC} = 15V) to TTL/CMOS (V_{CC} = 5V): LTC1045 DS

Logic Ground Isolation: LTC1045 DS

TTL/CMOS Logic Levels to ± Analog Switch Driver: LTC1045 DS

Ribbon Cable

Flat Ribbon Cable Driver/Receiver: LTC1045 DS

RS232

Sharing a Receiver Line: LT1080 DS

New Developments in RS232 Interfaces: DN4, PG. 1

5V Powered RS232 Driver/Receiver: DN4, Pg. 2

Extending the Applications of 5V Powered RS232 Transceiver: DN14, Pg. 1

RS232 Receiver: DN20, Pg. 2

2500V Isolated 5-Driver/5-Receiver RS232 Transceiver: DN27, Pg. 1

Design Considerations for RS232 Interfaces: DN27, Pg. 1

Single Supply RS232 Interface for Bipolar A/D Converters: DN29, Pg. 1

Fast Turn On Transceiver with Automatic Shutdown Control: DN30, Pg. 1

RS232 Transcievers Withstand 10kV ESD: DN64, Pg. 1

Quad Low Power Line Driver: LT1030 DS; LT1032 DS

LT1080 Driving an LT1039: LT1039 DS

RS232 Compatible Shutdown Control Line: LT1039 DS

RS232 Driver/Reciever with Shutdown: LT1039 DS

Sharing a Transmitter Line: LT1039 DS; LT1080 DS

Transceiver: LT1039 DS; LT1080 DS

5V Powered RS232 Driver/Receiver with Shutdown: LT1080 DS

Operating with +5V and +12V Supplies: LT1130 DS; LT1180 DS

Paralleling Power Supply Generator with Common Storage Capacitors: LT1130 DS

RS232 Transceiver with Power Supply Generator: LT1130 DS

5V Powered RS232 Driver/Receiver with Shutdown and Small Capacitors: LT1180 DS

Keeping Alive One Receiver while in Shutdown: LT1237 DS; LT1330 DS; LT1331 DS

5V RS232 Transceiver with 3V Logic Interface: LT1330

3V Powered RS232 Driver/Receiver: LT1331 DS

RS232 Receiver: LTC1045 DS

RS485

Typical RS485 Network: DN39, Pg. 1; LTC485 DS

Differential Bus Transceiver: LTC485 DS

Quad, Low Power RS485 Driver: LTC486 DS; LTC487 DS

Differential Driver and Receiver Pair: LTC490 DS; LTC491 DS

SCSI

Active Termination for SCSI-2 Bus: AN52, Pg. 6; DN34, Pg. 2; LT1117 DS

SCSI Termination Power Protector: AN53, Pg. 16; LTC1153 DS; LTC1154 DS

SCSI Termination Power with Short Circuit Protection and Automatic Reset: LTC1155 DS

LAPTOP CIRCUITS

Flash Memory

All Surface Mount Flash Memory V_{PP} Generator: LT1109 DS

Switching Regulator

Cold Cathode Fluorescent Lamp (Back Light): AN45, Pg. 21; AN49, Pg. 2

LCD Display Contrast Power Supply: DN47, Pg. 2

Cold Cathode Fluorescent Lamp Power Supply: DN52, Pg. 2

LCD BIAS SUPPLY—See Regulator-Switching (Micropower)

LEVEL DETECTOR—See Signal Conditioning-Level

LEVEL SHIFT— See Comparator

LVDT—See Signal Conditioning-Distance

MEMORY

Discussion

A Primer on Flash Memory: AN31, Pg. 12

Preventing Memory Destruction: AN31, Pg. 14

EEPROM

EEPROM V_{PP} Pulse Generator: AN31, Pg. 5
EEPROM Pulse Generator: LT1013 DS

EPROMs

V_{PP} Generator for EPROMs—No Trim Required: LT1004 DS

Flash

Basic Flash Memory V_{PP} Programming Voltage Supply: AN31, Pg. 1
High Repetition Rate V_{PP} Programming Supply: AN31, Pg. 2
High Power, High Repetition Rate V_{PP} Pulse Generator: AN31, Pg. 3
All Surface Mount Flash Memory V_{PP} Generator: LT1109 DS

Save

Memory Save on Power Down: AN31, Pg. 8

METHANE DETECTOR— See Signal Conditioning

MICROPOWER

A-D

Micropower A-D (12-Bit, 300µs): AN23, Pg. 7
Micropower A-D (10-Bit, 100µs): AN23, Pg. 9

Comparator

Refrigerator Alarm: LT1017 DS

DC-DC

Low Quiescent Current Flyback Regulator (150µA, 6V-12V): AN29, Pg. 9; DN11, Pg. 2

Discussion

Some Guidelines for Micropower Design: AN23, Pg. 18
Sampling Techniques and Components for Micropower Circuits: AN23, Pg. 21
Parasitic Effects of Test Equipment on Micropower Circuits: AN23, Pg. 23

Instrumentation Amplifier

Precision, Micropower, Single Supply Instrumentation Amplifier: LT1101 DS
Micropower Single Supply Instrumentation Amplifier: LTC1047 DS

Op Amp

Low Power Chopper Stabilized Op Amp with Internal Capacitors (200µA): LTC1049 DS

Sample and Hold

Micropower Sample and Hold: AN23, Pg. 10; LT1006 DS

Strain Gauge

Sampled Strain Gauge Bridge Signal Conditioner: AN23, Pg. 3
Strobed Power Bridge Signal Conditioner: AN23, Pg. 4

Temperature Sensor

Platinum RTD Signal Conditioner with Curvature Correction (2°C-400°C): AN23, Pg. 1; LT1006 DS
Thermocouple Signal Conditioner with Cold Junction Compensation (0°C-60°C): AN23, Pg. 2; LT1006 DS
Thermistor Based Current Loop Signal Conditioner (0°C-100°C): AN23, Pg. 5
Wall Type Thermostat: AN23, Pg. 6
Freezer Alarm: AN23, Pg. 7
Micropower Cold Junction Compensation for Thermocouples: LT1004 DS
Micropower, Battery Operated, Remote Temperature Sensor: LT1101 DS
Ultra Low Power 50°F to 100°F Thermostat: LTC1041 DS

V-F

Micropower V-F Converter (10kHz): AN23, Pg. 11
Micropower V-F Converter (1MHz): AN23, Pg. 13; LT1006 DS
90µA Supply Current V-F: AN45, Pg. 15
Micropower V-F Converter (0V-5V to 100Hz-1MHz): DN38, Pg. 1; LTC201 DS
Low Power V-F Converter: LT1018 DS

Voltage Reference

Self-Buffered Micropower Reference: DN23, Pg. 1; LT1178 DS
Low Input Voltage Reference Driver: LM134 DS
Micropower 5V Reference: LM185 DS; LM134 DS
Micropower Voltage Reference: LT1004 DS

Voltage Regulator

Buck Switching Regulator (5.8V-10V to 5V): AN23, Pg. 15
Post Regulated Switching Regulator (6V-10V to 5V): AN23, Pg. 16
Micropower Pre-Regulated Linear Regulator: AN32, Pg. 8
Micropower Regulator with Comparator and Shutdown: LT1120 DS

MODELS

Macromodel

Questions and Answers on the Spice Macromodel Library: AN41
Using the LTC Op Amp Macromodels: AN 48
LT1014 Op Amp Spice Macromodel: DN12, Pg. 1
Spice Op Amp Macromodel for the LT1012: DN28, Pg. 1
LT1056 Macromodel: DN43, Pg. 2

MOTOR CONTROL

Driver

DC Motor Driver with Stall-Current Circuit Breaking: LTC1153 DS

Speed

Motor Speed Controller: AN1, Pg. 7; AN4, Pg. 6
Piezoelectric Fan Servo: AN4, Pg. 7
Motor Speed Controller, Tachless: AN11, Pg. 8
A Simple Motor Tachometer Servo Loop: AN25, Pg. 11
Motor Speed Controller Needs No Tachometer: LF198 DS
Proportional Motor Speed Controller: LT1005 DS; LT1035 DS
High Efficiency Motor Speed Controller: LT1011 DS
Motor Speed Controller, No Tachometer Required: LT1013 DS
Motor Speed Servo: LT1054 DS
10A Full Bridge Motor Control: LT1158 DS
High Efficiency 6-Cell Ni-Cad Protected Motor Drive: LT1158 DS
Potentiometer-Adjusted Open Loop Motor Speed Control: LT1158 DS
Motor Speed Controller: LTC1041 DS

Stepper Motor Driver

Power MOSFET Driver Low Power Consumption Stepper Motor Driver: LTC1045 DS
4-Phase Stepper Motor Driver with Short Circuit Protection: LTC1156 DS; LTC1255 DS

MURPHY'S LAW

Discussion

Understanding the Behavior of Inanimate Objects: AN47, Pg. 130

NATURE

Mother

Control of Circuits: AN47, Pg. 5

NOISE

Discussion—See Also Amplifier

Minimizing: AN9, Pg. 3
Noise Calculation in Op Amps: DN15, Pg. 1
Voltage Noise vs Current Noise: LT1028 DS

OP AMP—See Amplifier

OSCILLATORS

Crystal

Temperature Compensated Crystal Oscillator, TXCO: AN3, Pg. 15
Crystal Stabilized Relaxation Oscillator: AN12, Pg. 2; LT1011 DS
Gate Oscillators: AN12, Pg. 2
Crystal Oscillator (10MHz-25MHz): AN12, Pg. 3; AN 31, Pg. 11; LT1016 DS
Oscillator (1MHz-10MHz): AN12, Pg. 3; AN31, Pg. 11; LT1016 DS
Ovenized Oscillator: AN12, Pg. 3
Temperature Compensated Crystal Oscillator, TXCO: AN12, Pg. 4
Voltage Controlled Crystal Oscillator (VCXO): AN12, Pg. 5
1.5V Temperature Compensated Crystal Oscillator: (3.5MHz): AN15, Pg. 6
Low Frequency Crystal Oscillator Clock: AN31, Pg. 11
Quartz Stabililized, Low Distortion: AN45, Pg.12
Temperature Compensated, 1.5V Powered: AN45, Pg. 14
10MHz Quartz Stabilized Sine Wave Oscillator: AN47, Pg. 49
20MHz Quartz Stabilized Sine Wave Oscillator with Electronic AGC: AN47, Pg. 50
Temperature Compensated Crystal Oscillator: LT1013 DS
Low Distortion, Crystal Stabilized Oscillator: LT1057 DS
1.5V Powered Temperature Compensated Crystal Oscillator: LT1073 DS
3.58MHz Oscillator: LT1227 DS

Discussion

Quartz Crystal Oscillator: AN12, Pg. 8
Wien Bridge: AN43, Pg. 43

Half Sine Wave

A Half Sine Reference Generator: AN35, Pg. 28

Pulsed

Temperature Compensated Crystal Oscillator, TXCO: AN3, Pg. 15

Crystal Stabilized Relaxation Oscillator: AN12, Pg. 2; LT1011 DS; LT311A DS

Gate Oscillators: AN12, Pg. 2

Crystal Oscillator (10MHz-25MHz): AN 12, Pg. 3; LT1016 DS

Oscillator (1MHz-10MHz): AN12, Pg. 3; LT1016 DS

Ovenized Oscillator: AN12, Pg. 3

Temperature Compensated Crystal Oscillator, TXCO: AN12, Pg. 4

Reset Stabilized Oscillator: AN12, Pg. 6

Stable RC Oscillator: AN12, Pg. 7; LT1011 DS; LT1016 DS

1.5V Temperature Compensated Crystal Oscillator (3.5MHz): AN15, Pg. 6

Bridge Oscillator: AN43, Pg. 27

Low Frequency Square Wave Generator: LM101 DS

Temperature Compensated Crystal Oscillator: LT1013 DS

Phase Shift Oscillator: LT1032 DS

Single Supply Crystal Oscillator 10MHz-15MHz: LT1116 DS

Sine Wave

Low Distortion Sine Wave: AN5, Pg. 8

Voltage Controlled Sine Wave Oscillator: AN12, Pg. 5

Voltage Controlled Sine Wave Oscillator (1Hz-1MHz): AN13, Pg. 13

Sine Wave Output VCO (1Hz-100kHz): AN14, Pg. 10

Bridge Based Crystal Oscillator: AN43, Pg. 27

Common Mode Suppression for Quartz Oscillator Lowers Distortion: AN43, Pg. 28

Crystal Oscillator with Lamp Added for Gain Stabilization: AN43, Pg. 28

Multi-Range Wien Bridge Based Oscillator: AN43, Pg. 29

Wien Bridge Sine Wave Oscillator: AN43, Pg. 29; LT1221 DS; LT1225 DS

Wien Bridge with FET Stabililization: AN43, Pg. 30; AN43, Pg. 31

Wien Bridge Oscillator with Photocell Stabililization: AN43, Pg. 32

Wien Bridge with 3ppm Distortion: AN43, Pg. 33

10MHz Quartz Stablized Sine Wave Oscillator: AN47, Pg. 49

20MHz Quartz Stabilized Sine Wave Oscillator-Electronic AGC: AN47, Pg. 50

Varactor Tuned 1MHz-10MHz Wien Bridge Oscillator: AN47, Pg. 51

Wein Bridge Sine Wave Oscillator: LM101 DS

Ultra Pure Sine Wave Generator: LT1007 DS; LT1022 DS

Super Low Distortion Variable Sine Wave Oscillator: LT1028 DS

Low Distortion, Crystal Stabilized Oscillator: LT1057 DS

Ultra Low THD Oscillator (5ppm Distortion): LT1115 DS

Quartz Stabilized Oscillator with 9ppm Distortion: LT1122 DS

Synchronized

Synchronized Oscillator: AN12, Pg. 6

High Noise Immunity Line Synchronization Circuit: AN31, Pg. 12

V-F—See Converters

VCO

Voltage Controlled Crystal Oscillator (VCXO): AN12, Pg. 5

Voltage Controlled Sine Wave Oscillator (1Hz-1MHz): AN13, Pg. 13

Sine Wave Output Voltage to Frequency (1Hz-100kHz): AN14, Pg. 10; LT1055 DS

Oscillator VCO 1Hz-1MHz Sine Wave Output: AN47, Pg. 53

Voltage Controlled Crystal Oscillator: LT319A DS

OSCILLOSCOPE

Discussion

Evaluating Oscilloscope Overload Performance: AN10, Pg. 6

Considerations for High Speed Work: AN13, Pg. 8

Probes and Oscilloscopes: AN13, Pg. 27

Measuring Equipment Response: AN13, Pg. 30

About Oscilloscopes: AN47, Pg. 20

OTT PROCESS

Thermal

High Thermal Resistance Die Attach: AN22, Pg. 4

PEAK DETECTOR

Fast

Closed Loop Peak Detector: DN61, Pg. 1
Open Loop High Speed Peak Detector: DN61, Pg. 1
Fast Pulse Detector: DN61, Pg. 2

Negative

Negative Peak Detector: LT1011 DS; LT311A DS

Positive

Positive Peak Detector: LT1011 DS; LT311A DS

PERMIT

FCC

FCC Licensing for AM Broadcasting Station: AN47, Pg. 123

PHASE LOCK LOOPS

Discussion

Unique Applications for the LTC1062 Lowpass Filter: AN24, Pg. 1

Filter—Switched Capacitor

DC Accurate Filter Eases PLL Design: DN7, Pg. 1

PHILBRICK, GEORGE A.

Analog

Analog Functions: AN35, Pg. 28

PHOTODIODE—See Signal Conditioning-Photodiode

PLATINUM RTD—See Signal Conditioning-Temperature

POWER ACTUATORS—See Driver

POWER MOSFET DRIVER

POWER SUPPLY—See Regulator-Voltage

POWER SUPPLY SUPERVISORY CIRCUITS—See Digital Help Circuits

PREAMPLIFIER—See Amplifier

PRESSURE MEASUREMENT—See Signal Conditioning

PROBES

Current

Techniques and Equipment for Current Measurement: AN35, Pg. 24

Discussion

Probes and Probing Techniques: AN47, Pg. 16
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Fast

Ultra Fast High Impedance: AN47, Pg. 96

High Impedance

High Impedance Buffer: AN23, Pg. 24

Oscilloscope

About Probes and Oscilloscope: AN13, Pg. 27

PROGRAMMING

C Language

A "C" Cruise through Data Acquisition: AN34, Pg. 1

CAD

Contact Factory for Your Copy of FilterCAD
Contact Factory for Your Copy of SwitcherCAD

Don't Be Silly

PULSE GENERATOR

Fast Rise

Avalanche Pulse Generator: AN47, Pg. 93; AN45, Pg. 18

RADIO STATION

AM

A Complete AM Radio Station: AN47, Pg. 52

REFERENCE-AC

Half Sine Wave

A Half Sine Reference Generator: AN35, Pg. 28

REFERENCE—CURRENT—See Also Current

Sink

Precision Current Sink: LT1001 DS

Source

Precision Current Source: LT1001 DS
Precision Current Source (1μA): LT1019 DS

REFERENCE—VOLTAGE

2-Terminal

1.235V Micropower Reference: AN42, Pg. 10; LT1004 DS; LT1034 DS
1.25V Reference: AN42, Pg. 10; LT1004 DS

1.24V Output, Micropower, Current Boosted Reference (100mA): AN42, Pg. 11
1.2V Output, Micropower Reference with Wide Input Voltage Range: AN42, Pg. 11
2.5V Reference: AN42, Pg. 11; LT1004 DS; LM185 DS
2.5V Output, Micropower Reference with Wide Input Voltage Range: AN44, Pg. 11
10V Buffered Reference Using a Single Supply: LM129 DS; OP07 DS
6.9V Reference: LM129 DS
Low Noise Reference: LT1004 DS

3-Terminal

2.5V Reference, ±5% Trim Range: AN42, Pg. 5; LT1009 DS; LM136 DS
Trimming Output to 5.120V: AN42, Pg. 6; LT1029 DS
Wide Supply Range, Adjustable Reference: AN42, Pg. 11; LT1009 DS
Wide Supply Range: LM136 DS
Low Noise 2.5V Buffered Reference: LT1009 DS; LM136 DS
Switchable ±1.25V Bipolar Reference: LT1009 DS; LM136 DS
Split ±2.5V References: LT1029 DS

Current Boost

Precision High Current Reference (1.5A): AN2, Pg. 7
1.24V Output, Micropower, Current Boosted Reference (100mA): AN42, Pg. 11
Boosted Output Current with No Current Limit: AN42, Pg. 12; LT1021 DS; LT1031 DS
Handling Higher Load Currents: AN42, Pg. 12; LT1019 DS; LT1027 DS
Output Current Boost with Current Limit: LT1019 DS; LT1021 DS; LT1031 DS

Discussion

Heat Mode Reduces Temperature Drift to <2ppm/°C: LT1019 DS
Output Trimming: LT1019 DS
Effects of Air Movement on Low Frequency Noise: LT1021 DS
Trimming Output Voltage: LT1021 DS
Application Hints for Ultra Precision Reference: LTZ1000 DS

High Voltage

Ultra Precision Variable Voltage Reference (7.45ppm/°C): AN6, Pg. 6

Low Noise

Low Noise Reference: LT1004 DS
2-Pole Lowpass Filtered Reference: LT1021 DS; LT1031 DS
Low Noise Reference: LTZ1000 DS

Micropower

1.235V Micropower Reference: AN42, Pg. 10; LT1004 DS
2.5V Micropower Reference: AN42, Pg. 11; LT1004 DS
Self-Buffered Micropower Reference: AN42, Pg. 11; DN23, Pg. 1; LT1178 DS
Micropower 5V Reference: LM185 DS; LM134 DS
Micropower 5V Reference: LT1004 DS

Negative

Ultra Precision Inverter: AN3, Pg. 14
Basic Negative Reference: AN42, Pg. 9; LT1021 DS; LT1031 DS
Negative Series Reference: AN42, Pg. 9; LT1019 DS; LT1021 DS
Negative Shunt Reference Driven by Current Source: AN42, Pg. 9; LT1021 DS; LT1031 DS
Negative Voltage Reference: AN42, Pg. 16; LTZ1000 DS
Negative 10V Reference for CMOS DAC: LT1019 DS; AD580 DS
CMOS DAC with Low Drift Full-Scale Trimming: LT1021 DS

Precision

10V Buffered Reference: AN42, Pg. 17; LM199 DS
6.95V Reference: AN42, Pg. 19; LM199 DS
Portable Calibrator: LM199 DS
Standard Cell Replacement: LM199 DS
Precision ±10V Reference: LT1002 DS
Buffered Reference for A to D Converters: LT1012 DS
Heat Mode Reduces Temperature Drift to <2ppm/°C: LT1019 DS
Operating 5V Reference from 5V Supply: LT1021 DS
Precision DAC Reference with System TC Trim: LT1021 DS; LT1031 DS
Restricted Trim Range for Improved Resolution: LT1021 DS; LT1019 DS

Shunt

- 2.5V Reference (LT1431): AN42, Pg. 6; LT1431
- 2.5V Reference (LT1431Z): AN42, Pg. 6; LT1431 DS
- 5V Reference: AN42, Pg. 6; LT1431 DS
- Programmable Reference with Adjustable Current Limit: AN42, Pg. 6; LT1431 DS

Standard Cell

- Standard Grade Variable Voltage Reference: AN9, Pg. 5
- Saturated Standard Cell Amplifier: LT1008 DS; LT1012 DS; LT1097 DS

Ultra Precision

- Ultra Precision Variable Voltage Reference (7.45ppm/°C): AN6, Pg. 6; LT1001 DS; LT1002 DS
- 7V Positive Reference: AN42, Pg. 16; LTZ1000 DS
- Adjusting Temperature Coefficient in Unstabililized Application: LTZ1000 DS
- Averaging Reference Voltages for Lower Noise and Better Stability: LTZ1000 DS
- Low Noise Reference: LTZ1000 DS

REGULATOR—CURRENT—See Also Current

REGULATOR—SWITCHING

Backlight

- Cold Cathode Fluorescent Lamp (CCFL) Power Supply: AN45, Pg. 21; AN49, Pg. 2; AN51, Pg. 6
- Two-Tube CCFL: AN49, Pg. 4
- Low Power CCFL Power Supply: AN49, Pg. 5
- "Hot" Cathode Fluorescent Lamps: AN49, Pg. 7
- Backlight Efficiency Measurements: AN49, Pg. 10
- The Thermometer Effect: AN49, Pg. 15

Boost

- Single Cell Up Converter (1.5V to 5V): AN 8, Pg. 8; AN30, Pg. 8
- Up Converter (6V to 15V): AN8, Pg. 9; LT1013 DS; AN30, Pg. 7
- Single Inductor, Dual Polarity Regulator (6V to ±15V): AN8, Pg. 10; LT1013 DS; AN30, Pg. 9
- Boost Converter (1.5V to 5V): AN15, Pg. 7; AN30, Pg. 8; LT1018 DS
- Boost Converter (5V to 12V): AN19, Pg. 13; AN30, Pg. 5; AN46, Pg. 1
- Voltage Boosted Boost Converter (15V to 100V): AN19, Pg. 37; AN30, Pg. 5; LT1070 DS
- Negative Boost Regulator (–15V to –28V): AN19, Pg. 38 AN30, Pg. 5; LT1070 DS
- Current Boosted Boost Converter (16V-24V to 28V): AN19, Pg. 40; AN30, Pg. 5; LT1070 DS
- Low Noise Converter (5V to ±15V): AN29, Pg. 2; AN30, Pg. 11
- Ultra Low Noise Sine Wave Drive (5V to ±15V): AN29, Pg. 4; AN30, Pg. 12
- Single Inductor Regulated Converter (5V to ±15V): AN29, Pg. 6; AN30, Pg. 10
- Low Quiescent Current Flyback Regulator (150µA, 6V to 12V): AN29, Pg. 9; DN11, Pg. 2; AN30, Pg. 6
- 200mA Output Converter (1.5V to 5V): AN29, Pg. 15; AN30, Pg. 7
- Single Inductor Dual Output Converter (5V to ±15V): AN30, Pg. 13
- Negative Boost Converter (–5V to –15V to –15V): AN44, Pg. 33; LT1074 DS
- 90V DC-DC: AN45, Pg. 19
- Basic Flash EEPROM V_{PP} Pulse Generator (5V to 12.75V or 12.00V): DN17, Pg. 2; AN30, Pg. 43
- High Repetition Rate V_{PP} Pulse Generator (5V to 12.75V or 12.00V): DN17, Pg. 2; AN30, Pg. 43
- Low Voltage Circuit Provides Constant Output Voltage as Battery Discharges: DN41
- Up Converter (1.5V to 5V): LM10 DS; AN30, Pg. 8
- Regulated Up Converter (5V to 10V): LT1018 DS; AN30, Pg. 8
- Boost Converter (15V to 90V): LT1082 DS
- 100kHz Boost Converter (5V to 12V): LT1172 DS

Buck

- Linear Regulator with Switching Pre-Regulator (28V to Adj.): AN2, Pg. 3; AN30, Pg. 31
- High Current Low Dissipation Pre-Regulated Linear Regulator (0V-35V, 0A-10A): AN2, Pg. 4; AN30, Pg. 33; LT1083 DS
- Low Power Switching Regulator (9V to 5V): AN8, Pg. 4; AN30, Pg. 17; LT1013 DS
- Switching Pre-Regulator Linear Regulator (9V to 5V): AN8, Pg. 5; AN30, Pg. 17; LT1013 DS
- Negative Buck Converter (–20V to –5.2V): AN19, Pg. 17; AN30, Pg. 16; LT1070 DS
- Positive Buck Converter: AN19, Pg. 23; AN30, Pg. 15; LT1070 DS

Micropower Switching Regulator (5.8V-10V to 5V): AN23, Pg. 15; AN 30, Pg. 17
Micropower Post Regulated Switching Regulator (6V-10V to 5V): AN23, Pg. 16; AN30, Pg. 32
Low Quiescent Current Buck Converter (150μA, 8V-16V to 5V): AN29, Pg. 12; AN30, Pg. 14
90% Efficient Positive Buck with Synchronous Switch (9.5V-14.5V to 5V): AN29, Pg. 18; AN30, Pg. 16
Positive Buck Converter (15V-35V to 5V): AN29, Pg. 23; AN30, Pg. 13
High Power Linear Regulator with Switching Pre-Regulator: AN29, Pg. 25; AN 30, Pg. 30; LT1083 DS
Positive Buck Converter (7V-15V to 5V, 250mA): AN30, Pg. 15
Buck Regulator, 1A (8V-30V to 5V): AN30, Pg. 18; LT3524 DS
Low Dissipation Regulator (10V-20V to 5V): AN30, Pg. 32; LT1035 DS; LT1036 DS
Switching Pre-Regulated for Wide Input Voltage Range (7.5V-30V to 5V): AN30, Pg. 33; LT1020 DS
High Current Positive Buck with Bootstrapped NMOS Gate Drive (15V-35V to 5V): AN30, Pg. 44
A Practical Step-Down Regulator Using the LT1074 (10V-60V to 5V): AN35, Pg. 2; AN44, Pg. 18; AN46, Pg. 3
Coupled Inductor Provides Positive and Negative Outputs (28V to 15V, –5V): AN35, Pg. 3
"Current Boosted" Step-Down Regulator (20V-30V to 5V): AN35, Pg. 5; AN44, Pg. 25; LT1074 DS
A Simple Loop Reduces Quiescent Current to 150μA (12V to 5V): AN35, Pg. 7
Adjustable Linear Post-Regulator Maintains Efficiency (35V to 1.2V-28V): AN35, Pg. 7
Gives Better Regulation while Maintaining 150μA Quiescent Current (12V to 5V): AN35, Pg. 8
High Efficiency Buck Converter with Active Catch Diode: AN44, Pg. 15
LT1070 Floating Input Step-Down Switching Regulator: AN46, Pg. 5
LT1070 High Efficiency Buck Switching Regulator: AN46, Pg. 7
High Efficiency 3.3V Regulator with Burst Mode™ Operation: AN51, Pg. 3
High Efficiency 5V Regulator with Burst Mode™ Operation: AN51, Pg. 3; LT1432 DS
LT1158 (24V to 5V/10A) Buck Converter: AN52, Pg. 9
Floating Input Low Saturation Loss Buck Regulator: DN21, Pg. 2
No Design Switching Regulator: DN48, Pg. 2; DN53, Pg. 2
5V High Current Step-Down (30V-60V to 5.1V/12A): DN59, Pg. 1
5V High Current Step-Down (10V-60V to 5V/10A): DN59, Pg. 2
Basic Positive Buck Converter: LT1074 DS
Tapped-Inductor Buck Converter: LT1074 DS
High Efficiency Buck Converter: LT1270 DS; AN46 Pg. 7
12V to 5V Buck Converter with Foldback Current Limit: LT1431 DS

Buck-Boost

Negative to Positive Buck-Boost Converter (–40V to –60V to 5V): AN19, Pg. 20; AN25, Pg. 4; AN29, Pg. 21
Positive to Negative Buck-Boost Converter (10V-30V to –12V): AN19, Pg. 39; AN30, Pg. 19; LT1070 DS
Positive Buck-Boost Converter (15V-35V to 28V): AN29, Pg. 24; AN30, Pg. 18
Negative Output Step-Down Regulator (12V to –5V): AN35, Pg. 4
A (Better) Negative Output Step-Down Regulator (–5V Output): AN35, Pg. 5; AN46, Pg. 9; LT1074 DS
Positive to Negative Converter (4.5V-40V to –5V): AN44, Pg. 28; AN46, Pg. 9; LT1074 DS
LT1070 High Efficiency Positive to Negative Switching Regulator: AN46, Pg. 10
No Design Switching Regulator: DN49, Pg. 2
Positive to Negative Converter: LT1074 DS
"5V to 5V" Step-Up or Step-Down Converter: LT1173 DS

Discussion

LT1070 Operation: AN19, Pg. 3; AN25, Pg. 13; AN29, Pg. 44
Basic Switching Regulator Topologies: AN19, Pg. 8
Input and Output Capacitors: AN19, Pg. 16; AN19, Pg. 55
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Switching Diodes: AN19, Pg. 50; AN25, Pg. 18
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Foldback Current Limiting: AN19, Pg. 51
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Basic Step-Down Circuit: AN35, Pg. 1
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Inductor Selection-Alternate Method: AN35, Pg. 22; AN44, Pg. 34
Techniques and Equipment for Current Measurement: AN35, Pg. 24
Optimizing Switching Regulators for Efficiency: AN35, Pg. 26
The Magnetics Issue: AN35, Pg. 30; AN44, Pg. 34
Oscilloscope Techniques: AN44, Pg. 44
Thermal Considerations for Aluminum Electrolytic Filter Capacitors: AN46, Pg. 15
Measuring RMS Current in Switching Regulator Filter Capacitors: AN46, Pg. 19
Bipolar Power Switch Conduction Losses: AN46, Pg. 22
Diode Conduction Losses: AN46, Pg. 25
Inductor Selection: DN8, Pg. 1

Flyback

Flyback Converter (20V-30V to 5V): AN19, Pg. 26; AN29, Pg. 20; AN30, Pg. 20
Totally Isolated Converter (5V to ±15V): AN19, Pg. 30; AN30, Pg. 21; LT1070 DS
Positive Current Boosted Buck Converter (28V to 5V): AN19, Pg. 34; AN30, Pg. 22; LT1070 DS
Negative Current Boosted Buck Converter: AN19, Pg. 36; AN30, Pg. 23; LT1070 DS
Negative Input-Negative Output Flyback Converter: AN19, Pg. 36; AN30, Pg. 23; LT1070 DS
Positive Input-Negative Output Flyback Converter: AN19, Pg. 37; AN30, Pg. 24; LT1070 DS
Fully Isolated Regulator (–40V to –60V to 5V): AN25, Pg. 6; AN30, Pg. 24
Low Iq, Isolated (5V to ±15V): AN29, Pg. 7; AN30, Pg. 25
Transformer Coupled Low Quiescent Current Converter: (150μA, 12V to 5V, ±15): AN29, Pg. 13; AN30, Pg. 42; DN18, Pg. 2
800μA Output Converter (1.5V to 5V): AN29, Pg. 14; AN30, Pg. 26
High Efficient Flux Sensed Isolated Converter (12V to 5V): AN29, Pg. 19; AN30, Pg. 22
Input Positive, Output Negative Flyback Converter (3.5V-35V to –5V): AN29, Pg. 22; AN30, Pg. 21
Multi-Output Flyback Converter (12V to 5V, ±12V): AN30, Pg. 42; DN18, Pg. 1

Forward

Forward Converter (20V-30V to 5V): AN19, Pg. 41; AN30, Pg. 27; LT1070 DS
Push-Pull Forward Converter: UC1846 DS

Help

Who Are You Going to Call?: AN35, Pg. 32

High Voltage

Non-Isolated Converter (15V to 1kV): AN29, Pg. 26; AN30, Pg. 27
Isolated Output Converter (15V to 1kV): AN29, Pg. 27; AN30, Pg. 28
Converter with 20,000V Isolation (15V to 10V): AN29, Pg. 28; AN30, Pg. 28
High Voltage Power Supply (8V-15V to 330V): AN39, Pg. 1
Parasitic Capacitance Effects in Step-Up Transformer Design: AN39, Pg. 1

High Voltage, Variable

LT1074 Permits High Voltage Output (28V to 0V-500V): AN35, Pg. 12

Isolated

Totally Isolated Converter (5V to ±15V): AN19, Pg. 30; AN30, Pg. 21; LT1070 DS

Fully Isolated Regulator (–40V to –60V to 5V): AN25, Pg. 6; AN30, Pg. 24
Low Iq, Isolated (5V to ±15V): AN29, Pg. 7; AN30, Pg. 25
High Efficient Flux Sensed Isolated Converter (12V to 5V): AN29, Pg. 19; AN30, Pg. 22
Isolated 5V to ±15V Flyback Converter: LT1431 DS

Laptop
Cold Cathode Fluourescent Lamp (Backlight): AN45, Pg. 21; AN49, Pg. 2; AN51, Pg. 6
LCD Display Contrast Power Supply: AN49, Pg. 6; DN47, Pg. 2
Inductor and Switch Capacitor Technique Provide Bipolar Output: DN47, Pg. 1
Cold Cathode Fluorescent Lamp Power Supply: DN52, Pg. 2

Laser
Laser Power Supply: AN49, Pg. 13

LCD Bias
LCD Bias Currents: AN49, Pg. 6; AN51, Pg. 10

Local Area Network
Isolated Power Supply for Local Area Networks: DN31, Pg. 1

Low Power
Battery Splitter: AN8, Pg. 2; AN30, Pg. 38; LTC1044 DS
Low Power Switching Regulator (9V to 5V): AN 8, Pg. 4; AN30, Pg. 17; LT1013 DS
Switching Pre-Regulated Linear Regulator (9V to 5V): AN8, Pg. 5; AN30, Pg. 31; LT1013 DS
Regulated Voltage Up Converter: AN8, Pg. 7; AN30, Pg. 39; LTC1044 DS
Single Cell Up Converter (1.5V to 5V): AN8, Pg. 8; AN30, Pg. 8
Up Converter (6V to 15V): AN 8, Pg. 9; AN30, Pg. 7; LT1013 DS
Boost Converter (1.5V to 5V): AN15, Pg. 7; AN30, Pg. 8; LT1018 DS
Micropower Switching Regulator (5.8V-10V to 5V): AN23, Pg. 15; AN30, Pg. 17
Micropower Post Regulated Switching Regulator (6V-10V to 5V): AN23, Pg. 16; AN30, Pg. 32
Low Quiescent Current Flyback Regulator (150µA, 6V to 12V, 2A): AN29, Pg. 9; AN30, Pg. 6; DN11, Pg. 2
Low Quiescent Current Buck Converter (8V-16V to 5V): AN29, Pg. 12; AN30, Pg. 14
Transformer Coupled Low Quiescent Current Converter (12V to 5V, ±15V): AN29, Pg. 13; AN30, Pg. 20; DN18, Pg. 2
800µA Output Converter (1.5V to 5V): AN29, Pg. 14; AN30, Pg. 26
200mA Output Converter (1.5V to 5V): AN29, Pg. 15; AN30, Pg. 7
Regulated Up Converter (5V to 10V): AN30, Pg. 8; LT1018 DS
Up Converter (1.5V to 5V): AN30, Pg. 8; LM10 DS
Generating CMOS Logic Supply from Two Mercury Batteries (2.4V to 4.8V): AN30, Pg. 38; LTC1044 DS
A Simple Loop Reduces Quiescent Current to 150µA (12V to 5V): AN35, Pg. 7
Better Regulation while Maintaining 150µA Quiescent Current (12V to 5V): AN35, Pg. 8

Multi-Output
Single Inductor, Dual Polarity Regulator (6V to ±15V): AN8, Pg. 10; AN30, Pg. 9; LT1013 DS
Totally Isolated Converter (5V to ±15V): AN19, Pg. 30; AN30, Pg. 21; LT1070 DS
Low Noise (5V to ±15V): AN29, Pg. 2; AN30, Pg. 11
Ultra Low Noise Sine Wave Drive Converter(5V to ±15V): AN29, Pg. 4; AN30, Pg. 12
Single Inductor Regulated Converter (5V to ±15V): AN29, Pg. 6; AN30, Pg. 10
Low Iq, Isolated (5V to ±15V): AN29, Pg. 7; AN30, Pg. 25
Multi-Output, Transformer Coupled Low Quiescent Current Converter: AN29, Pg. 13; AN30, Pg. 42; DN18, Pg. 2
Transformer Coupled Low Quiescent Current Converter (150µA, 12V to 5V, ±1): AN29, Pg. 13; AN30, Pg. 42; DN18, Pg. 2
High Current Switched Capacitor Converter (6V to ±5V): AN29, Pg. 29; AN30, Pg. 41
Switched Capacitor Converter (5V to ±12V): AN29, Pg. 30; AN30, Pg. 35; LT1054 DS
Switched Capacitor Based (6V to ±7V): AN29, Pg. 31; AN30, Pg. 40
Switched Capacitor Charge Pump Based Voltage Multiplier: AN29, Pg. 31; AN30, Pg. 36
Single Inductor, Dual Output Converter (5V to ±15V): AN30, Pg. 13
Dual Pre-Regulated Supply (90V$_{AC}$-130V$_{AC}$ to ±12V): AN30, Pg. 30; LT1086 DS

Dual Output Voltage Doubler: AN30, Pg. 35; LT1054 DS
Dual Output Switch Capacitor Voltage Generator: AN30, Pg. 39; LT1026 DS
Voltage Multiplier (±5V to ±15V): AN30, Pg. 41; LT1032 DS
Multi-Output Flyback Converter (12V to 5V, ±12V): AN30, Pg. 42; DN18, Pg. 1
Coupled Inductor Provides Positive and Negative Outputs (28V to 15V, –5V): AN35, Pg. 3
Inductor and Switch Capacitor Techniques Provide Bipolar Output: DN47, Pg. 1

Offline

100W Offline Switching Regulator (5V at 20A): AN 25, Pg. 8; AN30, Pg. 29
No Design Offline Power Supply: DN62, Pg. 2
Fully Isolated Flyback 100KHz, 50W Converter: LT1103/LT1105 DS
300kHz Offline Power Supply: LT1241 DS

Pre-Regulator

Linear Regulator with Switching Pre-Regulator (28V to Adj.): AN 2, Pg. 3; AN30, Pg. 31
High Current Low Dissipation Pre-Regulated Linear Regulator (0V-35V, 0A-10A): AN2, Pg. 4; AN30, Pg. 33; LT1083 DS
Switching Pre-regulated Linear Regulator (9V to 5V): AN8, Pg. 5; AN30, Pg. 31; LT1013 DS
Micropower Post Regulated Switching Regulator (6V-10V to 5V): AN23, Pg. 16; AN30, Pg. 32
High Power Linear Regulator with Switching Pre-Regulator: AN29, Pg. 25; AN30, Pg. 30; LT1083 DS
Dual Pre-Regulated Supply (90V_{AC}-130V_{AC} to ±12V): AN30, Pg. 30; LT1086 DS
Low Dissipation Regulator (10V-20V to 5V): AN30, Pg. 32; LT1035 DS; LT1036 DS
Switching Pre-Regulator for Wide Input Voltage Range (7.5V-30V to 5V): AN30, Pg. 33; LT1020 DS
SCR Pre-Regulator (90V_{AC}-140V_{AC} to 15V): AN32, Pg. 3
Pre-Regulated Low Dropout Regulator (7V-20V to 5V): AN32, Pg. 4
Ultra-Low Dropout Linear Regulator with Pre-Regulator: AN32, Pg. 7
Micropower Pre-Regulated Linear Regulator (6V-10V to 5V): AN32, Pg. 8
Linear Post-Regulator Improves Noise and Transient Response (5V Output): AN35, Pg. 6
Adjustable Linear Post-Regulator Maintains Efficiency (35V to 1.2V-28V): AN35, Pg. 7

Step-Down—See Buck

Step-Up—See Boost and Flyback

Switched Capacitor

High Power Switched Capacitor Voltage Converter (12V to 5V): AN3, Pg. 16; AN8, Pg. 5; AN29, Pg. 32
Battery Splitter (9V to ±4.5V): AN8, Pg. 2; AN30, Pg. 38; LTC1046 DS
Regulated Negative Voltage Converter: AN8, Pg. 2; AN30, Pg. 39; LTC1046 DS
Voltage Doubler: AN8, Pg. 6; AN30, Pg. 38
Regulated Voltage Up Converter (3V to 5V): AN8, Pg. 7; AN30, Pg. 39; LTC1044 DS
–V_{IN} to +V_{OUT} Converter: AN29, Pg. 29; AN30, Pg. 34
High Current Switched Capacitor Converter (6V to ±5V): AN29, Pg. 29; AN30, Pg. 41
Positive Doubler: AN29, Pg. 30; AN30, Pg. 34; LT1054 DS
Switched Capacitor Converter (5V to ±12V): AN29, Pg. 30; AN30, Pg. 35; LT1054 DS
Switched Capacitor Based Converter (6V to ±7V): AN29, Pg. 31; AN30, Pg. 40
Switched Capacitor Charge Pump Based Voltage Multiplier (5V to ±12V): AN29, Pg. 31; AN30, Pg. 36
Basic Voltage Inverter: AN30, Pg. 34; LT1054 DS
Basic Voltage Inverter/Regulator: AN30, Pg. 34; LT1054 DS
Dual Output Voltage Doubler: AN30, Pg. 35; LT1054 DS
Regulated Negative Doubler (100mA): AN30, Pg. 35; LT1054 DS
Regulating 200mA Converter (12V to –5V): AN30, Pg. 36; LT1054 DS
Switched Capacitor Regulator (3.5V to 5V: AN30, Pg. 36; LT1054 DS
Digitally Programmable Negative Supply: AN30, Pg. 37; LT1054 DS
Negative Doubler with Regulator: AN30, Pg. 37; LT1054 DS
Negative Voltage Converter: AN30, Pg. 37; LTC1044 DS; LTC1046 DS
Positive Doubler with Regulation: AN30, Pg. 37; LT1054 DS
Voltage Doubler: AN30, Pg. 37; LTC1044 DS
Paralleling for Lower Output Resistance: AN30, Pg. 38; LTC1044 DS

Stacking for Higher Voltage: AN30, Pg. 38; LTC1044 DS
Dual Output Switched Capacitor Voltage Generator: AN30, Pg. 39; LT1026 DS
Voltage Tripler/Quadrupler: AN30, Pg. 39; LTC1044 DS
Charge Pump Negative Voltage Generator: AN30, Pg. 41; LT1020 DS
Charge Pump Voltage Doubler: AN30, Pg. 41; LT1020 DS
Voltage Multiplier (±5V to ±15V): AN30, Pg. 41; LT1032 DS
Negative Voltage Doubler: AN30, Pg. 43; LT1054 DS
4.5V-15V Input, Voltage Doubler Using the LTC203: DN38, Pg. 2; LTC203 DS
Paralleling for 100mA Load Current: LTC1046 DS
Micropower, ±4.5V to ±15V, Voltage Inverter Using the LTC203: LTC203 DS

Telecom

Negative to Positive Buck-Boost Converter (–40V to –60V to 5V): AN25, Pg. 4; AN29, Pg. 21; LT1082 DS
Fully Isolated Regulator (–40V to –60V to 5V): AN25, Pg. 6; AN30, Pg. 24
Totally Isolated Converter: LT1082 DS

Ultra High Efficiency

LTC1148 (2V-5V to 5V/1A) Boost Converter: AN54, Pg. 21
LTC1147 (4V-14V to 3.3V/1A) Buck Converter—Surface Mount: AN54, Pg. 12
LTC1147 (5V-14V to 5V/1A) Buck Converter—Surface Mount: AN54, Pg. 11
LTC1148 (10V-14V to 5V/10A) High Current Buck Converter: AN54, Pg. 13
LTC1148 (30V-75V to 24V/3A) High Voltage Buck Converter: AN54, Pg. 17
LTC1148 (4V-10V to –5V/1A) Positive to Negative Converter: AN54, Pg. 20
LTC1148 (4V-14V to +5V/0.5A, –5V/0.5A) Split Supply Converter: AN54, Pg. 19
LTC1148 (4V-14V to 3.3V/1A) Buck Converter—Surface Mount: AN54, Pg. 6
LTC1148 (4V-14V to 3.3V/2A) Buck Converter—Surface Mount: AN54, Pg. 7
LTC1148 (4V-14V to 5V/1A) Buck-Boost Converter: AN54, Pg. 18
LTC1148 (5V-14V to 5V/1A) Buck Converter—Surface Mount: AN54, Pg. 3
LTC1148 (5V-14V to 5V/2A) Buck Converter—Surface Mount: AN54, Pg. 4
LTC1148 (5V-14V to 5V/2A) High Frequency Buck Converter—Surface Mount: AN54, Pg. 5
LTC1149 (10V-48V to 3.3V/2A) High Voltage Buck Converter: AN54, Pg. 10
LTC1149 (10V-48V to 5V/2A) High Voltage Buck Converter: AN54, Pg. 8
LTC1149 (10V-48V to 5V/2A) High Voltage Buck Converter with Large P-Channel and N-Channel MOSFETs: AN54, Pg. 9
LTC1149 (12V-48V to 5V/10A) High Current, High Voltage Buck Converter: AN54, Pg. 15
LTC1149 (12V-36V to 5V/5A) High Current, High Voltage Buck Converter: AN54, Pg. 14
LTC1149 (32V-48V to 24V/10A) High Current, High Voltage Buck Converter: AN54, Pg. 16
High Efficiency Synchronous Buck (5.5V-13V to 5V/2A): DN68, Pg. 1
High Current, High Efficiency Synchronous Buck (12V-36V to 5V/5A): DN68, Pg. 2

REGULATOR—SWITCHING (MICROPOWER)

Backlight

Micropower CCFL Driver Delivers up to 1mA: AN51, Pg. 16

Boost

Two "AA" Cells to 5V Deliver 150mA: AN51, Pg. 13; LT1107 DS; LT1108 DS
Main Logic Converter with Backup Converter: AN51, Pg. 14
Two "AA" Cells to 6V/550mA: AN52, Pg. 7
Two "AA" Cell to 5V Step-Up Converter Delivers 150mA: DN52, Pg. 1
3V to 12V Step-Up Converter: LT1073 DS
3V to 15V Step-Up Converter: LT1073 DS
3V to 5V Step-Up Converter: LT1073 DS; LT1173 DS; LT1110 DS
3V to 5V/100mA Step-Up Converter with Under Voltage Lockout: LT1073 DS
3V to 6V at 1A Step-Up Converter: LT1073 DS
5V to 12V Step-Up Converter: LT1073 DS
5V to 15V Step-Up Converter: LT1073 DS
3V to 5V Converter: LT1109 DS

2V to 5V/300mA Step-Up Converter with Under Voltage Lockout: LT1173 DS
Step-Up Converter (5V to 12V): LT1173 DS

Buck
9V to 5V Reduced Noise Step-Down Converter: LT1073 DS
9V to 5V Step-Down Converter: LT1073 DS; LT1173 DS; LT1111 DS
9V to 5V Step-Down Converter: LT1173 DS
High Power, Low Quiescent Current Step-Down Converter: LT1173 DS; LT1111 DS

Buck-Boost
DC to DC Converter Generates –24V from 3V or 5V: DN52, Pg. 1
9V to 3V Step-Down Converter: LT1073 DS
Positive to Negative Converter: LT1073 DS; +5V to –5V/75mA; LT1173 DS; LT1111 DS
Positive to Negative Converter (5V to –5V): LT1173 DS
Voltage Controlled Positive to Negative Converter: LT1173 DS; LT1111 DS

Digital System Support
Memory Backup Supply: LT1073 DS

Laser
1.5V Powered Laser Diode Driver: AN52, Pg. 12; LT1110 DS

LCD Bias
LCD Bias Generator Delivers –24V at 10mA: AN51, Pg. 19; LT1173 DS; LT1111 DS

Multi-Output
1.5V to 10V/3mA, 5V/3mA Dual Output Step-Up Converter: LT1110 DS

Single Cell
1.5V to 12V Step-Up Converter: LT1073 DS
1.5V to 3V Step-Up Converter: LT1073 DS
1.5V to 5V Bootstrapped Step-Up Converter: LT1073 DS
1.5V to 5V Low Noise Step-Up Converter: LT1073 DS
1.5V to 5V Step-Up Converter with Logic Shutdown: LT1073 DS
1.5V to 5V Step-Up Converter with Low Battery Detector: LT1073 DS
1.5V to 5V Very Low Noise Step-Up Converter: LT1073 DS
1.5V to 9V Step-Up Converter: LT1073 DS
Single Cell to 5V Converter: LT1073 DS

Telecom
Telecom Supply: LT1173 DS

REGULATOR—VOLTAGE

Additional Feature Circuits
Remote Sensing: AN2, Pg. 8; LT117 DS; LT138 DS
Voltage Regulator Run from 110V_{AC} or 220V_{AC}: AN2, Pg. 8
Low Temperature Coefficient Power Regulator: LT1009 DS
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Strain Gauge Bridge Signal Conditioner: LT1013 DS

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SECTION 1—APPLICATION NOTES

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Questions and Answers on the SPICE Macromodel Library

Walt Jung

INTRODUCTION

This document is provided to answer some of the potential questions raised about the Linear Technology SPICE macromodel library. It assumes that you have a diskette copy of the library already, and want some background and/or additional information. Those needing a copy of the current SPICE macromodel diskette may obtain one by calling (800) 637-5545. The macromodel library is available on IBM PC format (high density) diskettes, in either 5.25″ or 3.5″ styles. If you should have a question not answered by this text, you may call LTC applications at (408) 432-1900. For more general SPICE questions, references are provided.

GETTING STARTED

Question (1): What hardware and software do I need to get the LTC SPICE model package up and running?

Answer (1): Obviously, you first need an IBM PC compatible computer with a high density drive, either 5.25″ or 3.5″. Beyond that, you will need only a minimal amount of RAM (512k or more). With this SPICE macromodel diskette, we have not just given you a model library, we have also furnished a working demo copy of PSpice™ from MicroSim, right on the diskette with our model software. To run this demo copy of PSpice, there are no minimum CPU speed, display or printer requirements. Unlike the production version, this special version of PSpice does not require a coprocessor to run, so you can see the models at work almost immediately, with no configuration or file editing necessary.

The demo PSpice version will run up to two models at once. To see it operate, all you need to do is slide the diskette into your computer, log onto the A: drive, and type in: "DEMOLTC <Enter>". The rest is all automatic!

Question (2): That sounds a bit too easy. Isn't there some configuration necessary to run SPICE? Also, is there some "on diskette" help available?

Answer (2): To minimize the configuration necessary for PSpice, the graphics display Probe™ comes pre-configured for a "text" style of screen display, one which will display a plot on any monitor. Once you get your feet wet, you will want to edit the Probe configuration file, "PROBE.DEV" to better match your equipment (this file is in the SPICE directory).

Yes, there are two help files on the diskette. One, "README.COM" is in the root directory, and it lists the specific LTC device types modeled. To use it type "README <Enter>", then just follow the on screen prompts. The information can also be printed out, if desired. The second help utility is "README2.COM", and it is in the SPICE directory. It has information on PSpice and Probe in general, and this demo version in particular. From the SPICE directory, type "README2 <Enter>" to use it, and follow the prompts. Note that this help file has the detailed info needed to customize "PROBE.DEV", with an ASCII editor. We recommend printing out the information in both of these help utilities for future reference.

Question (3): Where can I get more information on PSpice and Probe?

Answer (3): The two help utilities mentioned will serve you here, or write or call MicroSim (mentioning this demo diskette) at:

MicroSim Corporation
20 Fairbanks, Irvine, CA 92718
(714) 770-3022

Question (4): Will the devices in this LTC macromodel library run on any version of SPICE? Are they copy protected or encrypted?

Answer (4): You can use the LTC models with other versions of SPICE, either on a PC or another computer system. All of the LTC SPICE model files are furnished in an ASCII file format, which are actually usable on any type of computer; a PC, a workstation and/or mainframes. If you don't intend final use for them on a PC, they can be transferred from the PC environment to a dissimilar system via modem, using an error checking protocol (such as Xmodem or Kermit).

As was noted, the models are in ASCII form, and are designed to be Berkeley SPICE 2G.6 compatible (generic SPICE). They were in fact developed and debugged using PSpice, but other vendors' PC based SPICE implementations can be used with them, and they will also work on workstations and large mainframes (once transferred). So, while we can recommend PSpice as highly useful, the generic nature of our models allows their use on virtually any 2G.6 compatible host.

Since the models are ASCII files, they are easily copied, and we encourage use on diverse systems. Model encryption, in our opinion, is counter-productive to our goals of widespread LTC model use. In fact, it could be said that it is contrary to a "universal" SPICE 2G.6 ASCII file format.

MODEL COVERAGE

Question (5): How many of the LTC linear devices are now included in the SPICE macromodel library, and what device types are covered?

Answer (5): Right now, most of the LTC operational amplifier models are already contained in the library. This collection of 40-odd part numbers includes NPN and PNP bipolar and JFET input amplifier types. There is also an instrumentation amplifier, and it is hoped that more amplifiers will soon follow. Other linear devices (comparators, A/Ds, references, regulators) are not modeled as yet.

MODEL SUPPORT

Question (6): If your models are in fact ASCII files, that means they are easily edited and changed. Does this mean that I can "tweak" a model to suit my own specific needs?

Answer (6): You sure can edit the models, but you'd better understand all the implications of it before doing so! Modifying a model by definition makes it something other than what it was when released. Please note that LTC will only support models in their released form, and at our discretion. Does this then mean that you won't ever be able to make useful model changes? Not really, if you just use common sense, and keep an original reference copy of the model, in "as received" form. Common sense means that you don't change 10 model parameters, then call us up and ask why "our" model doesn't fly. LTC (or any other IC vendor) won't step into such a Pandora's box!

Question (7): What if I really do have a problem with the models? Will I be able to get help from LTC?

Answer (7): Problems using SPICE models will generally fall into one of three types: 1) Problems with the user's system which are hardware and/or software related, 2) Problems of application, that is a circuit application which presents some general modeling difficulty. Or, in some circumstance, 3) A real problem with the model itself. Obviously LTC cannot be responsible for the correct operation of your computer system and application of your software, so we will not become involved with case 1). Case 3), problems which can be directly attributed to an LTC model will be serviced at the discretion of LTC.

Case 2) is the most difficult of all, since it can actually be open-ended, with no practical solution. For example, you may need to simulate a circuit using an LTC model, but some other crucial part is not modeled, say something from another vendor. While we can sympathize with this dilemma, we could not logically be expected to help develop such a model. Due to time and manpower realities, we may not even be able to help develop a new model for one of our own parts (on short notice). More on this and related areas is answered in the next two questions.

Question (8): Are these models guaranteed to run?

Answer (8): Users should bear in mind that software models are at their very best just approximations of the real thing, that is they amount to clever apings of actual ICs. LTC does guarantee (and fully supports) its IC devices, the ones you plug in to do genuine work on your PC boards. By way of contrast, models are software support items, and are supplied on an "as is" basis. With regard to their use and performance, they should never be confused with the performance of the real item. Think about this as in the context of what gets shipped out your door as product, that is real, and measured performance results on it validates your equipment guarantees. Model results will likely mean little or nothing to your customers, since they are much less tangible to your product.

Question (9): What if a model functions, but it simply doesn't reveal everything I want it to?

Answer (9): It is entirely possible that a given model may fall short of specific expectations, especially if they tend towards the unrealistic or the impractical. We don't get paranoid when a real op amp has finite gain as opposed to infinite, we consider the implications in context and proceed from there. It is simply impractical (at least at this point in modeling evolution) to make a macromodel emulate a device's specs with 100% fidelity in all regards, and still remain compact, fast running, and free of convergence problems.

What we have done in developing these models is to take into account all those performance/spec areas we saw as most important, and then pay serious attention to them in the models. Granted, this is a judgement call on our part, but we hope it is a reasonable one. This does not rule out special cases, where a model may be optimized to satisfy a given set of customer requirements, and LTC will respond to these as they arise. And, we will welcome inputs on future models!

PARAMETERS MODELED

Question (10): OK then, what are the specific performance areas and specifications which these models do cover?

Answer (10): The LTC op amp macromodels simulate a number of performance areas and specs, as noted in Table 1. We have chosen typical parameters from the device datasheet in generating these models, and room temperature operation.

Table 1.

SPECIFICATION	MODELED?	MODELING ACCURACY
V_{OS}	Yes	High
I_B/I_{OS}	Yes	High
Gain-bandwidth	Yes	Medium
Phase margin	Yes	Medium
SR	Yes	Medium
AV (dc)	Yes	High
CMRR	Yes	High
PSRR	No	NA
V_{SAT} (+ and −)	Yes	High
I_{SC}	Yes	High
R_{OUT}	Yes	High
I_q	Yes	High
en	No*	NA
in	No*	NA

*The model topology used does not address input stage noise simulation. Use the LTC "NOISE" software instead, which does model the LTC op amps for voltage and current noise (see question 20).

In addition, there are functional areas of performance where modeling attention should be directed for realistic behavior. For example, if an op amp is designed as a single-supply device, then the input/output ranges of the model should include the V^- rail (ground), with good accuracy. If clamping networks are used at the input, then the model should reflect this, and clamp at the same level. If the amplifier is pole-zero compensated, its transient response will not resemble a classic single pole plus parasitic rolloff, and the model should address this. Table 2 summarizes the LTC model characteristics in these functional regards.

Table 2.

CHARACTERISTIC	MODELED?	MODELING ACCURACY
Multiple pole/zero	Yes	Medium
Single supply op.	Yes	High
Common-mode clamps	Yes	Medium
Differential clamps	Yes	Medium

MODEL TOPOLOGY

Question (11): Sometimes it appears that the terms "model" and "macromodel" are being used interchangeably. Is there a difference, and what defines a macromodel?

Answer (11): "Model" is a general term, and a "macromodel" is a specific model form, one which is more compact and efficient. To be historically precise, the op amp macromodel was devised by Boyle[1] originally, and has been used since then. An op amp macromodel differs from a full "device level" model in that key parts of the circuit are defined by the use of synthetic SPICE elements, that is controlled current/voltage sources, etc., along with passive circuit elements such as Rs and Cs, and a minimum number of (simplified) semiconductors. By reducing the number of semiconductor junctions to a minimum, an op amp macromodel can achieve simulation times 5 to 10 times faster than a device level model, and so easily allow multiple amplifier simulations for large systems.

Question (12): This sounds like an area of tradeoff! Certainly a macromodel using synthesized elements cannot perform like a real device level model, can it?

Answer (12): For many aspects of performance, one cannot tell that macromodeling has been used. For any performance aspect with simulation speed as a criterion, a macromodel approach will almost always be faster, and with reasonable fidelity, *when properly executed*. A qualifying note here . . . comparatively speaking, we will rule out a SPICE "ideal" op amp model, which can be built with one or a few controlled sources. We feel this is too far removed from a real IC op amp, as it will be devoid of real bias currents, offset voltages, slew rates, etc.

The most useful macromodel approach is one which carefully balances the mutual goals of reasonable fidelity to the real part, along with a realistic simulation time, and finally the overall vigor or robustness of the model. The importance of the first two of these points cannot be overemphasized in considering the evolution of op amp macromodeling. As a case in point, it is not a widely useful thing to improve say, the fidelity of an op amp's transient response with a complex model which departs from the simplicity and speed advantages of a more basic model. In the extreme, one might find a board's worth of "more sophisticated" op amp models which takes all night to run simulations, or worst yet, won't run at all!

Question (13): What is meant by "won't run at all?" Is that related to the reported convergence problems of SPICE?

Answer (13): Yes, there are macromodel types which have been published which have problems with SPICE convergence for certain types of simulations. In the extreme case, a solution cannot be found and the simulator just quits, reporting an error. "Tweaking" of the simulator defaults may be necessary to make it run, and then slowly. Try a unity-gain follower small signal transient analysis to separate the macromodel wheat-from-chaff, and to see what a "robust" macromodel implies.

To our minds, it is simply not enough that a model yield good fidelity with the electrical results, it should also do so with reasonable speed and not be overly sensitive to system memory, applied signal, biasing, and/or supply voltages. So, we have purposely included a transient test for the LT1007 (one of our more complex models) in our demo to illustrate this point. We will be interested to learn of comparative tests, using other models (see Appendix).

THE BOYLE MODEL AND LTC IMPROVEMENTS

Question (14): We take it then, that your LTC models are based on the Boyle macromodel. Is it true that this model cannot handle differing transistor types, and that it has other serious deficiencies?

Answer (14): Yes, the LTC macromodels are in fact derived from the basic Boyle model. We should hasten at this point to note that this model is apparently little understood in terms of real versus perceived limits! In fact, many Boyle derived models (and we include LTC's here) are related topologically, but have been enhanced in many different and significant ways. Perhaps a fitting analogy is that all present day cars using internal combustion engines are in a sense related to Henry Ford's Model T. This

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Note 1: Boyle, G.R., Cohn, B.M., Pederson, D.O., Solomon, J.E. "Macromodeling of Integrated Circuit Operational Amplifiers," *IEEE Journal of Solid-State Circuits*, Vol. SC-9, #6, December 1974.

is of course intentionally dramatized to make the following point: Most of us will have no trouble at all appreciating that a basic design concept can be usefully enhanced in many aspects, while still retaining a fundamental lineage.

Yes, the original Boyle model used NPN bipolar input stage transistors, in the context of a 741. But replacing them with PNP types simply changes the connections, not the basic design equations. FET transistors were added to the Boyle model in 1979, in the paper by Krajewska and Holmes,[2] in both JFET and MOSFET form. Anyone implying that a Boyle-based model can't handle a variety of transistor types is confused as to history!

Question (15): But the Boyle model cannot handle multiple poles and zeros, and is therefore not suited for accurate transient response simulations. Some companies have discarded that approach long ago. How can you guys still be using it, with all those problems?

Answer (15): The LTC macromodels were developed with an attitude that transient response fidelity, while important, should not necessarily be achieved at the expense of many other equally critical performance areas. Accordingly, LTC macromodels use extensions to the overall Boyle topology for additional poles and zeros, as opposed to discarding it outright. This technique allows additional control over phase response, while still retaining relative simplicity. The LT1007 demo example cited uses this form of compensation, and the results can be seen in the demo example (see Appendix). This approach does have the virtue of still retaining the overall form of the Boyle topology. While it may be possible to more accurately simulate an OP-27, for example, with up to 10 pole-zero pair networks, a legitimate question arises: Is it worth the substantial overhead of the many additional active stages, for each and every simulation, however trivial? Every element added to a SPICE macromodel extracts some penalty in terms of speed, memory required, or overall model vigor. Carried to the extreme, significantly more complex models may even preclude multiple amplifier simulations, defeating the very purpose of macromodeling.

Question (16): The last statement seems to be a contradiction, as you have added additional networks, diode clamps, and entire circuit sections to model the unique internal features of your op amps. If you question others adding additional stages, how then can you justify it?

Answer (16): The answer lies in exactly how one goes about it! We certainly do recognize the potential penalties these added features can represent to users who simply may not care about a particular detail which they may be simulating. So, we have generally implemented them in ways which allow them to be easily disconnected. For example, the diode clamps at the inputs of the LT1078 series can be disconnected if they get in the way, as can the differential clamps for the LT1007 (and others). In other words, we haven't locked anyone away from stripping the model bare, so to speak, should they so wish. In most instances, a "*" in column one of a line is all that is needed to deactivate it.

Question (17): The Boyle model uses a ground node internally, node zero (node 0). Isn't it true that this creates simulation errors for power supply and load currents?

Answer (17): The model we use does have a node zero internally, which happens to be the default common (ground, or node 0) for SPICE circuits in general. The output signal current of our models therefore flows through this common node, and to/from the common node of the overall circuit in which it is used. Usually this is a common ground between source(s) and the load(s).

In our models (and most others which operate similarly) the actual model output current comes from controlled sources, which are referred to ground (node 0), inside the model. To an extent, this node voltage can be somewhat arbitrary; that is, it is possible for it to be referred to other points, and the model will still operate normally. For example, the "node 0" in single-supply op amps such as the LT1078 series gets tied to V^- in the main circuit, when the device is used in a single-supply mode (since the V^- pin, #4 is tied to ground). All still works OK in this fashion. If the very same model is used with dual supplies, obviously "node 0" gets referred to a level which is intermediate between the two supply levels, such as +15V and −15V.

Note 2: Krajewska, G., Holmes, F.E. "Macromodeling of FET/Bipolar Operational Amplifiers," *IEEE Journal of Solid-State Circuits*, Vol. SC-14, #6, December 1979.

A better understanding of how this operates can be realized if it is appreciated that the SPICE controlled sources do indeed have two terminal floating outputs, which can be referred to various levels. Thus, the op amp's output (load) current can actually be different from the power supply rail current, for the case where the internal common node (node 0) is not tied to a supply rail.

Is all of this a real problem? It actually becomes more one of bookkeeping, or adding up all the currents properly. We hope it is then not a great one, since the total current drain will still be that in the load, plus the static drain of the op amp itself. We have taken the step of making all the models reflect an internal DC power supply current which is that value typical to their operation (the real LT1007 draws 2.7mA, therefore Iee + Ip totals 2.7mA in the model).

SOME GENERAL SPICE QUESTIONS

Question (18): All of this seems to be implying that SPICE simulations can be quite burdensome, in terms of getting up and running to a point of realizing useful results. What can be said about this aspect to someone just getting started with modeling?

Answer (18): SPICE simulation is unquestionably very involved, and it is also quite demanding of analog circuit skills along with general computer proficiency. It is just as demanding of the computer hardware as well. While you don't need to be a programmer to use SPICE efficiently, well developed computer skills definitely do help. More important to overall effectiveness however is a strong design engineering background, in particular one in analog circuit design.

This should seem obvious, since SPICE is an analog simulator. But, it is being stressed here to make the point that someone proficient in analog design will likely produce quality SPICE results much faster than one equally proficient in digital design, with both starting from zero. Why? Because SPICE has its quirks, which must be dealt with to use it most effectively. By and large, there are often analogs between SPICE software problems and linear circuit problems. Thus, it helps in dealing with these types of problems to be comfortable in "thinking analog." Analog designers also tend to be well-developed in terms of patience, and SPICE if nothing else will be a challenge to one's patience!

These generalizations aside, SPICE will definitely be most demanding of hardware, as the bigger and faster the computer, the more quickly you get your results. The PSpice demo supplied with this macromodel library is quite exceptional in terms of what it does, but this does not change the fact that the full version counterpart is more demanding on the hardware. In the SPICE world, hardware dollars for RAM, coprocessors, and faster CPUs buy overall speed and complex circuit capability.

Question (19): OK, assuming that these general requirements can be met, what other potential bottlenecks lie in the path of my trip towards SPICE bliss?

Answer (19): Given adequate resources in terms of manpower and computer hardware/software, the next fundamental obstacle is the availability and quality of models. One certainly wouldn't want to build up a breadboard circuit faced with the necessity to make all the op amps up from scratch, but that is where you'd stand for a SPICE simulation without adequate models. Even assuming you had the time and manpower resources to make your own models, there is the very real question of their technical sufficiency.

Now, this actually brings us full circle, with the IC manufacturer such as LTC entering the picture as a supplier of op amp models for their catalog of devices. With this circumstance, you, as an IC user, are in the very best position to do useful simulations, since it is in the IC manufacturers interest to supply you with models that reasonably reflect actual device performance. This establishes your confidence in the devices as well as speeding your design towards completion, with a minimum of hassle with models.

Of course, this does not make the modeling problem go completely away, it only lessens it appreciably, with regard to LTC as one vendor. You still need models for all parts of your circuit, beyond the op amps. This will very likely continue to be a serious challenge in the months and years ahead, as more and more vendors become active with modeling support of their devices.

Question (20): The bottom line seems to be that the SPICE user in today's design world has their work really cut out for them. What level of confidence can be expected with SPICE op amp simulations, given typical designs and your models?

Answer (20): SPICE simulation results can and will vary in fidelity with regard to a real live op amp, dependent upon the type of circuit in use. Generally speaking, DC and low frequency AC results are good to excellent, and the models do a nice job with bias currents, offset voltages, and most input related parameters. By contrast, noise is not modeled well at all with the enhanced Boyle topology we employ, but we do provide a useful option here, in the form of the alternative software, Alan Rich's program "NOISE"[3] (available as noted).

The high frequency response of LTC wideband op amps such as the LT1007 and OP-27 is modeled with multiple poles and zeros, which yields a reasonable approximation to the real device's transient response (see demo). It is worthwhile noting that the precise pulse fidelity of a single given sample of a wideband amplifier is in reality a "moving-target." This is because device-to-device production variations can be of the same degree as the errors in their current modeling! Therefore, there is some question as to just what benefit a more precise high frequency model would provide.

The particular performance area of transient response has been and will continue to be one of challenge in terms of better models (without pitfalls). It is also likely to continue as one of controversy, in terms of the best overall solution to the technical challenge.

Output stage performance of the LTC models is good to excellent, with accurate current and voltage limits, and good simulation of the small signal characteristics, particularly the single supply devices near the rails.

All-in-all, we feel that this model collection is a quite useful addition to the analog designer's bag of tricks. Like the SPICE program itself, the models are no panacea, and they need to be used carefully and wisely. You will very likely encounter many crossroads with SPICE models, and often be tempted to decide between the lab results and a SPICE simulation . . . which one to believe? Our advice here is to not accept either without first carefully checking, but do be inclined to lean towards the lab performance of the real device, particularly if it passes all the conventional analog bench tests . . . Remember, that is real by default, while SPICE is a mimic by default!

We hope that the LTC models serve you well, and welcome your feedback on them.

SOME GENERAL SPICE REFERENCES

1. Nagel L.W., Pederson, D.O.	"Simulation Program with Integrated Circuit Emphasis (SPICE)," University CA @ Berkeley, ERL-M382, 1973.
2. Nagel, L.W.	"SPICE2: A Computer Program to Simulate Semiconductor Circuits," University CA @ Berkeley, ERL-M520, 1975.
3. Cohen, E.	"Program Reference for SPICE2," University CA @ Berkeley, ERL-M592, 1976.

Available from:

EECS/ERL Industrial Support Office
497 Cory Hall, University CA @ Berkeley
Berkeley, CA 94720

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[3] **Note 3:** Rich A. "Noise Calculation in Op Amp Circuits," LTC Design Note #15, September, 1988. (Program available on diskette, call (800) 637-5545).

APPENDIX

The LT1007 Op Amp Macromodel Transient Test Demonstration

```
03/02/90  ★★  Evaluation PSpice (LT 3.06)  ★★  08:41:27

LTC LT1007 VOLTAGE FOLLOWER DEMO: OUTPUT = V(55)
```

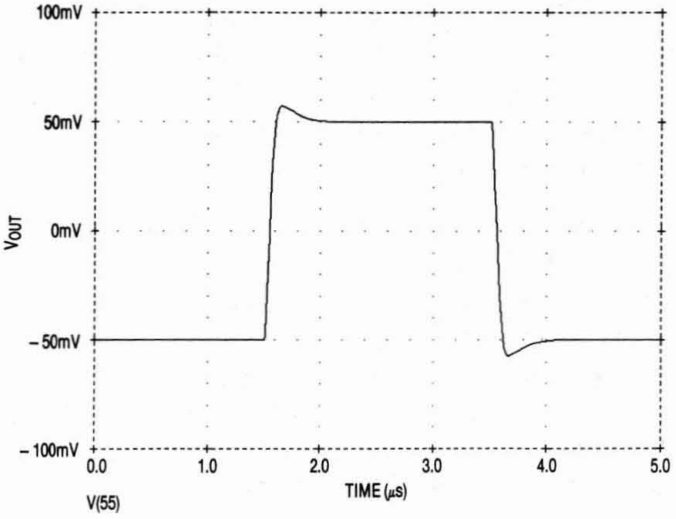
(edited for clarity/brevity; comments italicized)

```
MATRIX SOLUTION         6.09      4
MATRIX LOAD             8.74
READIN                  2.48
SETUP                   0.05
DC SWEEP                0.00      0
BIAS POINT              1.98     32
AC and NOISE            0.00      0
TRANSIENT ANALYSIS     22.41    455
OUTPUT                  0.22
TOTAL JOB TIME         26.53
```

Shown above are (edited) portions of an actual output file, "DEMO.OUT," as run from files on a released LTC SPICE macromodel diskette. The test is a small signal, voltage follower transient test. The computer used is a 16 megahertz 386 w/387 math coprocessor, and the times shown in the left column reflect operation from a RAM disc. Actual running times for other situations will vary. We invite relative comparisons using other models for this same transient test (edit "DEMO.CIR," to include your comparison model).

Shown below is the LT1007 test waveform simulated in this transient analysis, as seen on the screen.

LTC LT1007 Voltage Follower Demo: Output = V(55)



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LINEAR TECHNOLOGY
Application Note 42
June 1991

Voltage Reference Circuit Collection

Brian Huffman

This application note is a guidebook of circuits featuring voltage reference ICs in various configurations. The circuits shown are both basic as well as complex and employ many popular IC references. Included are 2-terminal and 3-terminal references in series and shunt modes, for positive and negative polarities, in voltage and current boosted versions. Additional circuit information can be located in the references listed in the index. The reference works as follows, i.e., AN8, page 2 = Application Note 8, page 2; LTC1044 DS = LTC1044 data sheet.

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Programmable Reference with Adjustable Current Limit	Figure 14	6	LT1431 DS
Basic Operation of Shunt Reference Family	Figure 1	5	LT1004 DS
Current Source Stabilized Reference	Figure 2	5	LM334 DS
Low TC Current Stabilized Reference	Figure 3	5	

Temperature Stabilized Reference

FIGURE TITLE	FIGURE #	PAGE	REFERENCE/SOURCE
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10V Output, Self-Biased Temperature Stabilized Reference	Figure 70	17	LM399 DS
Ultra-Precision Variable Voltage Reference	Figure 71	18	AN6, page 6
10V Output, Temperature Stabilized Reference	Figure 72	18	LM399 DS
Temperature Stabilized 10V Buffered Reference	Figure 73	18	LT1012 DS
6.95V Output, Temperature Stabilized Reference (V_{IN} = ± 15V)	Figure 74	19	LM399 DS
6.95V Output, Temperature Stabilized Reference (V_{IN} = 9V to 40V)	Figure 75	19	LM399 DS
6.95V Output, Temperature Stabilized Reference (V_{IN} = –9V to –33V)	Figure 76	19	LM399 DS
10V Output, Temperature Stabilized Reference	Figure 66	15	LT1019 DS
Low Noise, Ultra Low Drift, Long Term Stable 7V Positive Reference	Figure 67	16	LTZ1000 DS
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Appendix

FIGURE TITLE	FIGURE #	PAGE	REFERENCE/SOURCE
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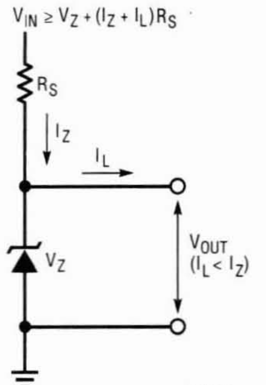
Trimming Techniques	Appendix C	29	

*See also 2-Terminal References

VOLTAGE REFERENCE SELECTION GUIDE*

* COMMERCIAL 0°C to + 70°C
** LTZ1000 requires external control and biasing circuits.

VOLTAGE V_Z (VOLTS)	VOLTAGE TOLERANCE MAXIMUM $T_A = 25°C$	DEVICE	TEMPERATURE DRIFT, ppm/°C OR mV CHANGE	OPERATING CURRENT RANGE (OR SUPPLY CURRENT)	MAXIMUM DYNAMIC IMPEDANCE (Ω)	MAJOR FEATURE
1.235	±0.32%	LT1004C-1.2	20ppm (typ)	10μA to 20mA	1.5	Micropower
	±0.32%	LT1004CS8-1.2	20ppm (typ)	10μA to 20mA	1.5	Micropower
	±1%	LT1034BC-1.2	20ppm (max)	20μA to 20mA	1.5	Low TC Micropower with 7V Aux. Reference
	±1%	LT1034C-1.2	40ppm (max)	20μA to 20mA	1.5	Low TC Micropower with 7V Aux. Reference
	±2%	LM385-1.2	20ppm (typ)	15μA to 20mA	1.5	Micropower
	±1%	LM385B-1.2	20ppm (typ)	15μA to 20mA	1.5	Micropower
2.5	±0.5%	LT1004C-2.5	20ppm (typ)	20μA to 20mA	1.5	Micropower
	±0.8%	LT1004CS8-2.5	20ppm (typ)	20μA to 30mA	1.5	Micropower
	±0.2%	LT1009C	6mV (max)	400μA to 10mA	1.4	Precision
	±2.5%	LT1009S8	25ppm (max)	400μA to 20mA	0.6	Precision
	±0.2%	LT1019C-2.5	20ppm (max)	1.2mA	N/A	Precision Bandgap
	±4%	LM336-2.5	6mV (max)	400μA to 10mA	1.4	General Purpose
	±2%	LM336B-2.5	6mV (max)	400μA to 10mA	1.4	General Purpose
	±3%	LM385-2.5	20ppm (typ)	20μA to 20mA	1.5	Micropower
	±1.5%	LM385B-2.5	20ppm (typ)	20μA to 20mA	1.5	Micropower
	±3%	LT580J	85 (max)	1.5mA	N/A	3 Terminal Low Drift
	±1%	LT580K	40 (max)	1.5mA	N/A	3 Terminal Low Drift
	±0.4%	LT580L	25 (max)	1.5mA	N/A	3 Terminal Low Drift
	±0.4%	LT580M	10 (max)	1.5mA	N/A	3 Terminal Low Drift
4.5	±0.2%	LT1019C-4.5	20ppm (max)	1.2mA	N/A	Precision Bandgap
5.0	±0.2%	LT1019C-5	20ppm (max)	1.2mA	N/A	Precision Bandgap
	±1%	LT1021BC-5	5ppm (max)	1.2mA	0.1	Very Low Drift
	±0.05%	LT1021CC-5	20ppm (max)	1.2mA	0.1	Very Tight Initial Tolerance
	±1%	LT1021DC-5	20ppm (max)	1.2mA	0.1	Low Cost, High Performance
	±1%	LT1021CS8	20ppm (max)	1.2mA	0.1	Low Cost, High Performance
	±0.02%	LT1027A	2ppm (max)	2.0mA	N/A	Low Drift, Tight Tolerance
	±0.05%	LT1027B	2ppm (max)	2.0mA	N/A	Low Drift, Tight Tolerance
	±0.05%	LT1027C	3ppm (max)	2.0mA	N/A	Low Drift, Tight Tolerance
	±0.05%	LT1027D	5ppm (max)	2.0mA	N/A	Low Drift, Tight Tolerance
	±0.1%	LT1027E	7.5ppm (max)	2.0mA	N/A	Low Drift, Tight Tolerance
	±0.2%	LT1029AC	20ppm (max)	700μA to 10mA	0.6	Precision Bandgap
	±1%	LT1029C	34ppm (max)	700μA to 10mA	0.6	Precision Bandgap
	±0.3%	REF02E	8.5ppm (max)	1.4mA	N/A	Precision Bandgap
	±0.5%	REF02H	25ppm (max)	1.4mA	N/A	Precision Bandgap
	±1%	REF02C	6.5ppm (max)	1.6mA	N/A	Precision Bandgap
	±2%	REF02E	250ppm (max)	2.0mA	N/A	Bandgap
6.9	±3%	LM329A	10ppm (max)	600μA to 15mA	1.0 (typ)	Low Drift
	±5%	LM329B	20ppm (max)	600μA to 15mA	1.0 (typ)	Low Drift
	±5%	LM329C	50ppm (max)	600μA to 15mA	1.0 (typ)	General Purpose
	±5%	LM329D	100ppm (max)	600μA to 15mA	1.0 (typ)	General Purpose
	±4%	LTZ1000	0.1ppm/°C	4mA	20.0	Ultra Low Drift, 2ppm Long Term Stability**
6.95	±5%	LM399	2ppm (max)	500μA to 10mA	1.5	Ultra Low Drift
	±5%	LM399A	1ppm (max)	500μA to 10mA	1.5	Ultra Low Drift
7.0	±0.7%	LT1021BC-7	5ppm (max)	1.0mA	0.2	Low Drift/Noise, Exc. Stability
	±0.7%	LT1021DC-7	20ppm (max)	1.0mA	0.2	Low Cost, High Performance
10.0	±0.2%	LT1019C-10	20ppm (max)	1.2mA	N/A	Precision Bandgap
	±0.5%	LT1021BC-10	5ppm (max)	1.7mA	0.25	Very Low Drift
	±0.05%	LT1021CC-10	20ppm (max)	1.7mA	0.25	Very Tight Initial Tolerance
	±0.5%	LT1021DC-10	20ppm (max)	1.7mA	0.25	Low Cost, High Performance
	±0.5%	LT1031BC	5ppm (max)	1.7mA	0.25	Very Low Drift
	±0.1%	LT1031CC	15ppm (max)	1.7mA	0.25	Very Tight Initial Tolerance
	±0.2%	LT1031DC	25ppm (max)	1.7mA	0.25	Low Cost, High Performance
	±0.3%	LT581J	30ppm (max)	1.0mA	N/A	3 Terminal Low Drift
	±0.1%	LT581K	15ppm (max)	1.0mA	N/A	3 Terminal Low Drift
	±0.3%	REF01E	8.5ppm (max)	1.4mA	N/A	Precision Bandgap
	±0.5%	REF01H	25ppm (max)	1.4mA	N/A	Precision Bandgap
	±1%	REF01C	65ppm (max)	1.6mA	N/A	Precision Bandgap



$V_{IN} \geq V_Z + (I_Z + I_L)R_S$
R_S
I_Z
I_L
V_{OUT}
$(I_L < I_Z)$
V_Z

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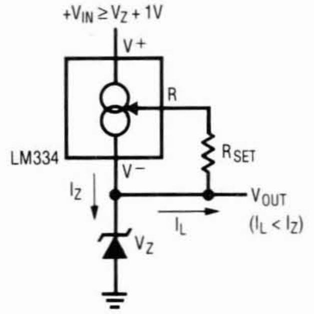
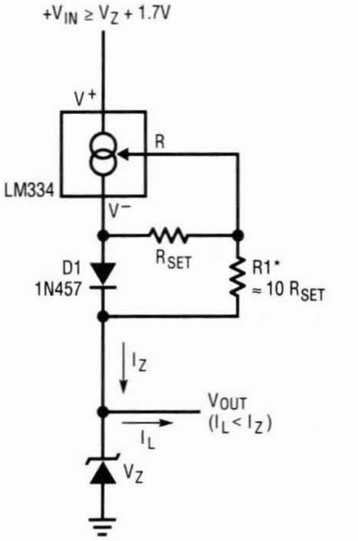
Figure 1. Basic Operation of Shunt Reference Family



$+V_{IN} \geq V_Z + 1V$
V+
R
LM334
R_{SET}
V−
I_Z
V_{OUT}
I_L
$(I_L < I_Z)$
V_Z

I_Z	R_{SET}
10µA	6.82k
100µA	6.82Ω
1mA	68.2Ω
10mA	6.82Ω

Figure 2. Current Source Stabilized Reference



$+V_{IN} \geq V_Z + 1.7V$
V+
R
LM334
V−
R_{SET}
D1
1N457
R1*
$\approx 10\ R_{SET}$
I_Z
V_{OUT}
$(I_L < I_Z)$
I_L
V_Z

$$I_Z \cong \frac{67mV}{R_{SET}} + \frac{667mV}{R1}$$

* TRIM R1 FOR MIN T_C OF I_Z (IF NECESSARY)

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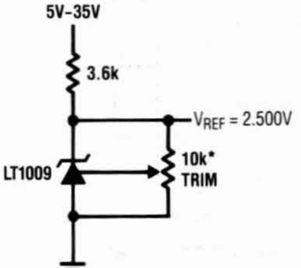
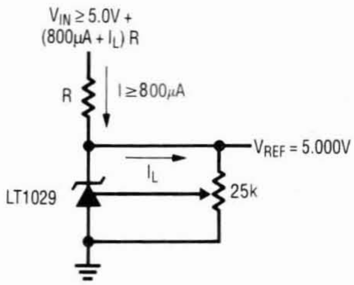
Figure 3. Low TC Current Stabilized Reference



5V-35V
3.6k
V_{REF} = 2.500V
LT1009
10k*
TRIM

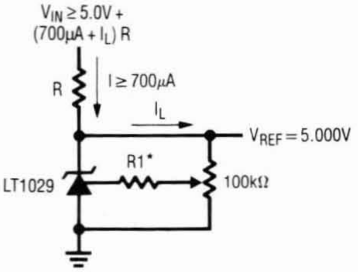
*DOES NOT AFFECT TEMPERATURE COEFFICIENT ±5% TRIM RANGE

Figure 4. 2.5V Output Reference, ±5% Trim Range



$V_{IN} \geq 5.0V +$
$(800\mu A + I_L)$ R
R
$I \geq 800\mu A$
V_{REF} = 5.000V
I_L
LT1029
25k

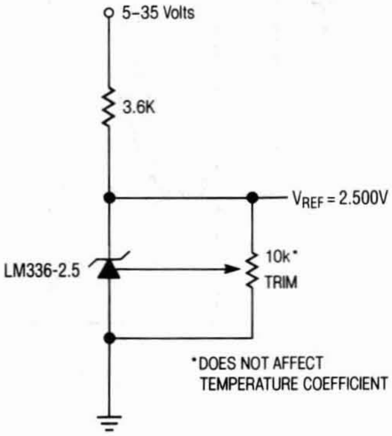
Figure 5. 5V Output Reference, +5%, −13% Trim Range



$V_{IN} \geq 5.0V +$
$(700\mu A + I_L)$ R
R
$I \geq 700\mu A$
I_L
$V_{REF} = 5.000V$
R1*
LT1029
100kΩ

TRIM RANGE
0.4% — LT1029A, R1 = 750k
1.2% — LT1029, R1 = 250k

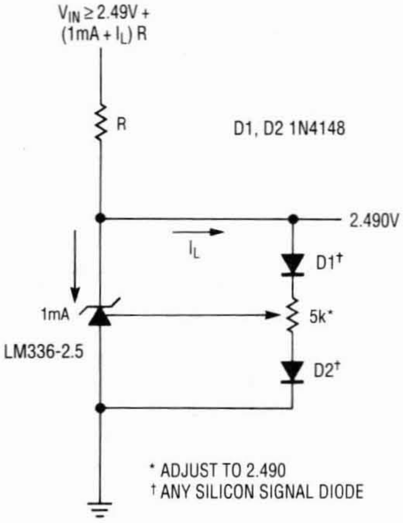
Figure 6. 5V Output Reference, Narrow Trim Range



5–35 Volts
3.6K
V_{REF} = 2.500V
LM336-2.5
10k*
TRIM

*DOES NOT AFFECT TEMPERATURE COEFFICIENT

Figure 7. 2.5V Output, Temperature Independent Trim



$V_{IN} \geq 2.49V +$
$(1mA + I_L)$ R
R
D1, D2 1N4148
2.490V
I_L
D1†
1mA
5k*
LM336-2.5
D2†

* ADJUST TO 2.490
† ANY SILICON SIGNAL DIODE

Figure 8. 2.490V Output, Trim for Minimum TC

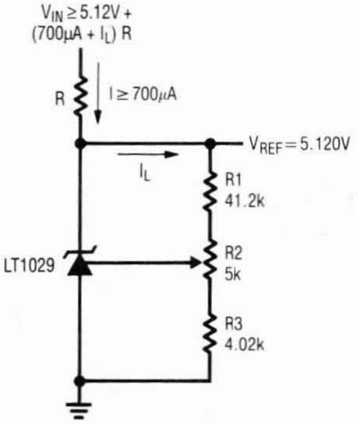

$V_{IN} \geq 5.12V +$
$(700\mu A + I_L)$ R
R
$I \geq 700\mu A$
$V_{REF} = 5.120V$
I_L
R1
41.2k
LT1029
R2
5k
R3
4.02k

Figure 9. 5.120V Output, Trimmed Reference

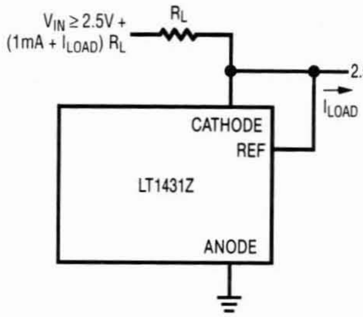

$V_{IN} \geq 2.5V +$
$(1mA + I_{LOAD})$ R_L
R_L
2.5V
I_{LOAD}
CATHODE
REF
LT1431Z
ANODE

Figure 10. 2.5V Reference

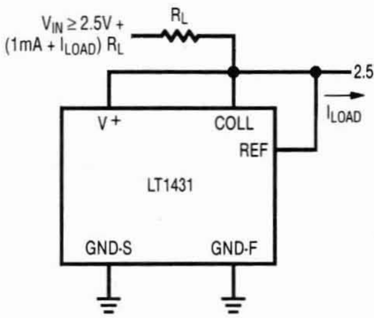

$V_{IN} \geq 2.5V +$
$(1mA + I_{LOAD})$ R_L
R_L
2.5V
I_{LOAD}
V+
COLL
REF
LT1431
GND-S
GND-F

Figure 11. 2.5V Reference

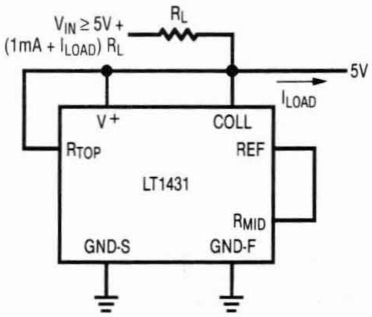
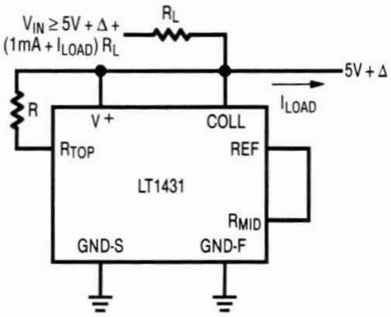
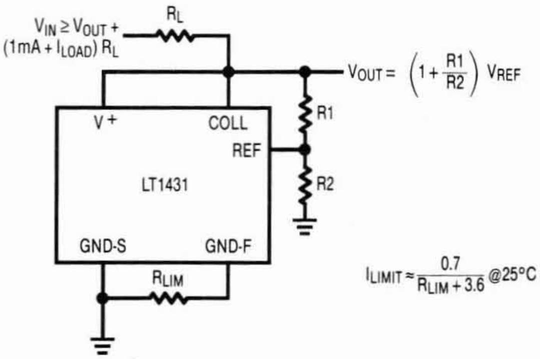

$V_{IN} \geq 5V +$
$(1mA + I_{LOAD})$ R_L
R_L
5V
I_{LOAD}
V+
COLL
R_{TOP}
REF
LT1431
R_{MID}
GND-S
GND-F

Figure 12. 5V Reference


$V_{IN} \geq 5V + \Delta +$
$(1mA + I_{LOAD})$ R_L
R_L
$5V + \Delta$
I_{LOAD}
R
V+
COLL
R_{TOP}
REF
LT1431
R_{MID}
GND-S
GND-F

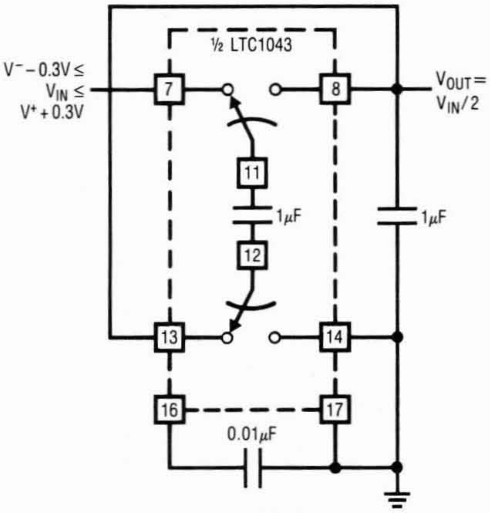
$\Delta = R \times (0.5mA) \pm 25\%$ PROCESS TOLERANCE
$\Delta \leq 500mV$

Figure 13. Increasing 5V Reference


$V_{IN} \geq V_{OUT} +$
$(1mA + I_{LOAD})$ R_L
R_L
$V_{OUT} = \left(1 + \frac{R1}{R2}\right) V_{REF}$
V+
COLL
REF
R1
LT1431
R2
GND-S
GND-F
R_{LIM}

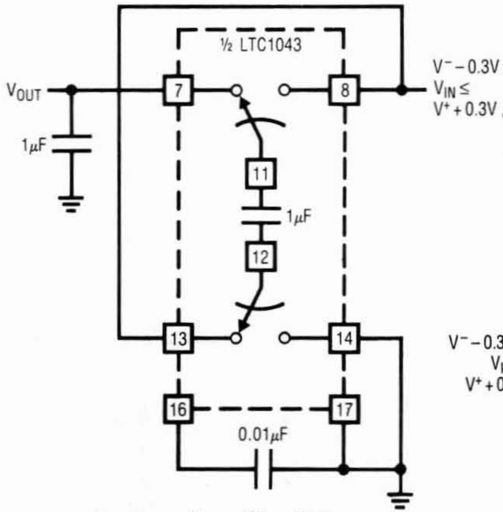
$I_{LIMIT} \approx \frac{0.7}{R_{LIM} + 3.6}$ @25°C

Figure 14. Programmable Reference with Adjustable Current Limit


½ LTC1043
$V^- - 0.3V \leq$
$V_{IN} \leq$
$V^+ + 0.3V$
7
8
$V_{OUT} =$
$V_{IN}/2$
11
1µF
1µF
12
13
14
16
17
0.01µF

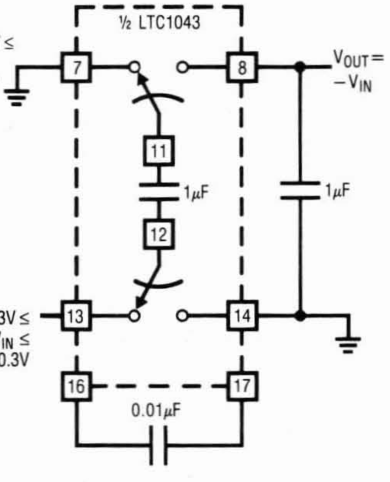
$V_{OUT} = V_{IN}/2 \pm 1ppm$
$0 \leq V_{IN} \leq V+$
$3 \leq V+ \leq 18V$

Figure 15. Precision Divide by Two


½ LTC1043
V_{OUT}
1µF
7
8
$V^- - 0.3V \leq$
$V_{IN} \leq$
$V^+ + 0.3V$
11
1µF
12
13
14
16
17
0.01µF

$V_{OUT} = 2V_{IN} \pm 5ppm$
$0 \leq V_{IN} < V+/2$
$3 \leq V+ \leq 18V$

Figure 16. Precision Multiply by Two


½ LTC1043
7
8
$V_{OUT} =$
$-V_{IN}$
11
1µF
1µF
12
$V^- - 0.3V \leq$
$V_{IN} \leq$
$V^+ + 0.3V$
13
14
16
17
0.01µF

$V_{OUT} = -V_{IN} \pm 2ppm$
$V- < V_{IN} < V+$
$V+ = +5V$, $V- = -5V$

Figure 17. Ultra-Precision Voltage Inverter

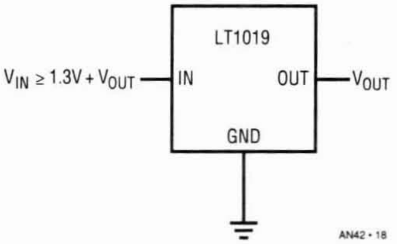

LT1019
$V_{IN} \geq 1.3V + V_{OUT}$
IN
OUT
V_{OUT}
GND
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Figure 18. Basic Hookup for LT1019 Series Reference

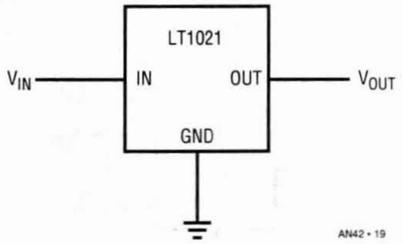
LT1021
V_{IN}
IN
OUT
V_{OUT}
GND
AN42 • 19

Figure 19. Basic Hookup for LT1021 Series Reference

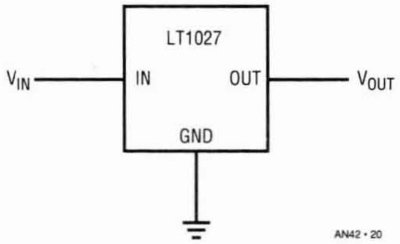
LT1027
V_{IN}
IN
OUT
V_{OUT}
GND
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Figure 20. Basic Hookup for LT1027 Series Reference

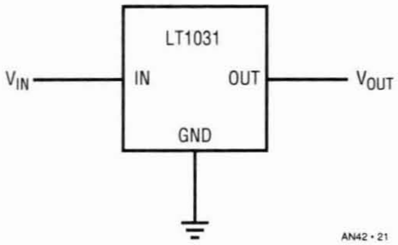
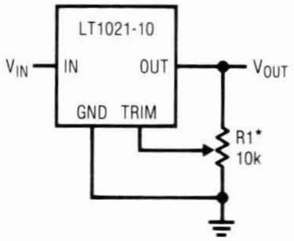
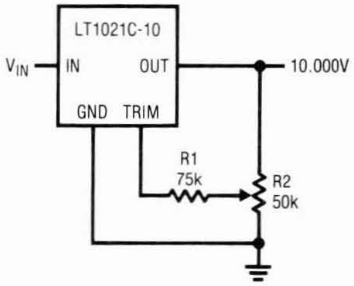

LT1031
V_{IN}
IN
OUT
V_{OUT}
GND
AN42 • 21

Figure 21. Basic Hookup for LT1031 Series Reference


LT1021-10
V_{IN}
IN
OUT
V_{OUT}
GND
TRIM
R1*
10k

* LOW TC CERMET
(CAN BE RAISED TO 20kΩ FOR
LESS CRITICAL APPLICATIONS)

Figure 22. 10V Output, Full Trim Range (±0.7%)


LT1021C-10
V_{IN}
IN
OUT
10.000V
GND
TRIM
R1
75k
R2
50k

TRIM RANGE ≈ ±10mV

Figure 23. 10V Output, Restricted Trim Range for Improved Resolution

LT1031 PERFORMANCE

DEVICE	V_{OUT}	TC IN ppm/°C (TYP/MAX)
LT1031B	10V ±5mV	3/5
LT1031C	10V ±10mV	6/15
LT1031D	10V ±20mV	10/25

LT1021 PERFORMANCE

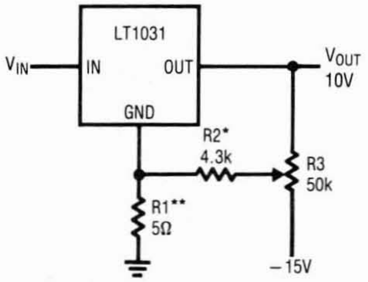
DEVICE	V_{OUT}	TC IN ppm/°C (TYP/MAX)
LT1021C-5	5V ±2.5mV	3/20
LT1021B-5	5V ±50mV	2/5
LT1021B-7	7V ±50mV	2/5
LT1021D-7	7V ±50mV	3/20
LT1021C-10	10V ±5mV	5/20
LT1021B-10	10V ±50mV	2/5

LT1019 PERFORMANCE

DEVICE	V_{OUT}	TC IN ppm/°C (TYP/MAX); C = COM, M = MIL
LT1019A-2.5	2.5V ±1.25mV	3/5 (C), 5/10 (M)
LT1019-2.5	2.5V ±5mV	5/20 (C), 8/25 (M)
LT1019A-5	5V ±2.5mV	3/5 (C), 5/10 (M)
LT1019-5	5V ±10mV	5/20 (C), 8/25 (M)
LT1019A-10	10V ±5mV	3/5 (C), 5/10 (M)
LT1019-10	10V ±20mV	5/20 (C), 8/25 (M)

LT1027 PERFORMANCE

DEVICE	V_{OUT}	TC IN ppm/°C (TYP/MAX)
LT1027A	5V ±1mV	1/2
LT1027B	5V ±2.5mV	1/2
LT1027C	5V ±2.5mV	2/3
LT1027D	5V ±2.5mV	3/5
LT1027E	5V ±5mV	5/7.5


LT1031
VIN
IN
OUT
VOUT
10V
GND
R2*
4.3k
R3
50k
R1**
5Ω
–15V

*CAN BE INCREASED TO 5.6k FOR LT1031B AND LH0070-2

**INCREASE TO 10Ω FOR LT1031D

Figure 24. 10V Output, Trimmed Reference

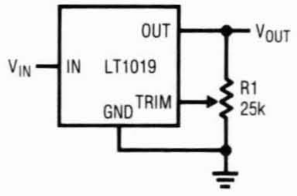
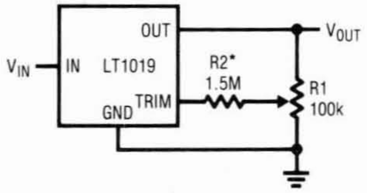
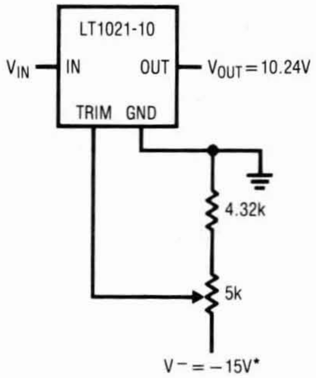

OUT
VOUT
VIN
IN
LT1019
GND
TRIM
R1
25k

Figure 25. Wide Trim Range (±5%)


OUT
VOUT
VIN
IN
LT1019
R2*
1.5M
GND
TRIM
R1
100k

*INCREASE TO 4.7MΩ FOR LT1019A (±0.05%)

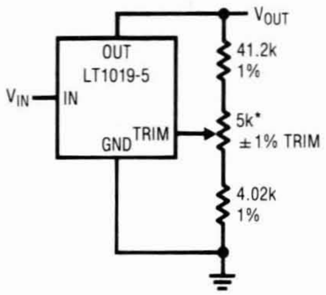
Figure 26. Narrow Trim Range (±0.2%)


LT1021-10
VIN
IN
OUT
VOUT = 10.24V
TRIM
GND
4.32k
5k
V– = –15V*

*MUST BE WELL REGULATED

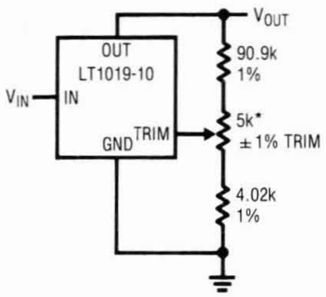
$\frac{dV_{OUT}}{dV^-} = \frac{15mV}{V}$

Figure 27. 10V Output, Trimmed to 10.24V


VOUT
OUT
LT1019-5
VIN
IN
GND
TRIM
41.2k
1%
5k*
±1% TRIM
4.02k
1%

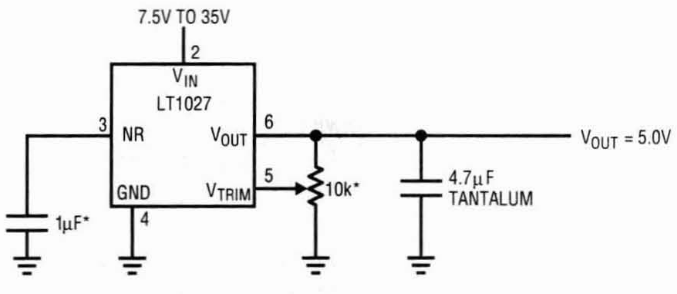
*LOW TC CERMET

Figure 28. 5V Output, Trimmed to 5.120V


VOUT
OUT
LT1019-10
VIN
IN
GND
TRIM
90.9k
1%
5k*
±1% TRIM
4.02k
1%

*LOW TC CERMET

Figure 29. 10V Output, Trimmed to 10.240V


7.5V TO 35V
2
VIN
LT1027
3
NR
VOUT
6
VOUT = 5.0V
5
GND
VTRIM
10k*
4.7μF
TANTALUM
1μF*
4

* NOISE REDUCTION CAP AND TRIM POTENTIOMETER OPTIONAL.

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Figure 30. 5V Output, Fast Settling, Trimmed Reference

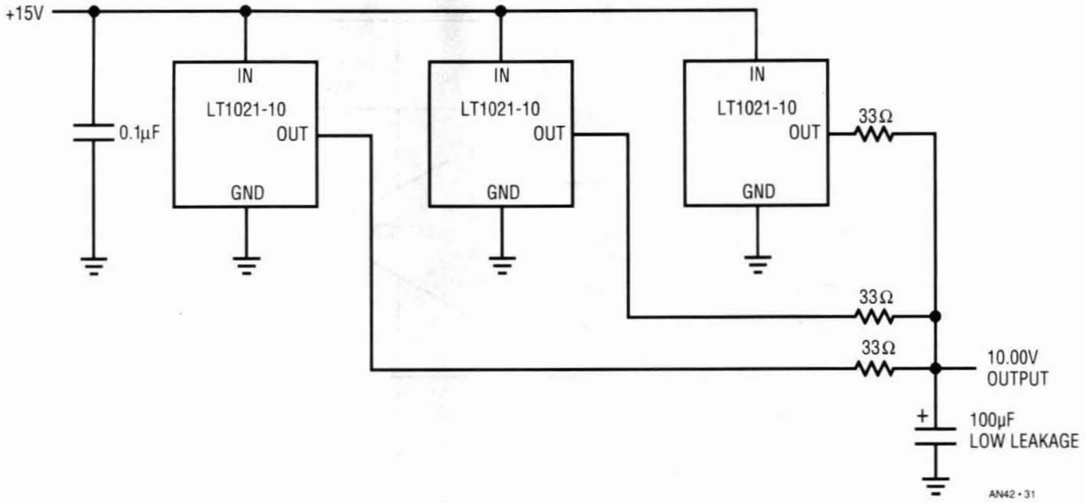
+15V
0.1µF
IN
LT1021-10
OUT
GND
IN
LT1021-10
OUT
GND
IN
LT1021-10
OUT
GND
33Ω
33Ω
33Ω
10.00V
OUTPUT
+
100µF
LOW LEAKAGE
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Figure 31. Low Noise Statistical Voltage Standard

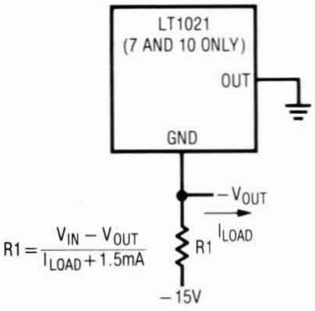
LT1021
(7 AND 10 ONLY)
OUT
GND
– V_OUT
I_LOAD
R1
R1 = (V_IN – V_OUT)/(I_LOAD + 1.5mA)
– 15V

Figure 32. Shunt Mode Operation of a Series Device (LT1021-7, -10)

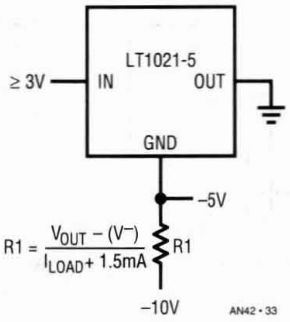
≥ 3V
IN
LT1021-5
OUT
GND
–5V
R1 = (V_OUT – (V⁻))/(I_LOAD + 1.5mA)
R1
–10V
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Figure 33. –5V Output Reference (LT1021-5)

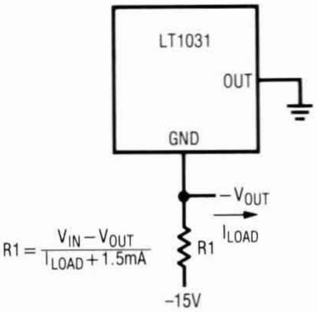
LT1031
OUT
GND
– V_OUT
I_LOAD
R1
R1 = (V_IN – V_OUT)/(I_LOAD + 1.5mA)
–15V

Figure 34. –10V Output for a Series Device

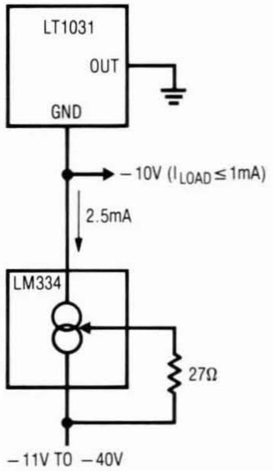
LT1031
OUT
GND
– 10V (I_LOAD ≤ 1mA)
2.5mA
LM334
27Ω
– 11V TO – 40V

Figure 35. –10V Output, Wide Input Range

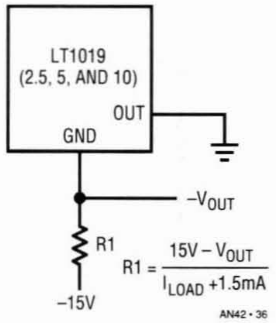
LT1019
(2.5, 5, AND 10)
OUT
GND
–V_OUT
R1
R1 = (15V – V_OUT)/(I_LOAD +1.5mA)
–15V
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Figure 36. Shunt Operation of a Series Device (LT1019-2.5, -5, -10)

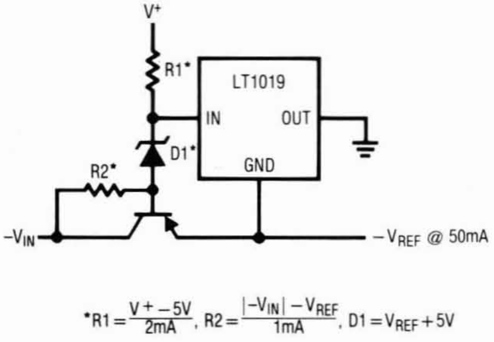
V⁺
R1*
LT1019
IN
OUT
GND
D1*
R2*
–V_IN
– V_REF @ 50mA
*R1 = (V + – 5V)/2mA, R2 = (|–V_IN| – V_REF)/1mA, D1 = V_REF + 5V

Figure 37. Current Boost Negative Reference (LT1019-2.5, -5, -10)

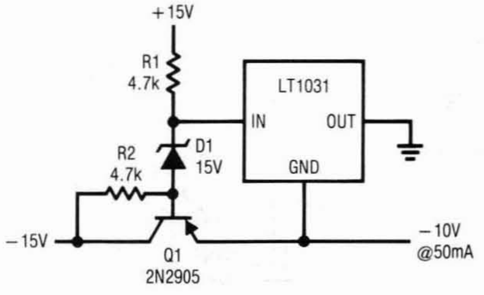
+15V
R1
4.7k
R2
4.7k
D1
15V
LT1031
IN
OUT
GND
–15V
Q1
2N2905
–10V
@50mA

Figure 38. –10V Output, Current Boosted Reference

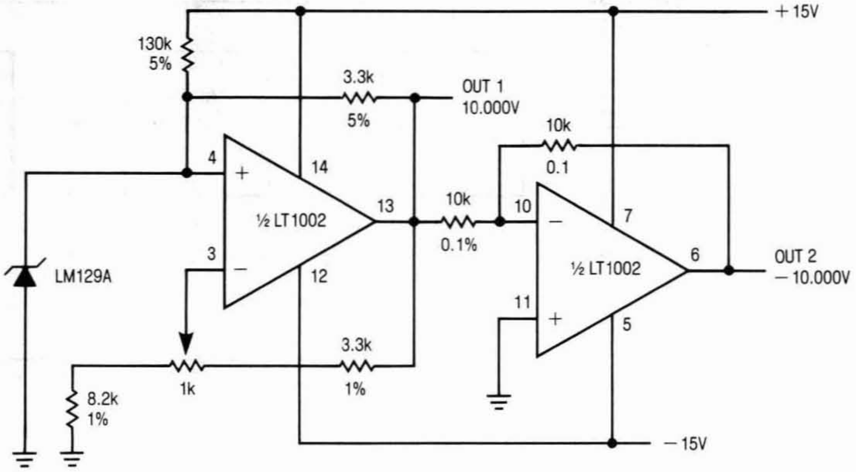
+15V
130k
5%
3.3k
5%
OUT 1
10.000V
10k
0.1
4
14
13
10k
0.1%
10
7
6
OUT 2
–10.000V
½ LT1002
½ LT1002
3
12
11
5
LM129A
3.3k
1%
1k
8.2k
1%
–15V

Figure 39. ±10V Output, Precision Reference

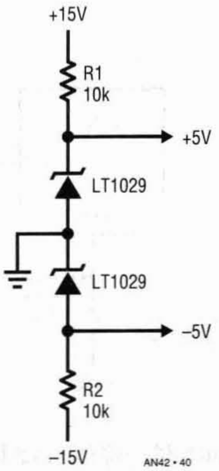
+15V
R1
10k
+5V
LT1029
LT1029
–5V
R2
10k
–15V
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Figure 40. ±5V Output Reference

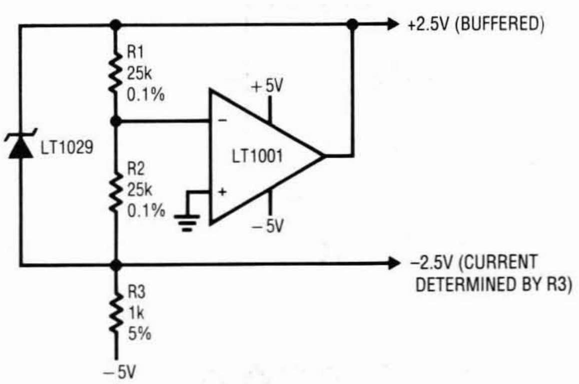
+2.5V (BUFFERED)
R1
25k
0.1%
+5V
LT1029
LT1001
R2
25k
0.1%
–5V
–2.5V (CURRENT
DETERMINED BY R3)
R3
1k
5%
–5V

Figure 41. ±2.5V Output Reference

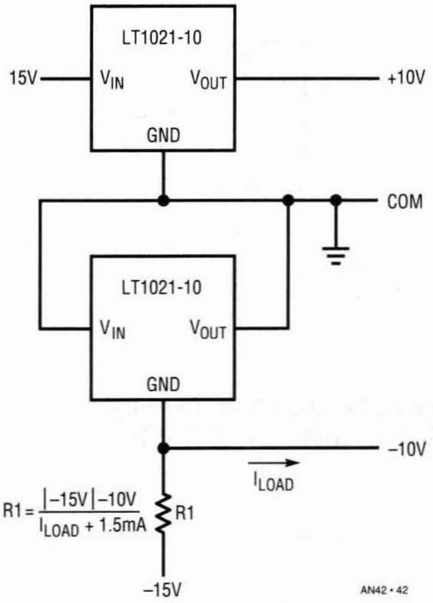
LT1021-10
15V
V_{IN}
V_{OUT}
+10V
GND
COM
LT1021-10
V_{IN}
V_{OUT}
GND
–10V
I_{LOAD}
$R1 = \frac{|-15V|-10V}{I_{LOAD} + 1.5mA}$
R1
–15V
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Figure 42. ±10V Output Reference

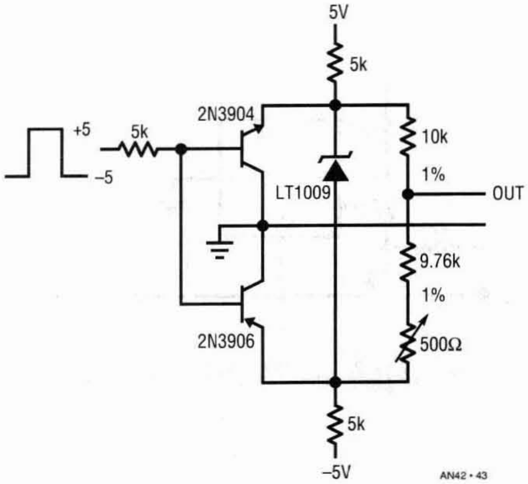
5V
5k
+5
–5
5k
2N3904
10k
1%
LT1009
OUT
9.76k
1%
2N3906
500Ω
5k
–5V
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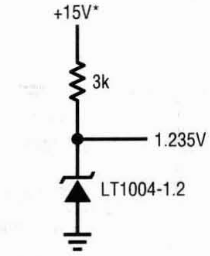
Figure 43. ±1.25V Output, Logic Programmable Reference


+15V*
3k
1.235V
LT1004-1.2

*OUTPUT REGULATES
DOWN TO 1.285V
FOR $I_{OUT} = 0$

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Figure 44. 1.2V Output, Micropower Reference from 1.5V Battery

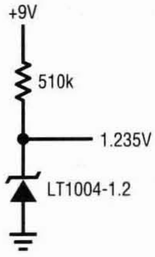
+9V
510k
1.235V
LT1004-1.2
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Figure 45. 1.2V Output, Micropower Reference from 9V Battery

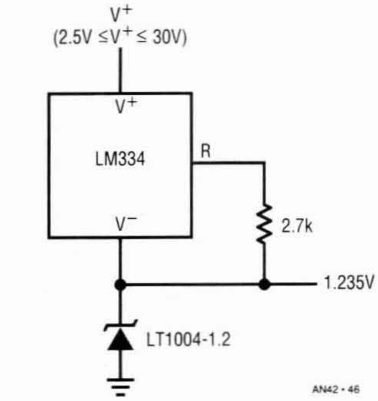
V+
(2.5V ≤ V+ ≤ 30V)
V+
LM334
R
V−
2.7k
1.235V
LT1004-1.2
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Figure 46. 1.2V Output, Micropower Reference with Wide Input Voltage Range

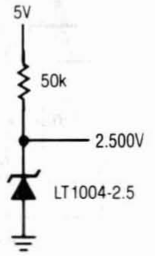
5V
50k
2.500V
LT1004-2.5

Figure 47. 2.5V Output, Micropower Reference

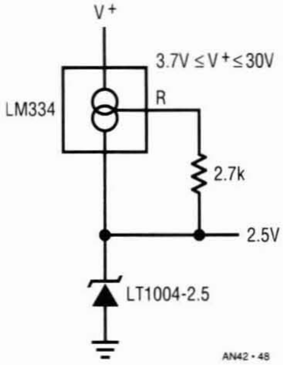
V+
3.7V ≤ V+ ≤ 30V
LM334
R
2.7k
2.5V
LT1004-2.5
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Figure 48. 2.5V Output, Micropower Reference with Wide Input Voltage Range

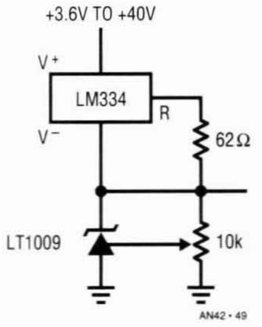
+3.6V TO +40V
V+
LM334
R
V−
62Ω
LT1009
10k
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Figure 49. 2.5V Output with Wide Input Range

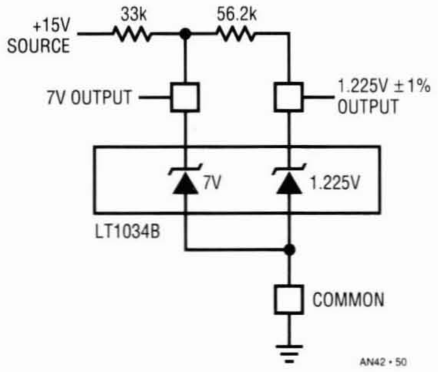
+15V
SOURCE
33k
56.2k
7V OUTPUT
1.225V ±1%
OUTPUT
7V
1.225V
LT1034B
COMMON
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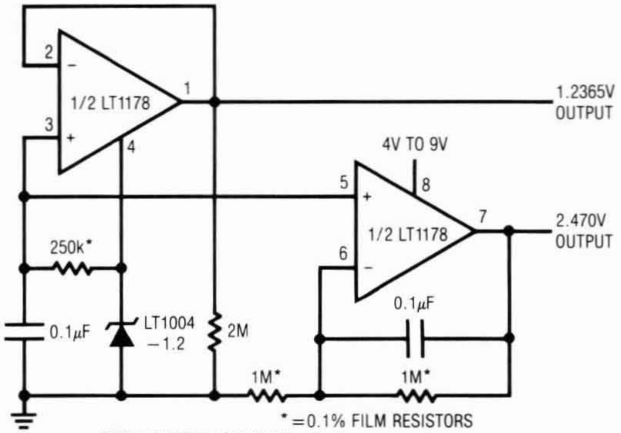
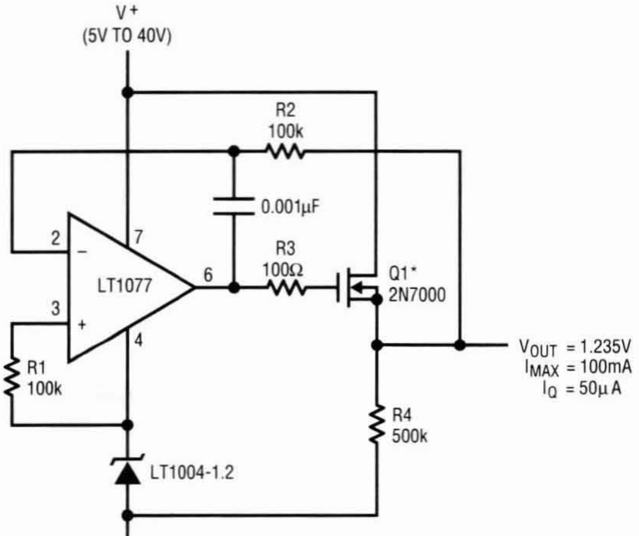
Figure 50. +1.2V, +7V Output, Pre-Regulated Reference


2
−
1/2 LT1178
1
3
+
4
1.2365V
OUTPUT
4V TO 9V
5
+
8
1/2 LT1178
7
2.470V
OUTPUT
6
−
250k*
0.1μF
LT1004
−1.2
2M
0.1μF
1M*
1M*

* = 0.1% FILM RESISTORS
TOTAL BATTERY CURRENT = 28μA
OUTPUT ACCURACY = ±0.4% MAX
TEMPERATURE COEFFICIENT = 20ppm/°C
LOAD REGULATION = 25ppm/mA, I_L ≤ 5mA, V+ ≥ 5V
LINE REGULATION = 10ppm/V

Figure 51. +1.227V, +2.45V Output, Self-Buffered, Micropower Reference


V+
(5V TO 40V)
R2
100k
0.001μF
R3
100Ω
Q1*
2N7000
2
−
7
LT1077
6
3
+
4
R1
100k
R4
500k
LT1004-1.2
V_{OUT} = 1.235V
I_{MAX} = 100mA
I_Q = 50μA

* USE HEATSINK IF HIGH POWER DISSIPATION IS REQUIRED

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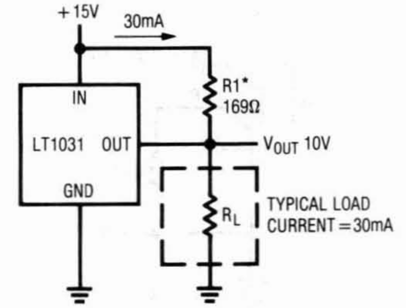
Figure 52. 1.24V Output, Micropower, Current Boosted Reference (100mA)


+15V
30mA
IN
LT1031
OUT
GND
R1*
169Ω
V_{OUT} 10V
R_L
TYPICAL LOAD
CURRENT = 30mA

*SELECT R1 TO DELIVER TYPICAL LOAD CURRENT. LT1031 WILL THEN SOURCE OR SINK AS NECESSARY TO MAINTAIN PROPER OUTPUT. DO NOT REMOVE LOAD AS OUTPUT WILL BE DRIVEN UNREGULATED HIGH. LINE REGULATION IS DEGRADED IN THIS APPLICATION.

Figure 53. 10V Output with $V_{IN}–V_{OUT}$ Shunt Resistor for Greater Current

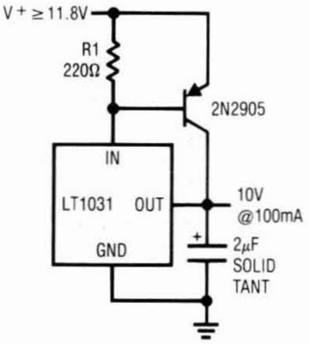
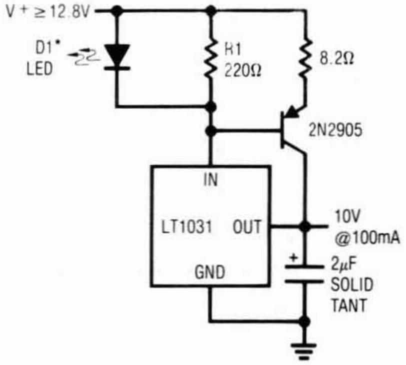
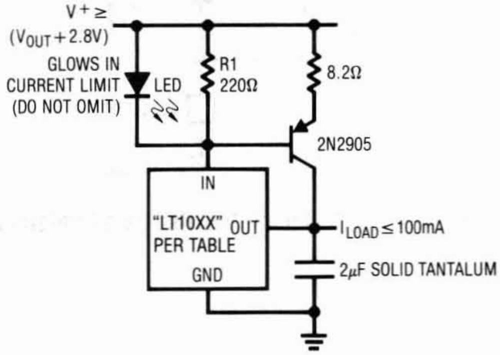

V+ ≥ 11.8V
R1
220Ω
2N2905
IN
LT1031
OUT
GND
10V
@100mA
+
2μF
SOLID
TANT

Figure 54. 10V Output with External PNP for Boosted Output (100mA)


V+ ≥ 12.8V
D1*
LED
R1
220Ω
8.2Ω
2N2905
IN
LT1031
OUT
GND
10V
@100mA
+
2μF
SOLID
TANT

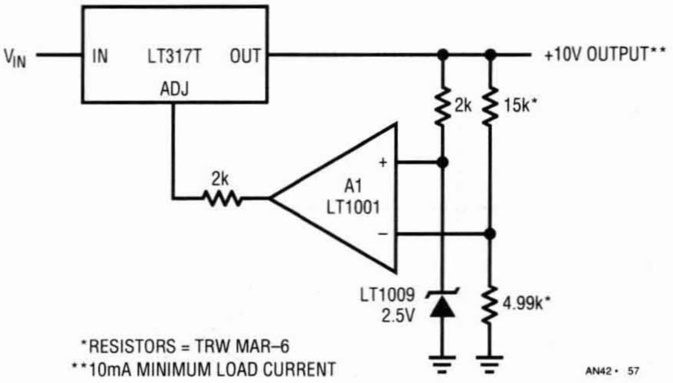
*GLOWS IN CURRENT LIMIT. DO NOT OMIT.

Figure 55. 10V Boosted Output with Current Limit (100mA)


V+ ≥
(V_{OUT} + 2.8V)
GLOWS IN
CURRENT LIMIT
(DO NOT OMIT)
LED
R1
220Ω
8.2Ω
2N2905
IN
"LT10XX"
PER TABLE
OUT
GND
I_{LOAD} ≤ 100mA
2μF SOLID TANTALUM

DEVICE	V_{OUT}
LT1019-2.5	2.5V
LT1019-5 LT1021-5 LT1027	5V
LT1021-7	7V
LT1019-10 LT1021-10	10V

Figure 56. Series Reference with PNP Boost


V_{IN}
IN
LT317T
OUT
ADJ
+10V OUTPUT**
2k
15k*
2k
+
A1
LT1001
–
LT1009
2.5V
4.99k*
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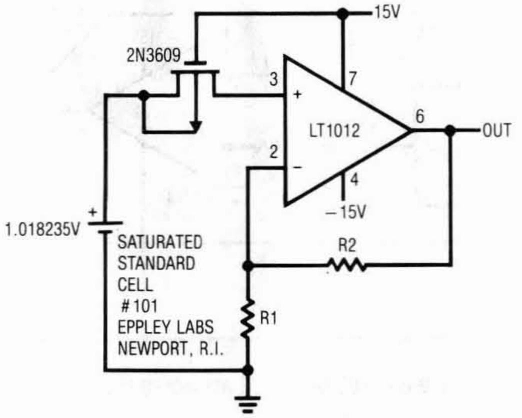
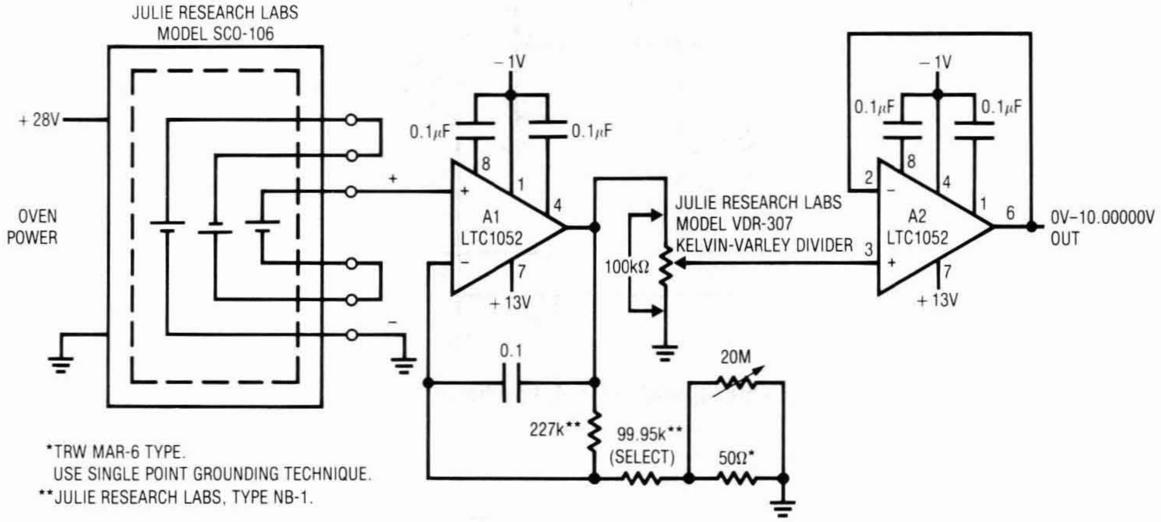
*RESISTORS = TRW MAR-6
**10mA MINIMUM LOAD CURRENT

Figure 57. Precision High Current Reference (1.5A)


15V
2N3609
3
+
7
LT1012
6
OUT
2
–
4
–15V
+
1.018235V
SATURATED
STANDARD
CELL
# 101
EPPLEY LABS
NEWPORT, R.I.
R2
R1

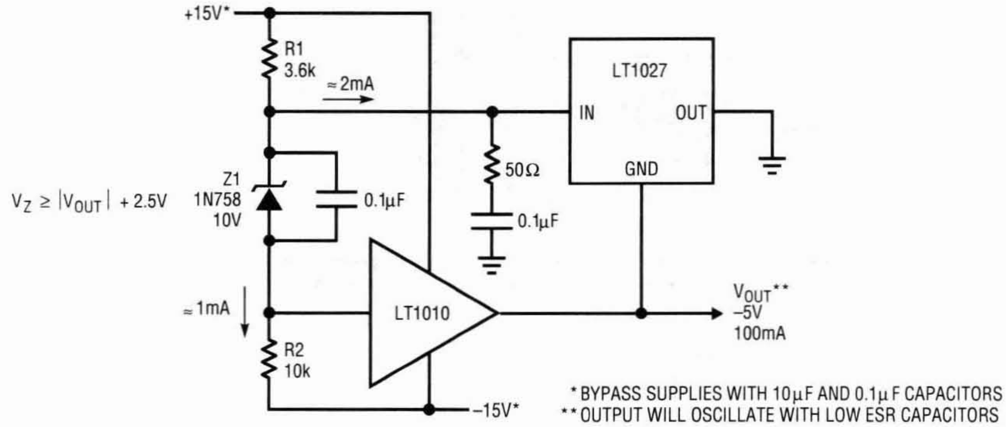
THE TYPICAL 30pA BIAS CURRENT OF THE LT1012 WILL DEGRADE THE STANDARD CELL BY ONLY 1ppm/YEAR. NOISE IS A FRACTION OF A ppm. UNPROTECTED GATE MOSFET ISOLATES STANDARD CELL ON POWER DOWN.

Figure 58. Buffered Standard Cell


JULIE RESEARCH LABS
MODEL SCO-106
+28V
OVEN
POWER
+
–
–1V
0.1μF
0.1μF
8
1
4
A1
LTC1052
7
+13V
JULIE RESEARCH LABS
MODEL VDR-307
KELVIN-VARLEY DIVIDER
100kΩ
–1V
0.1μF
0.1μF
2
8
4
A2
LTC1052
1
6
3
7
+13V
0V–10.00000V
OUT
0.1
227k**
99.95k**
(SELECT)
20M
50Ω*

*TRW MAR-6 TYPE.
USE SINGLE POINT GROUNDING TECHNIQUE.
**JULIE RESEARCH LABS, TYPE NB-1.

Figure 59. Standard Grade Variable Voltage Reference


+15V*
R1
3.6k
≈2mA
LT1027
IN
OUT
GND
50Ω
0.1μF
$V_Z \geq |V_{OUT}| + 2.5V$
Z1
1N758
10V
0.1μF
≈1mA
LT1010
R2
10k
–15V*
V_{OUT}**
–5V
100mA

* BYPASS SUPPLIES WITH 10μF AND 0.1μF CAPACITORS
** OUTPUT WILL OSCILLATE WITH LOW ESR CAPACITORS

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Figure 60. –5V Output, Current Boosted Negative Reference with Overload Protection

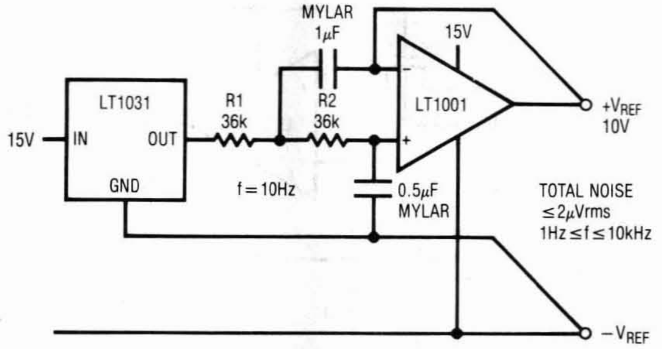
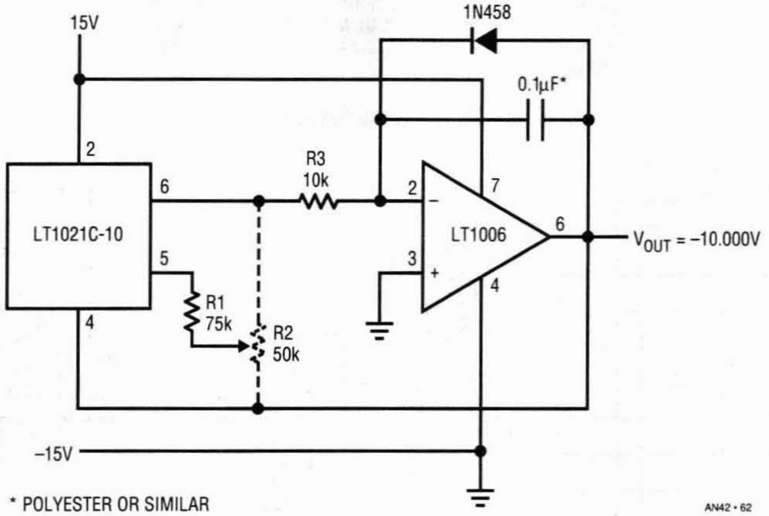

MYLAR
1μF
15V
LT1031
IN
OUT
GND
15V
R1
36k
R2
36k
LT1001
+V_{REF}
10V
f = 10Hz
0.5μF
MYLAR
TOTAL NOISE
≤ 2μVrms
1Hz ≤ f ≤ 10kHz
– V_{REF}

Figure 61. 10V Output, Low Noise Reference


15V
1N458
0.1μF*
2
LT1021C-10
6
5
4
R3
10k
2
3
7
LT1006
6
4
V_{OUT} = –10.000V
R1
75k
R2
50k
–15V
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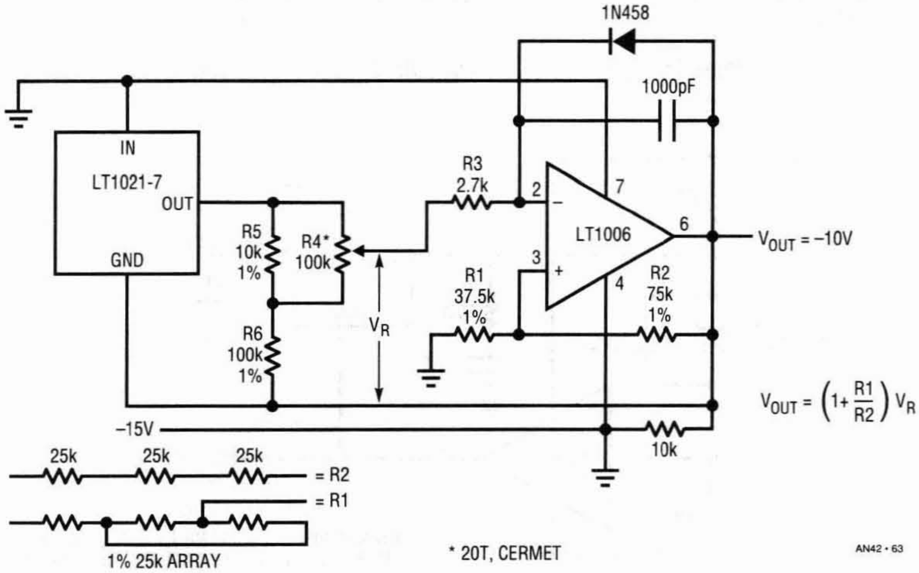
* POLYESTER OR SIMILAR

Figure 62. –10V Output, Low Noise Reference


1N458
1000pF
IN
LT1021-7
OUT
GND
R3
2.7k
2
7
LT1006
6
3
4
V_{OUT} = –10V
R5
10k
1%
R4*
100k
R1
37.5k
1%
R2
75k
1%
V_R
R6
100k
1%
$V_{OUT} = \left(1 + \frac{R1}{R2}\right) V_R$
–15V
10k
25k
25k
25k
= R2
= R1
1% 25k ARRAY
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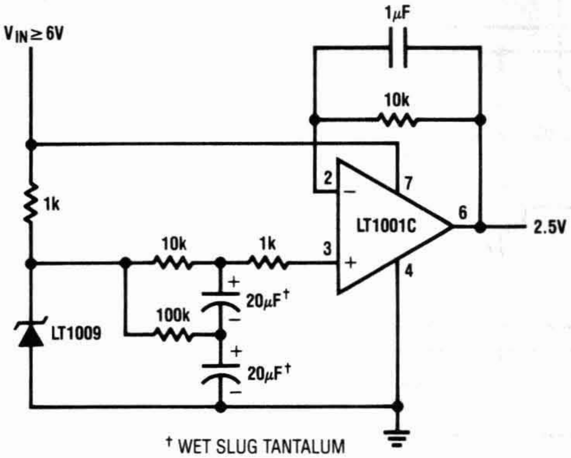
* 20T, CERMET

Figure 63. Single Supply, –10V Output, Trimmed Low Noise, Low TC Reference


$V_{IN} \geq 6V$
1μF
10k
2
7
LT1001C
6
2.5V
3
4
1k
10k
1k
20μF†
100k
LT1009
20μF†

† WET SLUG TANTALUM

Figure 64. 2.5V Output, Low Noise Reference

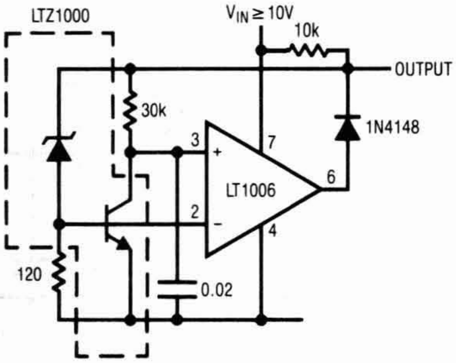
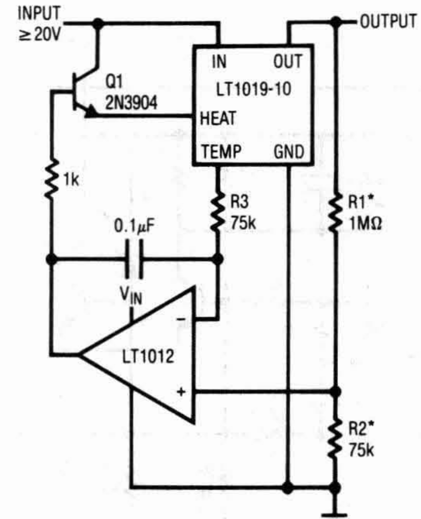
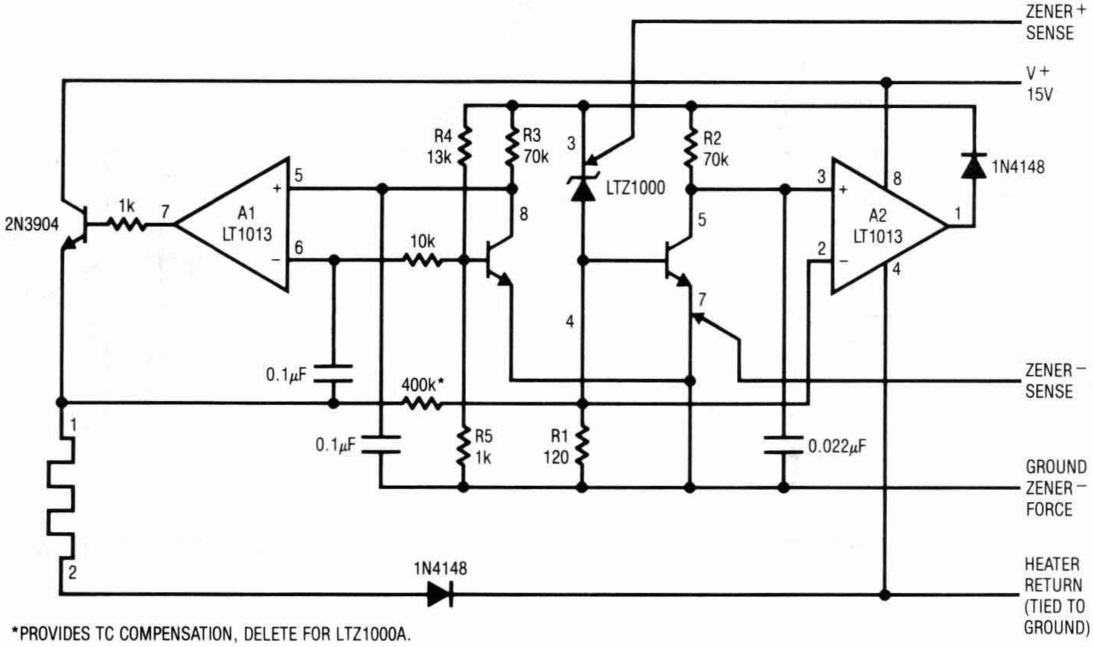

LTZ1000
$V_{IN} \geq 10V$
10k
OUTPUT
30k
1N4148
3
7
LT1006
6
2
4
120
0.02

Figure 65. 7V Output, Low Noise, Low Drift Reference


INPUT
≥ 20V
OUTPUT
Q1
2N3904
IN
OUT
LT1019-10
HEAT
TEMP
GND
1k
R3
75k
R1*
1MΩ
0.1μF
V_{IN}
LT1012
R2*
75k

*SELECT FOR DESIRED TEMPERATURE. VALUES GIVEN SET CHIP TEMPERATURE TO ≃70°C WITH $V_{OUT} = 10V$.

Figure 66. 10V Output, Temperature Stabilized Reference


ZENER + SENSE
V+ 15V
R4 13k
R3 70k
R2 70k
3
LTZ1000
1N4148
2N3904
1k
7
A1 LT1013
5
6
10k
8
5
3
8
A2 LT1013
1
2
4
7
4
0.1μF
400k*
0.1μF
R5 1k
R1 120
0.022μF
ZENER − SENSE
GROUND ZENER − FORCE
1
2
1N4148
HEATER RETURN (TIED TO GROUND)

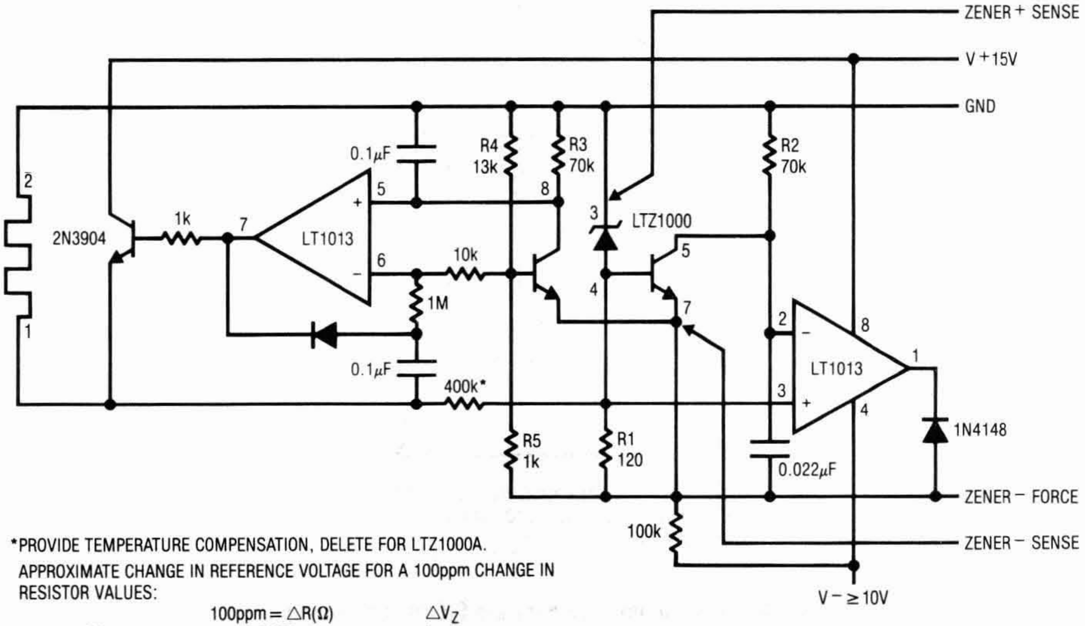
*PROVIDES TC COMPENSATION, DELETE FOR LTZ1000A.

APPROXIMATE CHANGE IN REFERENCE VOLTAGE FOR A 100ppm (0.01%) CHANGE IN RESISTOR VALUES:

	△R(Ω)	△V_Z
R1	0.012Ω	1ppm
R2	7Ω	0.3ppm
R3	7Ω	0.2ppm
R4/R5 RATIO	△R = 0.01%	1ppm

BOTH A1 AND A2 CONTRIBUTE LESS THAN 2μV OF OUTPUT DRIFT OVER A 50°C RANGE.

Figure 67. Low Noise, Ultra Low Drift, Long Term Stable 7V Positive Reference


ZENER + SENSE
V +15V
GND
2
1
2N3904
1k
7
0.1μF
LT1013
5
6
10k
1M
0.1μF
400k*
R4 13k
R3 70k
8
3
LTZ1000
5
4
7
R2 70k
2
3
8
LT1013
1
4
1N4148
R5 1k
R1 120
0.022μF
ZENER − FORCE
100k
ZENER − SENSE
V − ≥ 10V

*PROVIDE TEMPERATURE COMPENSATION, DELETE FOR LTZ1000A.

APPROXIMATE CHANGE IN REFERENCE VOLTAGE FOR A 100ppm CHANGE IN RESISTOR VALUES:

	100ppm = △R(Ω)	△V_Z
R1	0.012Ω	1ppm
R2	7Ω	0.3ppm
R3	7Ω	0.2ppm
R4/R5 RATIO	△R = 0.01%	1ppm

BOTH A1 AND A2 CONTRIBUTE LESS THAN 2μV OF OUTPUT DRIFT OVER A 50°C RANGE.

Figure 68. Low Noise, Ultra Low Drift, Long Term Stable Negative Voltage Reference

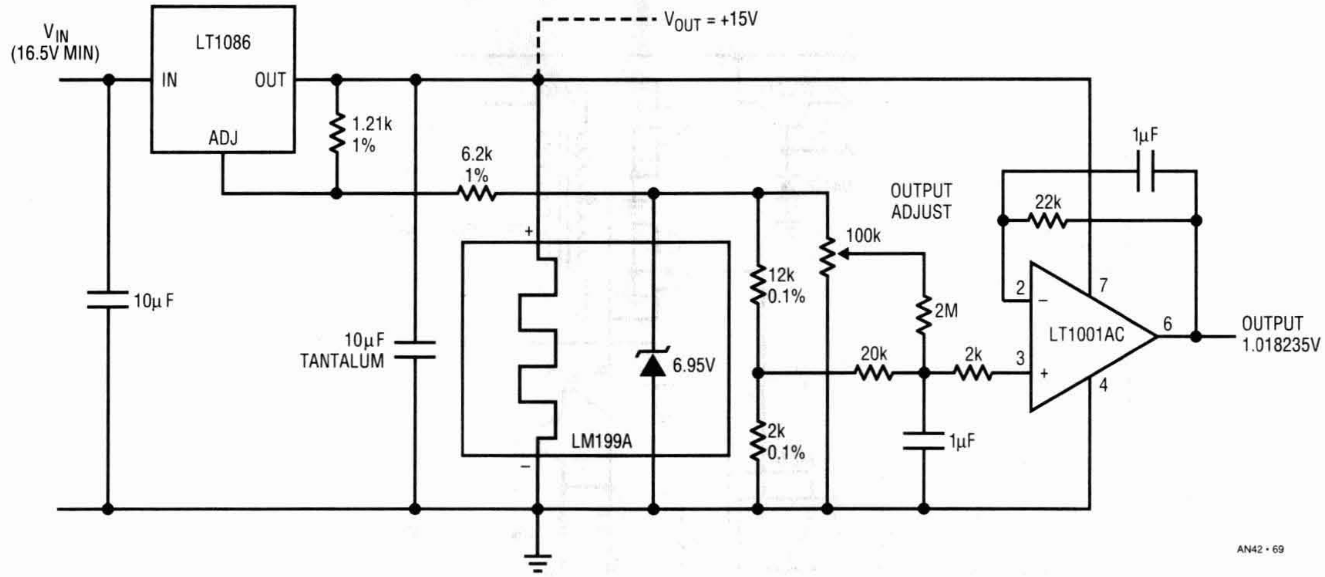

V_IN
(16.5V MIN)
LT1086
IN
OUT
ADJ
V_OUT = +15V
1.21k
1%
6.2k
1%
10μF
10μF
TANTALUM
LM199A
6.95V
+
–
12k
0.1%
2k
0.1%
100k
OUTPUT
ADJUST
2M
20k
2k
1μF
22k
1μF
LT1001AC
2
3
7
4
6
OUTPUT
1.018235V
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Figure 69. Buffered Standard Cell Replacement

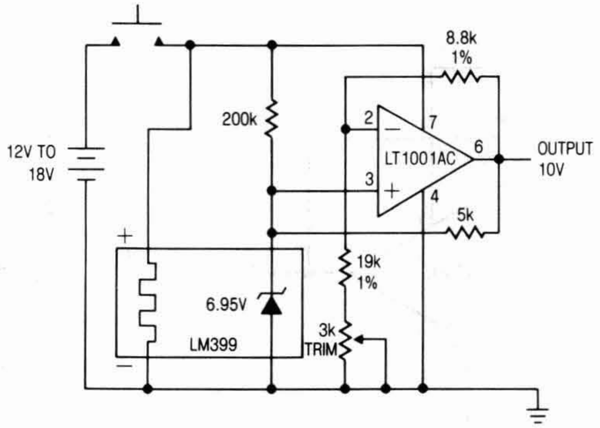
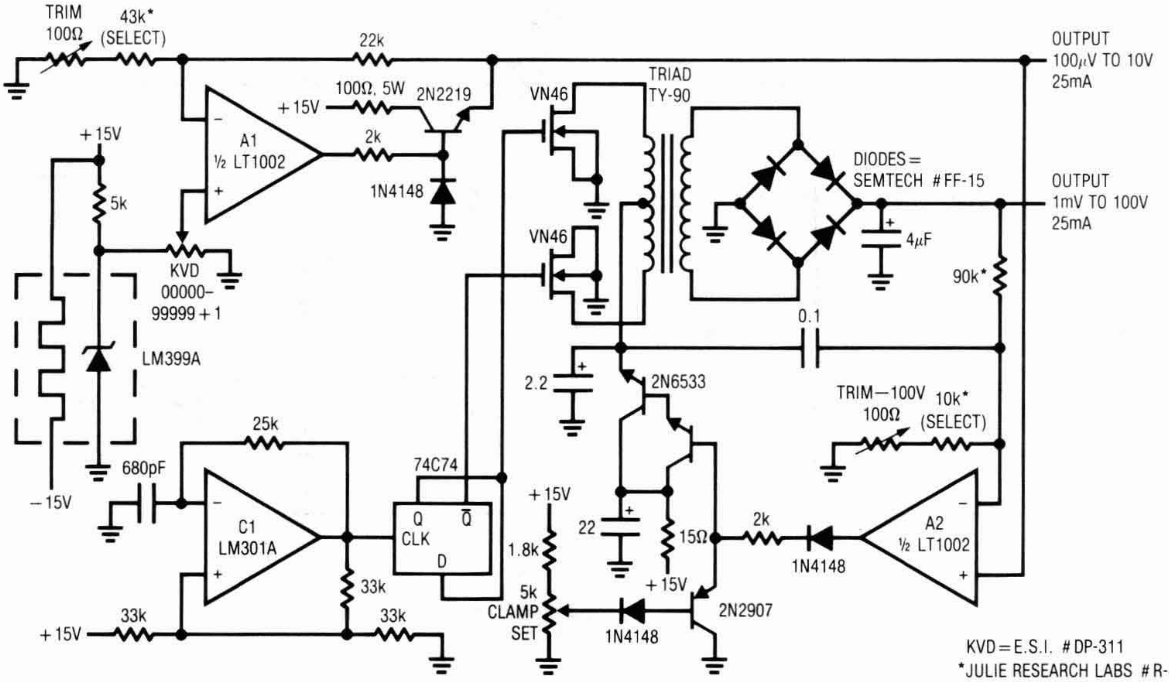

12V TO
18V
200k
8.8k
1%
LT1001AC
2
3
7
4
6
OUTPUT
10V
5k
19k
1%
3k
TRIM
6.95V
LM399
+
–

Figure 70. 10V Output, Self-Biased Temperature Stabilized Reference


TRIM
100Ω
43k*
(SELECT)
22k
OUTPUT
100μV TO 10V
25mA
+15V
100Ω, 5W
2N2219
VN46
TRIAD
TY-90
A1
½ LT1002
2k
1N4148
DIODES =
SEMTECH #FF-15
OUTPUT
1mV TO 100V
25mA
5k
VN46
4μF
KVD
00000–
99999 + 1
90k*
LM399A
0.1
2.2
2N6533
TRIM—100V
100Ω
10k*
(SELECT)
25k
74C74
−15V
680pF
+15V
C1
LM301A
Q
Q̄
CLK
D
1.8k
22
15Ω
2k
1N4148
A2
½ LT1002
33k
5k
CLAMP
SET
+15V
2N2907
+15V
33k
33k
1N4148

KVD = E.S.I. #DP-311
*JULIE RESEARCH LABS #R-44

Figure 71. Ultra-Precision Variable Voltage Reference

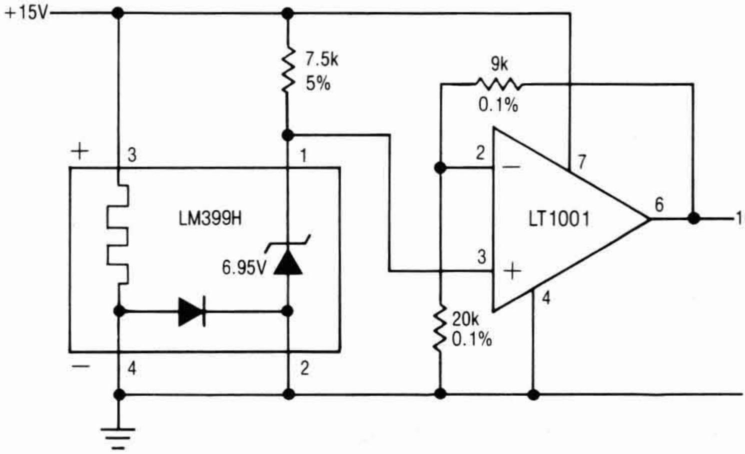
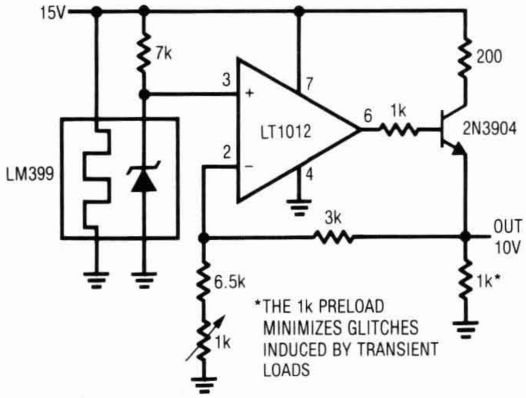

+15V
7.5k
5%
9k
0.1%
+
3
1
2
7
LM399H
LT1001
6
10V
6.95V
3
4
−
4
2
20k
0.1%

Figure 72. 10V Output, Temperature Stabilized Reference


15V
7k
200
3
7
LT1012
6
1k
2N3904
2
4
LM399
3k
OUT
10V
6.5k
1k*
1k

*THE 1k PRELOAD
MINIMIZES GLITCHES
INDUCED BY TRANSIENT
LOADS

Figure 73. Temperature Stabilized 10V Buffered Reference

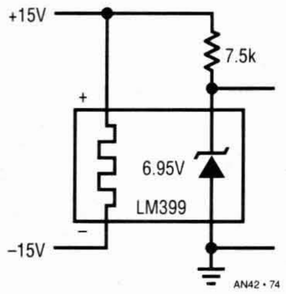

+15V
7.5k
+
6.95V
LM399
–
–15V
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Figure 74. 6.95V Output, Temperature Stabilized Reference

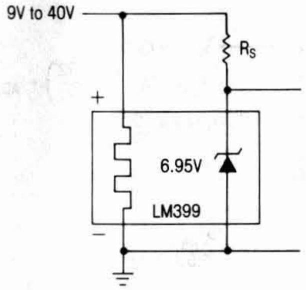

9V to 40V
R_S
+
6.95V
LM399
–

Figure 75. 6.95V Output, Temperature Stabilized Reference

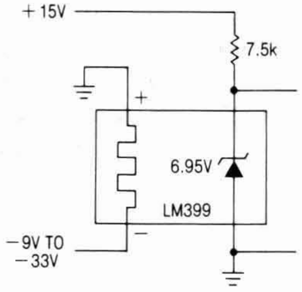
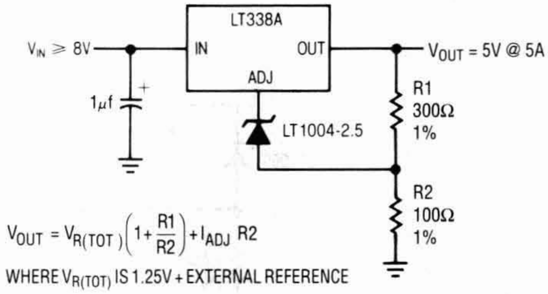

+ 15V
7.5k
+
6.95V
LM399
–
– 9V TO
– 33V

Figure 76. 6.95V Output, Temperature Stabilized Reference


LT338A
$V_{IN} \geq 8V$
IN
OUT
ADJ
V_{OUT} = 5V @ 5A
1μf
+
LT1004-2.5
R1
300Ω
1%
R2
100Ω
1%

$$V_{OUT} = V_{R(TOT)}\left(1 + \frac{R1}{R2}\right) + I_{ADJ}\ R2$$

WHERE $V_{R(TOT)}$ IS 1.25V + EXTERNAL REFERENCE

Figure 77. Simple High Stability Regulator

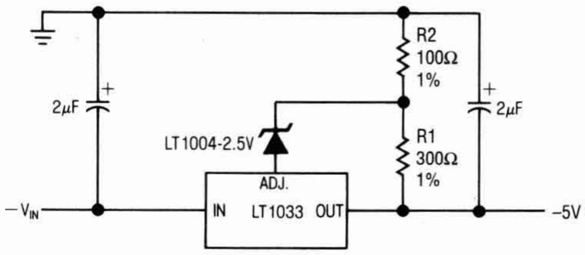
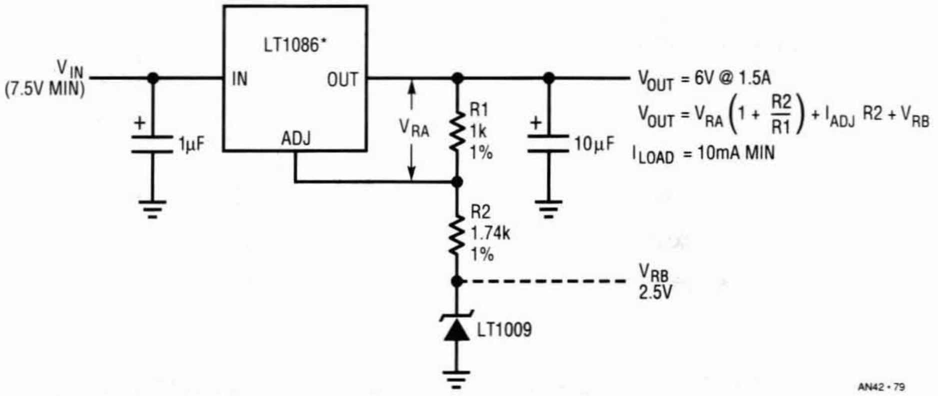

R2
100Ω
1%
2μF
+
LT1004-2.5V
R1
300Ω
1%
+
2μF
ADJ.
$-V_{IN}$
IN
LT1033
OUT
–5V

Figure 78. High Stability Negative Regulator


LT1086*
V_IN (7.5V MIN)
IN
OUT
ADJ
1µF
V_RA
R1 1k 1%
10µF
R2 1.74k 1%
LT1009
V_OUT = 6V @ 1.5A
V_OUT = V_RA (1 + R2/R1) + I_ADJ R2 + V_RB
I_LOAD = 10mA MIN
V_RB 2.5V
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DEVICE	FEATURES
LT1086	1.5A, Low Dropout
LT1085	3A, Low Dropout
LT1084	5A, Low Dropout
LT1083	7.5A, Low Dropout
LT317A	1.5A
LT350	3A
LT338A	5A
LT1038	10A

Figure 79. Regulator with Reference

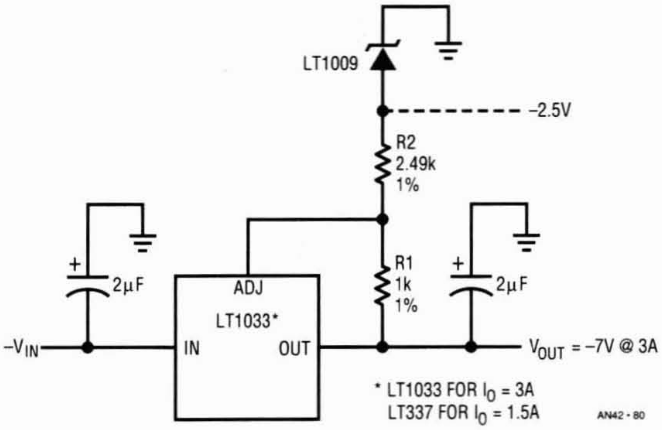
LT1009
–2.5V
R2 2.49k 1%
R1 1k 1%
2µF
2µF
ADJ
LT1033*
IN
OUT
–V_IN
V_OUT = –7V @ 3A
* LT1033 FOR I_O = 3A
LT337 FOR I_O = 1.5A
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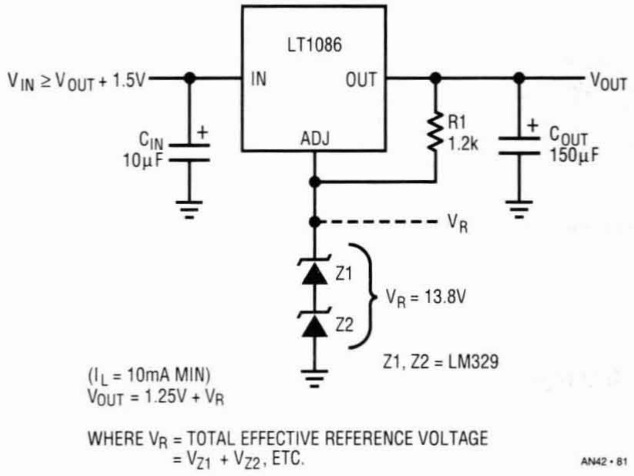
Figure 80. Negative Output Regulator with Reference


LT1086
V_IN ≥ V_OUT + 1.5V
IN
OUT
ADJ
V_OUT
C_IN 10μF
R1 1.2k
C_OUT 150μF
V_R
Z1
Z2
V_R = 13.8V
Z1, Z2 = LM329
(I_L = 10mA MIN)
V_OUT = 1.25V + V_R
WHERE V_R = TOTAL EFFECTIVE REFERENCE VOLTAGE = V_Z1 + V_Z2, ETC.
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Z1/Z2	V_Z	V_R	V_{OUT}
LT1034	1.225	1.225	2.475
LT1004	1.235	1.235	2.485
LT1009	2.500	2.500	3.750
LT1034 + LT1009	1.225 + 2.5	3.725	4.975
LT1004 + LT1009	1.235 + 2.5	3.735	4.985
LT1029	5	5	6.250
LT1034 + LT1029	6.225	6.225	7.475
LT1004 + LT1029	6.235	6.235	7.485
LM329	6.9	6.9	8.150
LT1009 + LT1029	2.5 + 5.0	7.500	8.750
LT1034 + LM329	1.225 + 6.9	8.125	9.375
LT1004 + LM329	1.235 + 6.9	8.135	9.385
LT1009 + LM329	2.5 + 6.9	9.400	10.650
2 × LT1029	5 + 5	10.000	11.250
LT1029 + LM329	5 + 6.9	11.900	13.250
2 × LM329	6.9 + 6.9	13.800	15.050

Figure 81. Simple Stacked Reference/Regulator

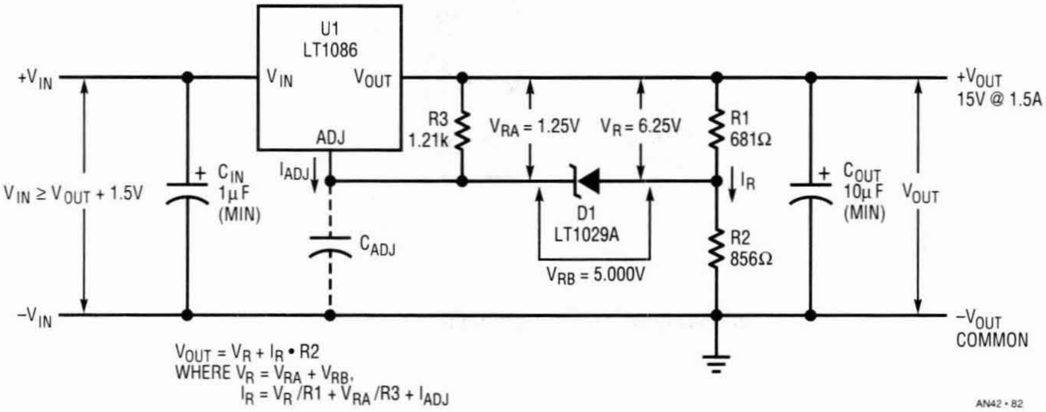
U1
LT1086
+V_IN
V_IN
V_OUT
ADJ
R3 1.21k
V_RA = 1.25V
V_R = 6.25V
R1 681Ω
I_R
+V_OUT 15V @ 1.5A
V_IN ≥ V_OUT + 1.5V
C_IN 1μF (MIN)
I_ADJ
C_ADJ
D1 LT1029A
V_RB = 5.000V
R2 856Ω
C_OUT 10μF (MIN)
V_OUT
–V_IN
–V_OUT COMMON
V_OUT = V_R + I_R • R2
WHERE V_R = V_RA + V_RB,
I_R = V_R/R1 + V_RA/R3 + I_ADJ
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Figure 82. Programmable High Stability Regulator

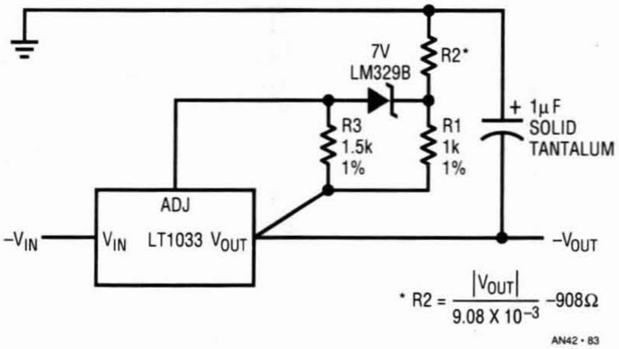
7V
LM329B
R2*
R3
1.5k
1%
R1
1k
1%
+ 1μF
SOLID
TANTALUM
ADJ
$-V_{IN}$
V_{IN}
LT1033
V_{OUT}
$-V_{OUT}$
$* R2 = \frac{|V_{OUT}|}{9.08 \times 10^{-3}} - 908\Omega$
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Figure 83. Programmable Negative Output High Stability Regulator

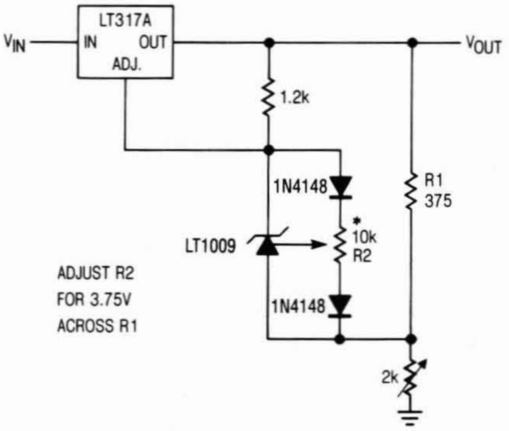

LT317A
V_{IN}
IN
OUT
ADJ.
V_{OUT}
1.2k
1N4148
R1
375
LT1009
*
10k
R2
1N4148
ADJUST R2
FOR 3.75V
ACROSS R1
2k

Figure 84. Low Temperature Coefficient Regulator

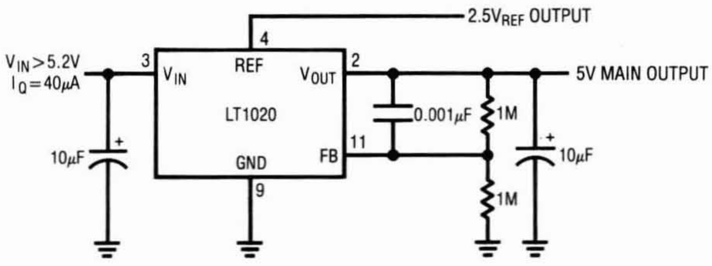

2.5V_REF OUTPUT
$V_{IN} > 5.2V$
$I_Q = 40\mu A$
3
V_{IN}
4
REF
LT1020
GND
9
V_{OUT}
2
FB
11
0.001μF
1M
1M
5V MAIN OUTPUT
10μF
+
10μF
+

Figure 85. 5V Output, Low Dropout, Micropower Regulator with 2.5V Reference

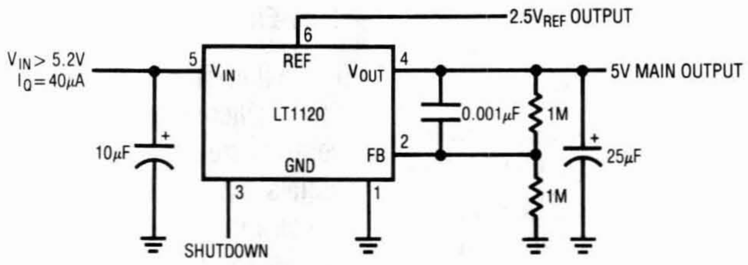
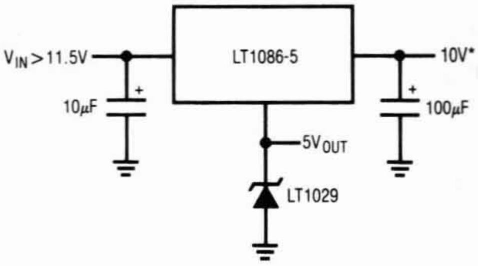

2.5V_REF OUTPUT
6
REF
V_IN > 5.2V
I_Q = 40μA
5
V_IN
V_OUT
4
5V MAIN OUTPUT
LT1120
0.001μF
1M
10μF
2
FB
GND
25μF
3
1
1M
SHUTDOWN

Figure 86. 5V Output, Low Dropout, Micropower Regulator with 2.5V Reference and Shutdown


V_IN > 11.5V
LT1086-5
10V*
10μF
100μF
5V_OUT
LT1029

* 10mA MINIMUM LOAD CURRENT

Figure 87. High Current Regulator with Reference

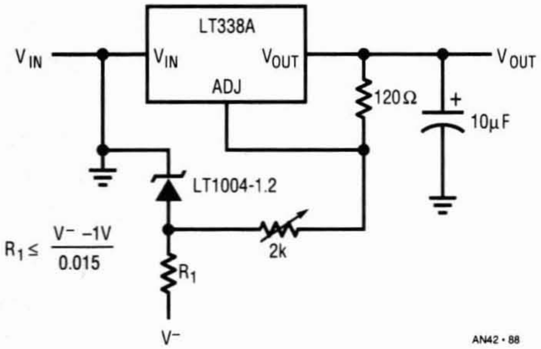

LT338A
V_IN
V_IN
V_OUT
V_OUT
ADJ
120Ω
10μF
LT1004-1.2
R_1 ≤ (V⁻ −1V)/0.015
2k
R_1
V⁻
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Figure 88. High Current Variable Output Supply

APPENDIX A

Precision Resistor Selection

Resistors are commonly used in precision linear circuits. Common precision resistor technologies include thin-film, thick-film, metal foil, and wirewound. Selecting the appropriate resistor type for a given application requires some understanding of the capabilities of the various devices available.

In many applications resistor selection depends on resistance value, absolute accuracy, and power dissipation. However, when designing precision linear circuits other performance parameters usually must be considered. These include temperature coefficient, load life stability, and voltage coefficient. The relative importance of any parameter depends on the particular application. Table A1 lists characteristics of different resistor types. Because individual processes vary, characteristics for the same resistor technology vary between manufacturers.

Package type can significantly influence stability. Some packages more effectively protect the resistive element from stresses due to handling, packaging, insertion, and lead forming. Also, manufacturing conditions including solder baths, cleaning solutions, and humidity can cause shifts in a resistor's value. Common package choices include conformal coating, molded and hermetic types. Conformal coated parts are the most common types in semi-precision applications. Hermetic sealing offers substantial stability improvements, regardless of resistor technology. Hermetically sealed metal cases also provide electrostatic shielding and isolation from humidity and other environmental effects.

Ultra-stable time and temperature characteristics become an issue when circuitry must hold calibration over extended ranges of time and temperature. In these applications an oil filled package may be required. The oil integrates ambient temperature variations, preventing thermal gradients across the resistor.

Various technologies available offer a spectrum of price-performance tradeoffs. Because of this, a summary of resistor types is useful.

Thin-Film

In the thin-film process, typically metal film, Nickel-Chromium (Nichrome) or Tantalum-Nitride is deposited on a ceramic substrate by evaporation or sputtering techniques. The sputtering process is preferred since it produces a more stable device. The 750Å-1500Å film can be applied to either a planar substrate or a ceramic cylindrical core. Resistor networks use the planar substrate with discrete thin-film resistors utilizing the familiar cylindrical shape. Nichrome parts have typical temperature coefficient of resistance (TCR) of 25ppm/°C for a planar substrate and 50ppm/°C for a ceramic core substrate. Tantalum-Nitride resistors tend to be slightly higher.

Bulk-Metal Foil

Bulk-metal foil resistors are made with a Nickel-Chromium alloy that is cemented to a planar ceramic substrate. The Nichrome alloy, substrate, and adhesive material are carefully balanced to achieve an overall low temperature sensitivity. The bulk-metal foil's 25,000Å thickness is significantly less susceptible to humidity than thin-film types.

Bulk-metal foil resistors are ultra-precision components. Generally, they offer tighter tolerance, better stability, and lower TCR's than their thin-film counterparts. Their high stability and uniformity makes them a good candidate for precision networks. The networks use hybrid type construction and offer extraordinary ratio stabilities (0.5ppm/°C). Unfortunately, bulk-metal technologies may cost two to five times that of film resistors.

Wirewound

Wirewound resistors are usually made by winding resistive wire of a specific diameter and characteristic around a core or card. Performance depends on the alloy used, wire lengths, diameter, and annealing process. Wirewound resistors can be ultra-precision components and are best suited in applications that require absolute accuracy, stability, power, or low resistance value. Wirewounds have excellent overload handling capability, but are poor candidates for high speed work due to inductive effects. Special winding schemes can greatly reduce this parasitic inductance, but never entirely eliminate it.

Table A1. Typical Resistor Characteristics

CHARACTERISTIC		CARBON COMPOSITION	THIN-FILM CARBON FILM	THICK-FILM CERMET	THIN-FILM NiCr FILM	WIREWOUND	METAL FOIL (MOLDED)	METAL FOIL (HERMETIC)
Ohmic Range		2.7M-100M	1M-4.7M	1M-3M	10M-3M	20k-468k	1k-250k	1k-250k
Absolute Accuracy*	Standard	5%	5.0%	1.0%	0.1%	0.01%	0.01%	0.01%
	Available	20%-5%		5.0%-0.1%	1.0%-0.01%	1.0%-0.005%	1.0%-0.005%	1.0%-0.001%
Temperature Coefficient*	Standard	– 5000ppm/°C	– 200ppm/°C	100ppm/°C	10ppm/°C	5ppm/°C		
	Available		– 100ppm/°C-–1500ppm/°C	25ppm/°C-200ppm/°C	5ppm/°C-25ppm/°C	1.0ppm/°C-20ppm/°C	2.5ppm/°C-8ppm/°C	0.6ppm°C
TCR Tracking*					1: (1-9), 1.0ppm/°C 1: (10-100), 2.0ppm/°C 1: (100-1000), 4.0ppm/°C	1: (1-4), 0.5ppm/°C 1: (5-10), 2.0ppm/°C	1: (1-4), 0.5ppm/°C 1: (5-10), 1.0ppm/°C	1: (1-4), 0.5ppm/°C 1: (5-10), 1.0ppm/°C
Ratio Matching*					1: (1-9), 0.005% 1: (10-100), 0.01% 1: (100-1000), 0.02%	1: (1-4), 0.005% 1: (5-10), 0.1%	1:(1-4), 0.005% 1: (5-10), 0.01%	1: (1-4), 0.005% 1: (5-10), 0.01%
Load-Life Stability*		1kHRS, 6% – 4%	3.0%	1.0%	1kHRS, 0.02%	10kHRS, 0.2%	2kHRS, 0.015% 10kHRS, 0.05%	2kHRS, 0.015%
Shelf-Life*		2.0%	0.1%	30ppm/YR	100ppm/YR	25ppm/YR	5ppm/YR	
Voltage Coefficient Of Resistance		– 0.02%/V		0.05ppm/V	0.1ppm/V	0.1ppm/V	0.1ppm/V	
Resistor Classification		General Purpose	General Purpose	Semi-Precision	Precision	Precision	Ultra-Precision	Ultra-Precision
Manufacturer's Part Number		Allen-Bradley** CB Series	International** Resistive Co.	International** Resistive Co.	International** Resistive Co. MAR5	Vishay/Ultronix** 105A	Vishay** S102 Series	Vishay** VHP1000

* ± Unless otherwise stated

** Parameters may vary between manufacturers

% = ppm × 0.0001
0.0001% = 1ppm
0.001% = 10ppm
0.01% = 100ppm
0.1% = 1000ppm
1% = 10000ppm

Thick-Film

Thick-film resistors are made from a paste mixture of Metal-Oxide (cermet) and binder particles, screen printed onto a ceramic substrate and fired at high temperatures. They are semi-precision components, with standard 1% tolerance and typical TC's of 100ppm/°C to 200ppm/°C.

Carbon Composition/Carbon Film

Carbon composition resistors are made from a large chunk of resistive material. They can handle large overloads for a short period of time. This is their main advantage over the other resistor technologies. They are general purpose components, not precision. Carbon composition resistors do not have constant TC's. TC's can vary anywhere between –2000ppm/°C to –8,000ppm/°C and have shelf-life stabilities of 2% to 5% of resistance value (20,000ppm/Yr to 50,000ppm/Yr).

Carbon film resistors are manufactured using a thin-film process. Initial tolerance and TC are similar to carbon composition. However, they do not have the high overload capability. The sole advantage is their low cost.

Resistor Manufacturers

1. Vishay/Ultronix
   461 North 22nd Street
   P.O. Box 1090
   Grand Junction, CO 81502
   (303) 242-0810

2. Vishay Resistive Systems Group
   63 Lincoln Highway
   Malvern, PA 19355
   (215) 644-1300

3. International Resistive Company
   P.O. Box 1860
   Boone, NC 28607
   (704) 264-8861

4. Julie Research Laboratories
   508 West 26th Street
   New York, NY 10001
   (212) 633-6625

5. Allen-Bradley Company, Inc.
   Electronic Components Division
   1414 Allen-Bradley Drive
   El Paso, TX 79936-4888
   (800) 592-4888

APPENDIX B

Capacitor Selection

Capacitor selection for voltage reference circuitry requires care. Capacitor parasitics can introduce errors. Typical capacitors found in reference circuitry include aluminum and tantalum electrolytics, ceramic, and polyester. Table B1 summarizes characteristics pertinent to reference applications. It reveals that equivalent value capacitors have electical characteristics that vary widely between different capacitor technologies.

Leakage current becomes an issue when an RC network filters a reference voltage. The leakage combines with the resistor to shift the output voltage. Leakage varies with time and temperature and varies from device to device. A low leakage capacitor must be used in these applications. The problem is illustrated by considering Figure B1. With R = 1M, a 1×10^{-12} leakage path in a capacitor creates a 1ppm error. Figure B2 is another approach to minimizing leakage induced errors. Here, the voltage across C1 is reduced to zero by bootstrapping via R1. Under these conditions C1's leakage current is effectively zero since there is 0V across it. C2's leakage appears in series with R1, rendering it harmless.

Output capacitors provide low output impedance at high frequencies. Large capacitors at the output of some references may cause oscillations. The capacitor introduces a feedback pole which reduces phase margin of the reference. Phase shift can be excessive with low effective series resistance (ESR) capacitors. The phase shift can be reduced by placing a small value resistor in series with the capacitor. If the phase shift is significant the reference will ring during transient conditions or simply oscillate. This condition is particularly significant for SAR type A/D converter applications. Here, the reference output must settle quickly or conversion errors will result. Consult manufacturers data sheet for recommended output bypassing techniques. Also, all references are not stable with all capacitive loads.

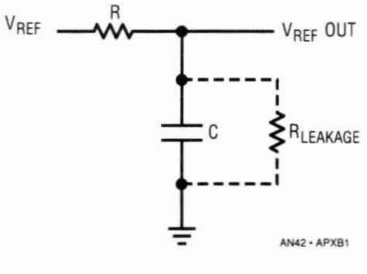


Figure B1. Leakage in the Capacitor Divides $V_{REF'S}$ Output, Introducing Error

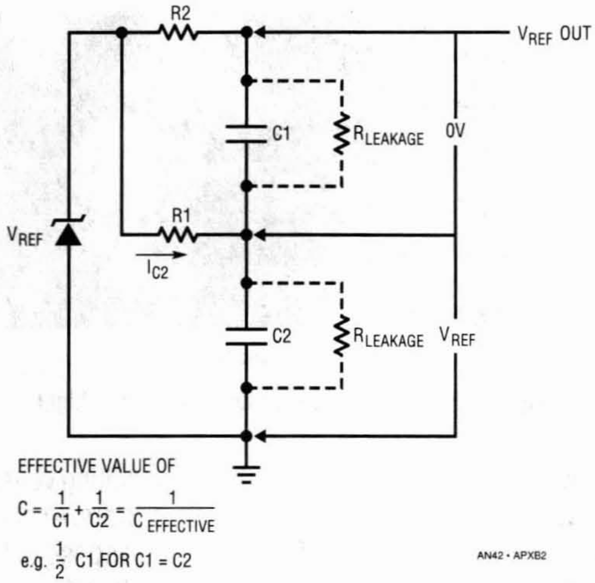


Figure B2. Bootstrapping Technique Minimizes Leakage Effects

Leakage and AC effects are not the only sources of problems. Some ceramic capacitors have a piezoelectric response. A piezoelectric device generates a voltage across it's terminals due to mechanical stress, similar to the way a piezoelectric accelerometer or microphone works. For a ceramic capacitor the stress can be induced by vibrations

Table B1. Typical Capacitor Characteristics

CHARACTERISTIC	ALUMINUM SOLID ELECTROLYTIC	POLYESTER FILM	SOLID TANTALUM ELECTROLYTIC	MULTILAYER CERAMIC	ALUMINUM ELECTROLYTIC	UNIT
Capacitance	0.47	0.47	0.47	0.47	0.47	µF
ESR* 100kHz	0.198	0.456	4.5	0.062	5.4	Ω
Leakage Current* @ 5V	20	0.03	30	0.16	175	nA
Manufacturer's	SANYO	SANYO	KEMET	KEMET	SANYO	

*Typical

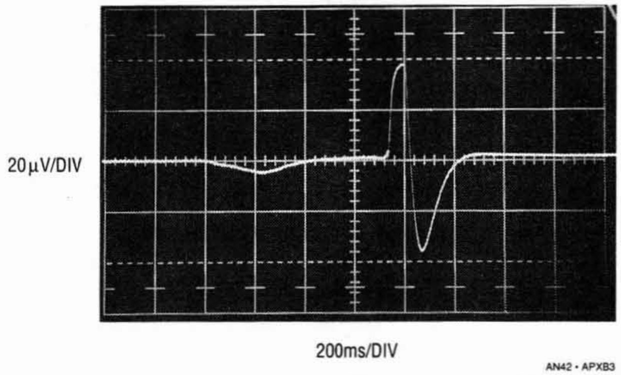


Figure B3. A Ceramic Capacitor Responds to Light Pencil Tapping

in the system or thermal transients. The resulting voltages produced can cause appreciable reference errors. A ceramic capacitor produced Figure B3's trace in response to light tapping from a pencil. Similar vibration induced behavior can masquerade as reference instabilities.

Capacitor Manufacturers

1. Nichicon (America) Corporation
   927 East State Parkway
   Schaumburg, IL 60195
   (708) 843-7500
2. Sanyo Video Components (USA) Corporation
   1201 Sanyo Avenue
   San Diego, CA 92073
   (619) 661-6322
3. United Chemi-Con, Inc.
   9801 West Higgins Road
   Rosemount, IL 60018
   (312) 696-2000
4. Illinois Capacitor, Inc.
   3757 West Touhy Avenue
   Lincolnwood, IL 60645
   (312) 675-1760
5. Kemet Electronics
   P. O. Box 5928
   Greenville, SC 29606
   (803) 963-6300

APPENDIX C

Trimming Techniques

It is often necessary to adjust a resistor's value in precision circuits. The desired value may not be available or readily predictable. Either case necessitates a trim.

For optimum stability and adjustability, always use the smallest value of trim resistance that gives the required range of adjustment. This reduces the stability and drift due to the poor matching characteristics between the fixed resistor and trim resistor. There seems to be a tendency for designers to use a 0.01% resistor with a 1% trim adjustment. Don't pay for accuracy that isn't needed.

Avoid the extremes of resistance range when using a trimmer. Although the entire range will meet the stated specifications, mid-range values tend to perform (TC, tracking, etc.) better than low and high values.

Typical resistor trimming techniques are shown in Figure C1. Selecting the appropriate method depends on various factors including trim range, temperature stability, long term stability, manufacturing processes, and calibration procedures. Figure C1(A) is a general purpose trim. This technique has an extremely wide range. Equation 1 represents the percentage change in the desired resistor value, R_{EQ}, for a change in trim resistance. This equation is useful when determining the optimum trimmer resistance and is provided for the various trimming schemes. If increased stability is required, the circuit in Figure C1(B) can be used. In this case, increased stability is achieved at the expense of a narrower trim range. R1 must have a tighter absolute tolerance than in the previous circuit for this technique to be useful. For improved resolution, a resistor can be placed in series with this network, see Figure C1(C). This approach is best suited for ultra-precision applications, since it has the highest resolution.

In some applications potentiometers may be unreliable. In these cases, resistor value can be trimmed by selecting the appropriate series resistor value, see Figure C1(D). However, this requires numerous resistors that must be hand picked in production. An alternative approach is to use a binary weighted trim as in Figure C1(E). The resistance is trimmed by opening various links. With just four resistors there are 16 different resistor values possible. With this method, the need for a bin of resistors on the production floor is eliminated.

Often, the best solution is to have coarse and fine adjustments. This can provide a more stable resistor value. Figure C1(F) illustrates various ways to implement this approach.

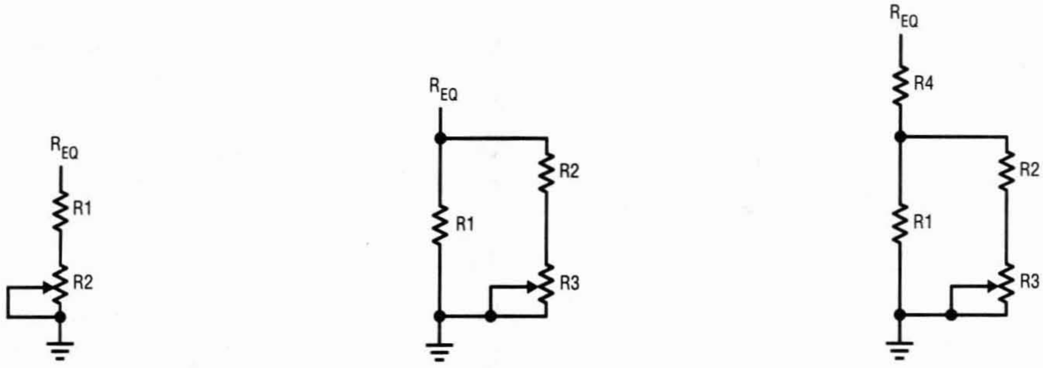
In many voltage reference circuits it is necessary to scale and buffer the output of a reference to some calibrated voltage. The trim sets the output voltage to the desired degree of accuracy. Figure C2 shows various techniques for trimming the buffered output. These examples utilize various resistor trimming techniques to set output voltage.

Figure C2 (B) shows a simple voltage reference circuit. The reference is connected to the non-inverting input of an op amp. The feedback resistors around the op amp scale the output voltage to the approximate output voltage. The potentiometer fine tunes the output to the desired value.

The temperature coefficient (TC) of the op amps gain setting resistors can add significant error to the reference output due to ambient temperature changes. The circuits temperature coefficient is primarily set by the ratio matching characteristics of the resistors, as opposed to their absolute tolerance. Matched resistor sets provide a decade or greater improvement in tempco performance than individually specified resistors. Therefore, resistors that have relatively high TC's can be used if they track.

Another interesting characteristic of this circuit is the magnitude of output voltage drift with temperature caused by the gain setting resistors. The drift error contributed by the resistors is determined by multiplying their ratio (R1/R2) by their TCR tracking tolerance. For example, to obtain a 10V output from a 6.9V reference the gain setting resistors ratio needs to be about 0.45. This means that 10ppm/°C resistor TCR tracking effects output voltage by only 4.5ppm/°C. Therefore, for minimum effect of the resistor's TCR tracking, it is desirable to have the reference voltage be a large percentage of the output voltage.

The remaining circuits in Figure C2 show some alternatives for trimming a reference voltage. The particular circuit selected depends upon the required performance specifications and manufacturing processes.


R_{EQ}
R1
R2
R_{EQ}
R1
R2
R3
R_{EQ}
R4
R1
R2
R3

1) $\%\Delta R_{EQ} = \frac{\Delta R2}{R1+R2} \bullet 100$

2) $\%\Delta R_{EQ} \approx \frac{\Delta R3\ R1}{(R2+R3)^2} \bullet 100$

$R1 << R2 + R3$

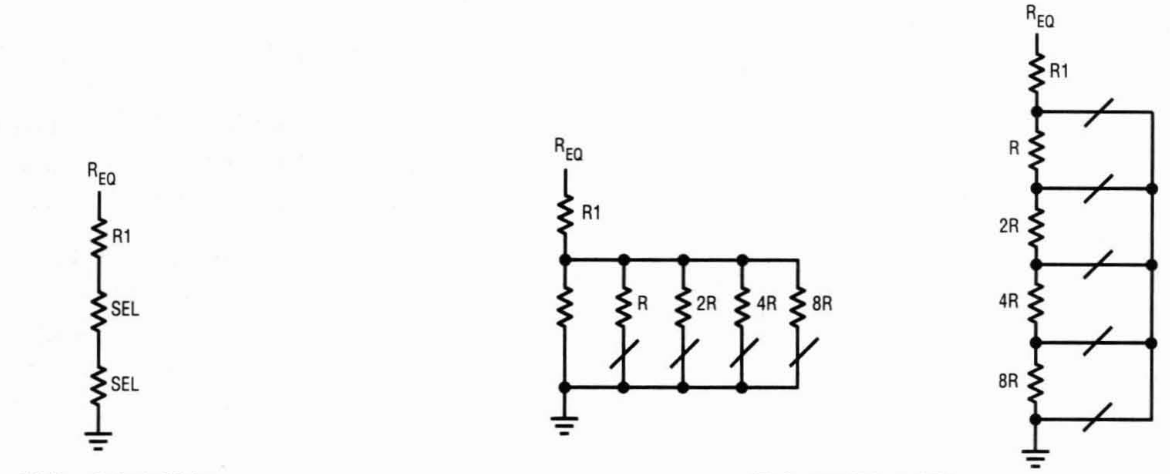
3) $\%\Delta R_{EQ} \approx \frac{R1}{(R1+R4)} \frac{\Delta R3\ R1}{(R2+R3)^2} \bullet 100$

$R1 << R2 + R3$

(A) General Purpose Trim

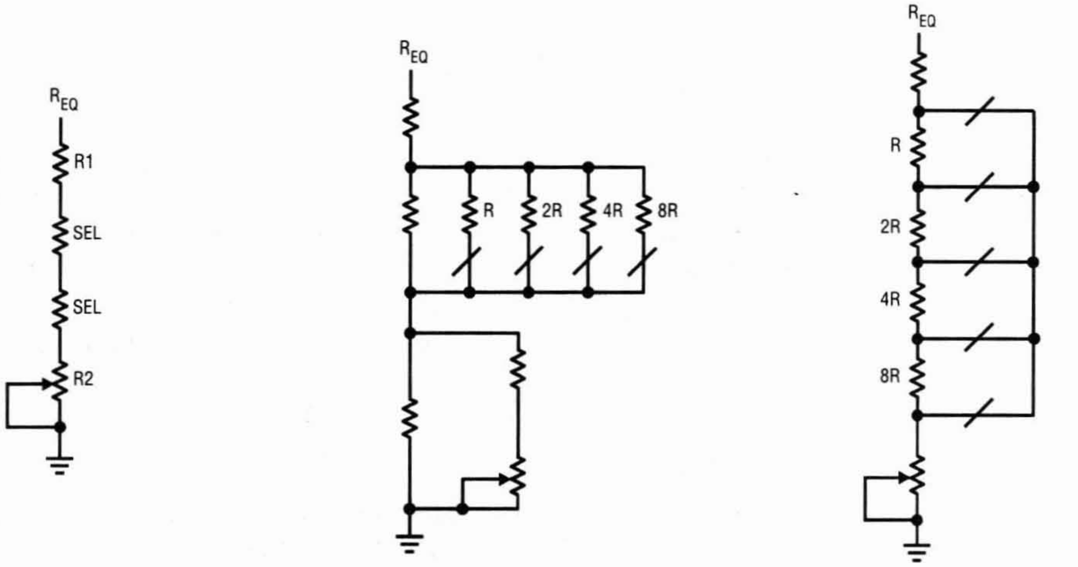
(B) Semi-Precision Trim

(C) Precision Trim


R_{EQ}
R1
SEL
SEL
R_{EQ}
R1
R
2R
4R
8R
R_{EQ}
R1
R
2R
4R
8R

(D) User Selected Trim

(E) Jumper Selected Trim


R_{EQ}
R1
SEL
SEL
R2
R_{EQ}
R
2R
4R
8R
R_{EQ}
R
2R
4R
8R
AN42 • APXC1

(F) Coarse and Fine Adjustments

Figure C1. Resistor Trimming Techniques

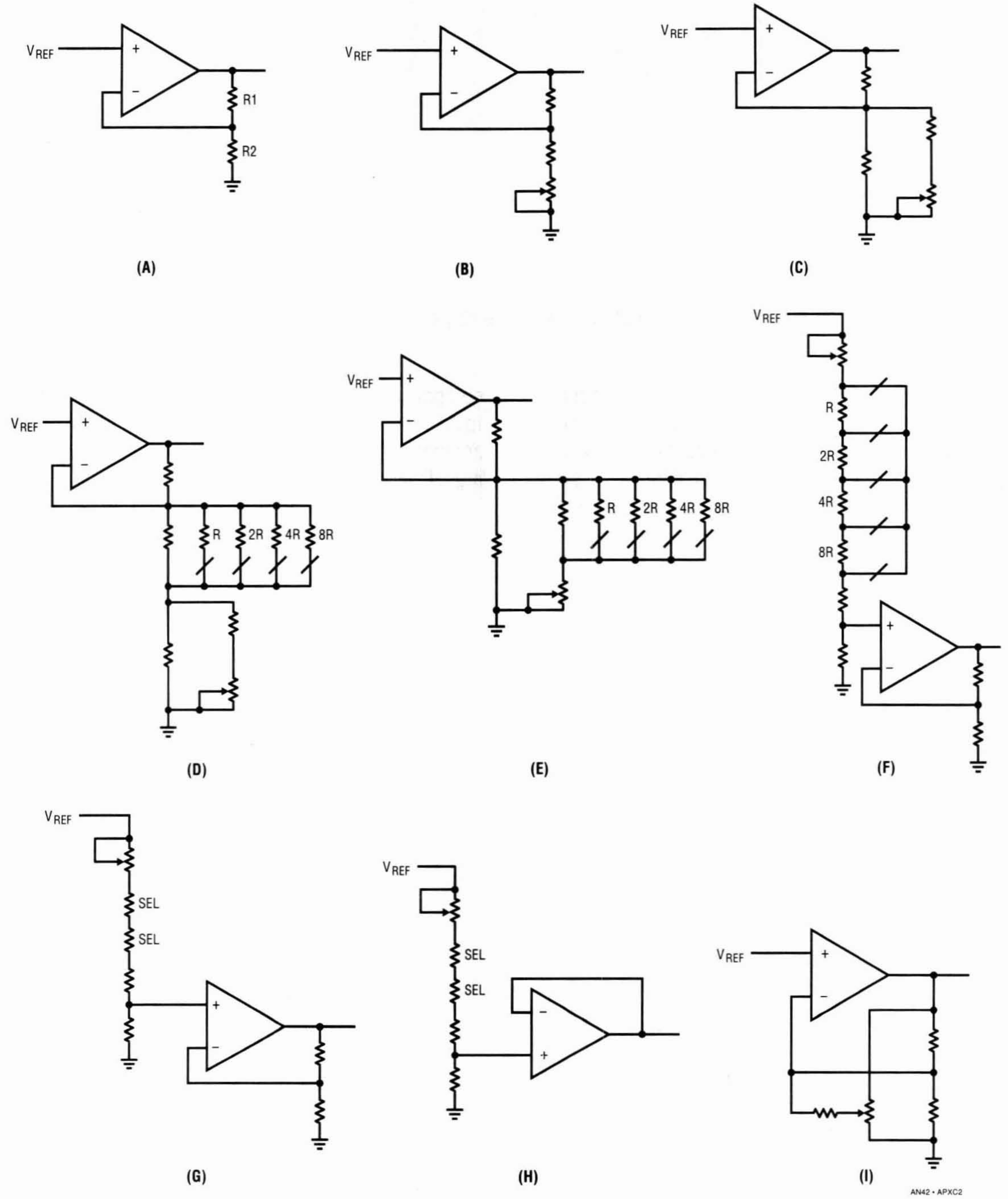

V_REF
+
−
R1
R2
(A)
(B)
(C)
R
2R
4R
8R
(D)
(E)
(F)
SEL
SEL
(G)
(H)
(I)
AN42 • APXC2

Figure C2. Output Voltage Trimming Techniques

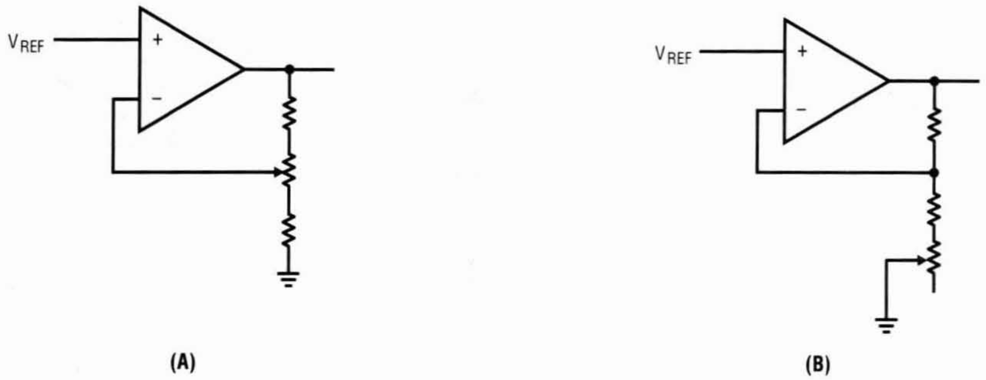


Figure C3. Unreliable Trimming Techniques

If reliability is an issue, do not rely on the potentiometer wiper contact. The open wiper condition is a common trimmer failure. If this occurs the outputs in Figure C3 will go to the supply rails, possibly damaging other system components. With the unused portion of the trimmer tied to the wiper (Figure C2 (B)) the output can only shift by the amount permitted by the total trimmer resistance, improving reliability.

June 1990

Bridge Circuits

Marrying Gain and Balance

Jim Williams

Bridge circuits are among the most elemental and powerful electrical tools. They are found in measurement, switching, oscillator and transducer circuits. Additionally, bridge techniques are broadband, serving from DC to bandwidths well into the GHz range. The electrical analog of the mechanical beam balance, they are also the progenitor of all electrical differential techniques.

Resistance Bridges

Figure 1 shows a basic resistor bridge. The circuit is usually credited to Charles Wheatstone, although S.H. Christie, who demonstrated it in 1833, almost certainly preceded him.[1] If all resistor values are equal (or the two sides *ratios* are equal) the differential voltage is zero. The excitation voltage does not alter this, as it effects both sides equally. When the bridge is operating off null, the excitation's magnitude sets output sensitivity. The bridge output is non-linear for a single variable resistor. Similarly, two variable arms (e.g., R_C and R_B both variable) produce non-linear output, although sensitivity doubles. Linear outputs are possible by complementary resistance swings in one or both sides of the bridge.

A great deal of attention has been directed towards this circuit. An almost uncountable number of tricks and techniques have been applied to enhance linearity, sensitivity and stability of the basic configuration. In particular, transducer manufacturers are quite adept at adapting the bridge to their needs (see Appendix A, "Strain Gauge Bridges"). Careful matching of the transducer's mechanical characteristics to the bridges electrical response can provide a trimmed, calibrated output. Similarly, circuit designers have altered performance by adding active elements (e.g., amplifiers) to the bridge, excitation source, or both.

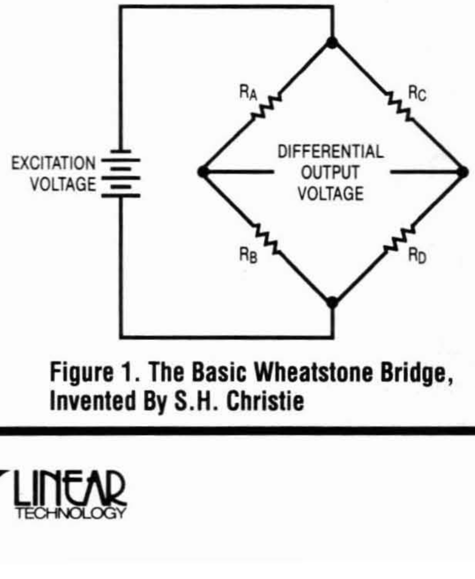


Figure 1. The Basic Wheatstone Bridge, Invented By S.H. Christie

Bridge Output Amplifiers

A primary concern is the accurate determination of the differential output voltage. In bridges operating at null the absolute scale factor of the readout device is normally less important than its sensitivity and zero point stability. An off-null bridge measurement usually requires a well calibrated scale factor readout in addition to zero point stability. Because of their importance, bridge readout mechanisms have a long and glorious history (see Appendix B, "Bridge Readout — Then and Now"). Todays investigator has a variety of powerful electronic techniques available to obtain highly accurate bridge readouts. Bridge amplifiers are designed to accurately extract the bridges differential output from its common mode level. The ability to reject common mode signal is quite critical. A typical 10V powered strain gauge transducer produces only 30mV of signal "riding" on 5V of common mode level. 12-bit readout resolution calls for an LSB of only 7.3μV.....almost 120dB below the common mode signal! Other significant error terms include offset voltage, and its shift with temperature and time, bias current and gain stability. Figure 2 shows an "Instrumentation Amplifier," which makes a very good bridge amplifier. These devices are usually the first choice for bridge measurement, and bring adequate performance to most applications. In general, instrumentation amps feature fully differential inputs and internally determined stable gain. The absence of a feedback network means the inputs are

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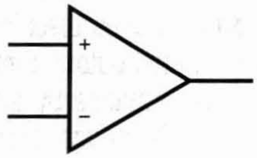
Note 1: Wheatstone had a better public relations agency, namely himself. For fascinating details, see reference 19.

essentially passive, and no significant bridge loading occurs. Instrumentation amplifiers meet most bridge requirements. Figure 3 lists performance data for some specific instrumentation amplifiers. Figure 4's table summarizes some options for DC bridge signal conditioning. Various approaches are presented, with pertinent characteristics noted. The constraints, freedoms and performance requirements of any particular application define the best approach.



→ NO FEEDBACK RESISTORS USED
→ GAIN FIXED INTERNALLY (TYP 10 OR 100) OR SOMETIMES RESISTOR PROGRAMMABLE
→ BALANCED, PASSIVE INPUTS

Figure 2. Conceptual Instrumentation Amplifier

DC Bridge Circuit Applications

Figure 5, a typical bridge application, details signal conditioning for a 350Ω transducer bridge. The specified strain gauge pressure transducer produces 3mV output per volt of bridge excitation (various types of strain based transducers are reviewed in Appendix A, "Strain Gauge Bridges"). The LT1021 reference, buffered by A1A and A2, drives the bridge. This potential also supplies the circuits ratio output, permitting ratiometric operation of a monitoring A-D converter. Instrumentation amplifier A3 extracts the bridges differential output at a gain of 100, with additional trimmed gain supplied by A1B. The configuration shown may be adjusted for a precise 10V output at full scale pressure. The trim at the bridge sets the zero pressure scale point. The RC combination at A1B's input filters noise. The time constant should be selected for the system's desired low pass cut off. "Noise" may originate as residual RF/line pick-up or true transducer responses to pressure variations. In cases where noise is relatively high it may be desirable to filter ahead of A3. This prevents any possible signal infidelity due to non-linear A3 operation. Such undesirable outputs can be produced by saturation, slew rate components, or rectification effects. When filtering ahead of the circuits gain blocks remember to allow for the effects of bias current induced errors caused by the filter's series resistance. This can be a significant consideration because large value capacitors, particularly electrolytics, are not practical. If bias current induced errors rise to appreciable levels FET or MOS input amplifiers may be required (see Figure 3).

To trim this circuit apply zero pressure to the transducer and adjust the 10k potentiometer until the output *just* comes off 0V. Next, apply full scale pressure and trim the 1k adjustment. Repeat this procedure until both points are fixed.

Common Mode Suppression Techniques

Figure 6 shows a way to reduce errors due to the bridges common mode output voltage. A1 biases Q1 to servo the bridges left mid-point to zero under all operating conditions. The 350Ω resistor ensures that A1 will find a stable operating point with 10V of drive delivered to the bridge. This allows A2 to take a single ended measurement, eliminating all common mode voltage errors. This approach works well, and is often a good choice in high precision

PARAMETER	LTC1100	LT1101	LT1102	LTC1043 (USING LTC1050 AMPLIFIER)
Offset	10μV	160μV	500μV	0.5μV
Offset Drift	100nV/°C	2μV/°C	2.5μV/°C	50nV/°C
Bias Current	50pA	8nA	50pA	10pA
Noise (0.1Hz–10Hz)	2μVp-p	0.9μV	2.8μV	1.6μV
Gain	100	10,100	10,100	Resistor Programmable
Gain Error	0.03%	0.03%	0.05%	Resistor Limited 0.001% Possible
Gain Drift	4ppm/°C	4ppm/°C	5ppm/°C	Resistor Limited <1ppm/°C Possible
Gain Non-Linearity	8ppm	8ppm	10ppm	Resistor Limited 1ppm Possible
CMRR	104dB	100dB	100dB	160dB
Power Supply	Single or Dual, 16V Max	Single or Dual, 44V Max	Dual, 44V Max	Single, Dual 18V Max
Supply Current	2.2mA	105μA	5mA	2mA
Slew Rate	1.5V/μs	0.07V/μs	25V/μs	1mV/ms
Bandwidth	8kHz	33kHz	220kHz	10Hz

Figure 3. Comparison of Some IC Instrumentation Amplifiers

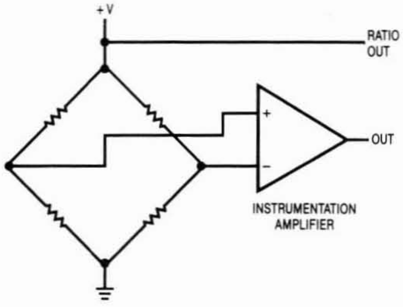
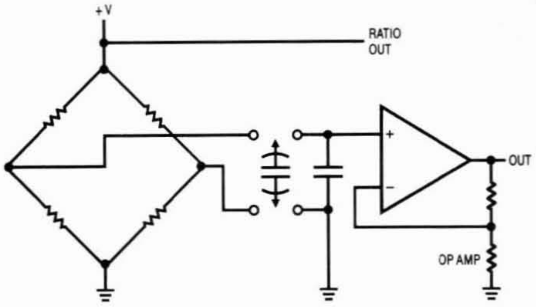
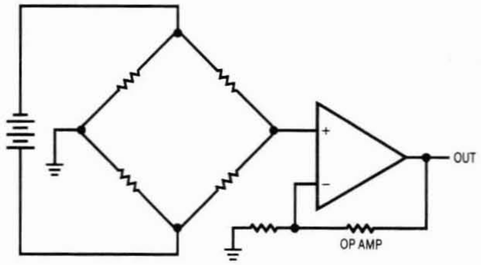
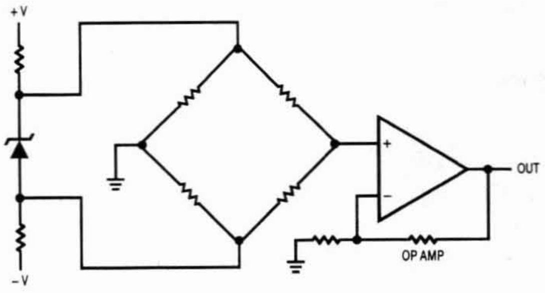
CONFIGURATION	ADVANTAGES	DISADVANTAGES
 +V RATIO OUT + – OUT INSTRUMENTATION AMPLIFIER	Best General Choice. Simple, Straightforward. CMRR Typically >110dB, Drift 0.05μV/°C-2μV/°C, Gain Accuracy 0.03%, Gain Drift 4ppm/°C, Noise 10nV√Hz — 1.5μV for Chopper Stabilized Types. Direct Ratiometric Output.	CMRR, Drift, and Gain Stability May Not Be Adequate in Highest Precision Applications. May Require Second Stage to Trim Gain.
	CMRR>120dB, Drift 0.05μV/°C. Gain Accuracy 0.001% Possible. Gain Drift 1ppm with Appropriate Resistors. Noise 10nV√Hz — 1.5μV for Chopper Stabilized Types. Direct Ratiometric Output. Simple Gain Trim. Flying Capacitor Commutation Provides Lowpass Filtering. Good Choice for Very High Performance — Monolithic Versions (LTC1043) Available.	Multi-Package — Moderately Complex. Limited Bandwidth. Requires Feedback Resistors to Set Gain.
	CMRR>160dB, Drift 0.05μV/°C-0.25μV/°C, Gain Accuracy 0.001% Possible, Gain Drift 1ppm/°C with Appropriate Resistors Plus Floating Supply Error, Simple Gain Trim, Noise 1nV√Hz Possible.	Requires Floating Supply. No Direct Ratiometric Output. Floating Supply Drift is a Gain Term. Requires Feedback Resistors to Set Gain.
	CMRR≈140dB, Drift 0.05μV/°C-0.25μV/°C, Gain Accuracy 0.001% Possible, Gain Drift 1ppm/°C With Appropriate Resistors Plus Floating Supply Error, Simple Gain Trim, Noise 1nV√Hz Possible.	No Direct Ratiometric Output. Zener Supply is a Gain and Offset Term Error Generator. Requires Feedback Resistors to Set Gain. Low Impedance Bridges Require Substantial Current from Shunt Regulator or Circuitry Which Simulates it. Usually Poor Choice if Precision is Required.

Figure 4. Some Signal Conditioning Methods for Bridges

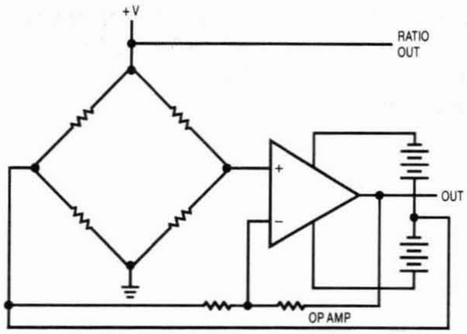
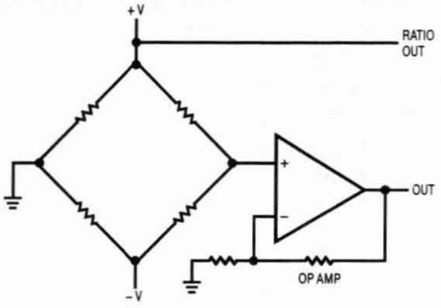
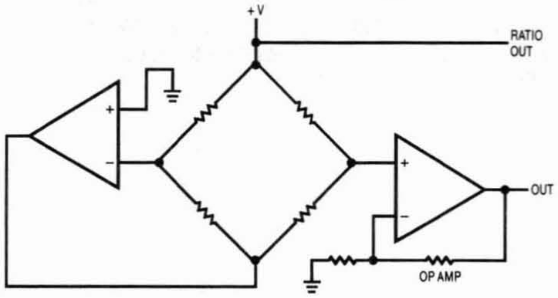
CONFIGURATION	ADVANTAGES	DISADVANTAGES
	CMRR > 160dB, Drift 0.05μV/°C–0.25μV/°C, Gain Accuracy 0.001% Possible, Gain Drift 1ppm/°C with Appropriate Resistors, Simple Gain Trim, Ratiometric Output, Noise $1\text{nV}\sqrt{\text{Hz}}$ Possible.	Requires Precision Analog Level Shift, Usually with Isolation Amplifier. Requires Feedback Resistors to Set Gain.
	CMRR ≈ 120dB–140dB, Drift 0.05μV/°C–0.25μV/°C, Gain Accuracy 0.001% Possible, Gain Drift 1ppm/°C with Appropriate Resistors, Simple Gain Trim, Direct Ratiometric Output, Noise $1\text{nV}\sqrt{\text{Hz}}$ Possible.	Requires Tracking Supplies. Assumes High Degree of Bridge Symmetry to Achieve Best CMRR. Requires Feedback Resistors to Set Gain.
	CMRR 160dB, Drift 0.05μV/°C–0.25μV/°C, Gain Accuracy 0.001% Possible, Gain Drift 1ppm/°C, Simple Gain Trim, Direct Ratiometric Output, Noise $1\text{nV}\sqrt{\text{Hz}}$ Possible.	Practical Realization Requires Two Amplifiers Plus Various Discrete Components. Negative Supply Necessary.

Figure 4. Some Signal Conditioning Methods for Bridges (Continued)

work. The amplifiers in this example, CMOS chopper stabilized units, essentially eliminate offset drift with time and temperature. Trade offs compared to an instrumentation amplifier approach include complexity and the requirement for a negative supply. Figure 7 is similar, except that low noise bipolar amplifiers are used. This circuit trades slightly higher DC offset drift for lower noise and is a good candidate for stable resolution of small, slowly varying measurands. Figure 8 employs chopper stabilized A1 to reduce Figure 7's already small offset error. A1 measures the DC error at A2's inputs and biases A1's offset pins to force offset to a few microvolts. The offset pin biasing at A2 is arranged so A1 will always be able to find the servo point. The 0.01μF capacitor rolls off A1 at low frequency, with A2 handling high frequency signals. Returning A2's feedback string to the bridges midpoint eliminates A4's offset contribution. If this was not done A4 would require a similar offset correction loop. Although complex, this approach achieves less than 0.05μV/°C drift, $1\text{nV}\sqrt{\text{Hz}}$ noise and CMRR exceeding 160dB.

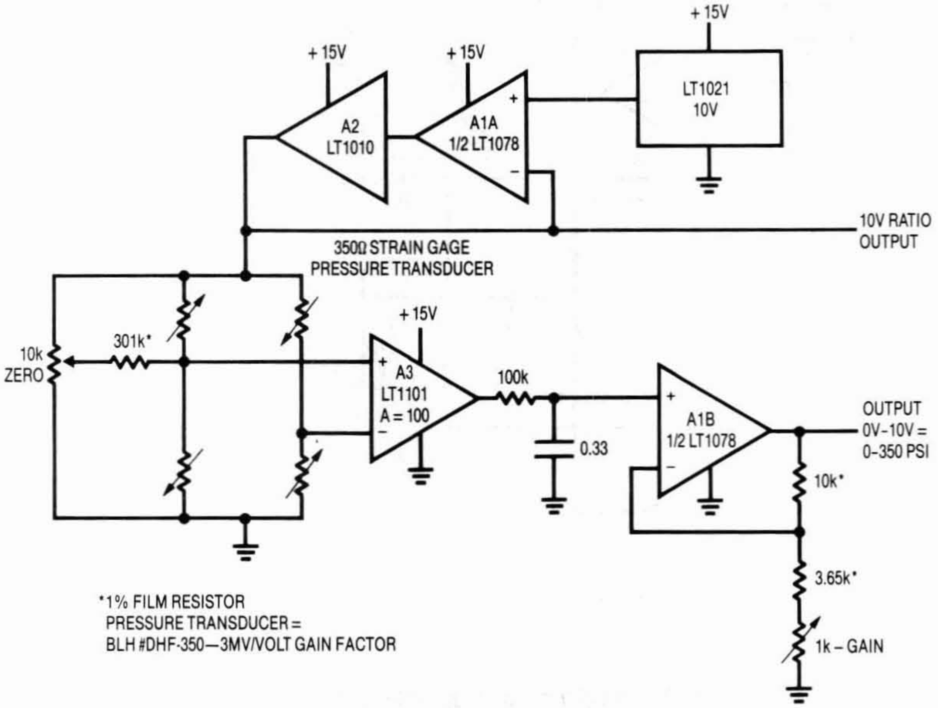

+15V
+15V
+15V
A2
LT1010
A1A
1/2 LT1078
LT1021
10V
10V RATIO
OUTPUT
350Ω STRAIN GAGE
PRESSURE TRANSDUCER
+15V
10k
ZERO
301k*
A3
LT1101
A = 100
100k
0.33
A1B
1/2 LT1078
OUTPUT
0V-10V =
0-350 PSI
10k*
3.65k*
1k – GAIN
*1% FILM RESISTOR
PRESSURE TRANSDUCER =
BLH #DHF-350—3MV/VOLT GAIN FACTOR

Figure 5. A Practical Instrumentation Amplifier Based Bridge Circuit

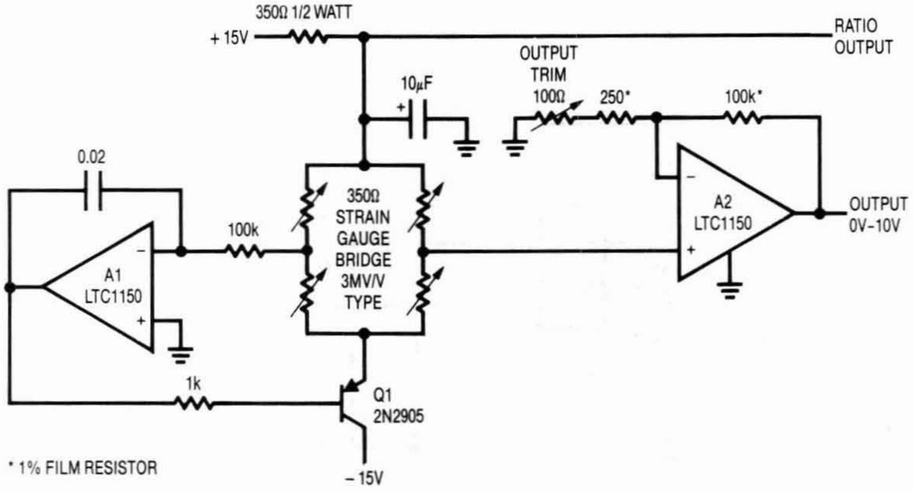

350Ω 1/2 WATT
+15V
RATIO
OUTPUT
OUTPUT
TRIM
100Ω
250*
100k*
10µF
0.02
100k
350Ω
STRAIN
GAUGE
BRIDGE
3MV/V
TYPE
A1
LTC1150
A2
LTC1150
OUTPUT
0V-10V
1k
Q1
2N2905
–15V
* 1% FILM RESISTOR

Figure 6. Servo Controlling Bridge Drive Eliminates Common Mode Voltage

Single Supply Common Mode Suppression Circuits

The common mode suppression circuits shown require a negative power supply. Often, such circuits must function in systems where only a positive rail is available. Figure 9 shows a way to do this. A2 biases the LTC1044 positive-to-negative converter. The LTC1044's output pulls the bridge's output negative, causing A1's input to balance at 0V. This local loop permits a single-ended amplifier (A2) to extract the bridge's output signal. The 100k-0.33μF RC filters noise and A2's gain is set to provide the desired output scale factor. Because bridge drive is derived from the LT1034 reference, A2's output is not affected by supply shifts. The LT1034's output is available for ratio operation. Although this circuit works nicely from a single 5V rail the transducer sees only 2.4V of drive. This reduced

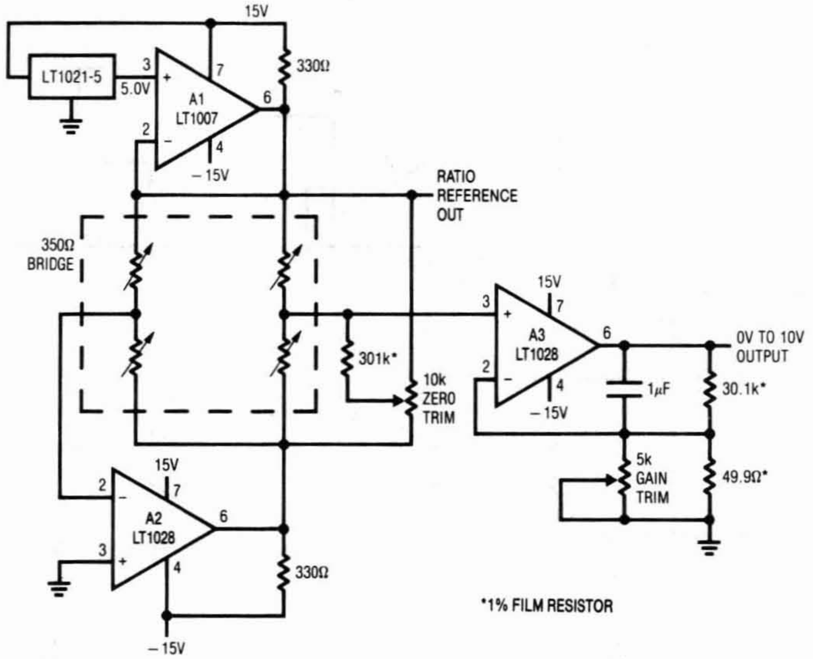

15V
LT1021-5
5.0V
A1
LT1007
330Ω
−15V
RATIO
REFERENCE
OUT
350Ω
BRIDGE
301k*
10k
ZERO
TRIM
A3
LT1028
15V
−15V
0V TO 10V
OUTPUT
1μF
30.1k*
5k
GAIN
TRIM
49.9Ω*
A2
LT1028
15V
330Ω
−15V
*1% FILM RESISTOR

Figure 7. Low Noise Bridge Amplifier with Common Mode Suppression

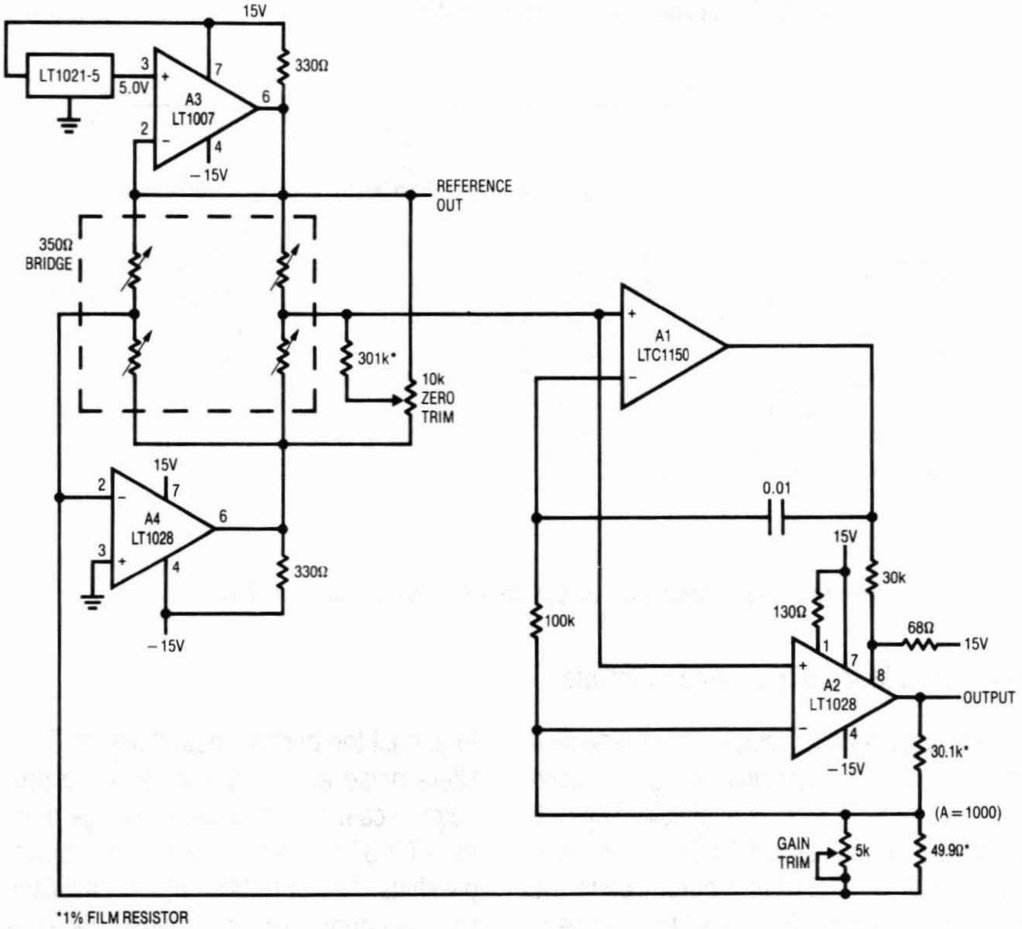

15V
LT1021-5
5.0V
A3
LT1007
330Ω
−15V
REFERENCE
OUT
350Ω
BRIDGE
301k*
10k
ZERO
TRIM
A1
LTC1150
A4
LT1028
15V
330Ω
−15V
0.01
15V
30k
130Ω
100k
68Ω
15V
A2
LT1028
OUTPUT
−15V
30.1k*
(A = 1000)
GAIN
TRIM
5k
49.9Ω*
*1% FILM RESISTOR

Figure 8. Low Noise, Chopper Stabilized Bridge Amplifier with Common Mode Suppression

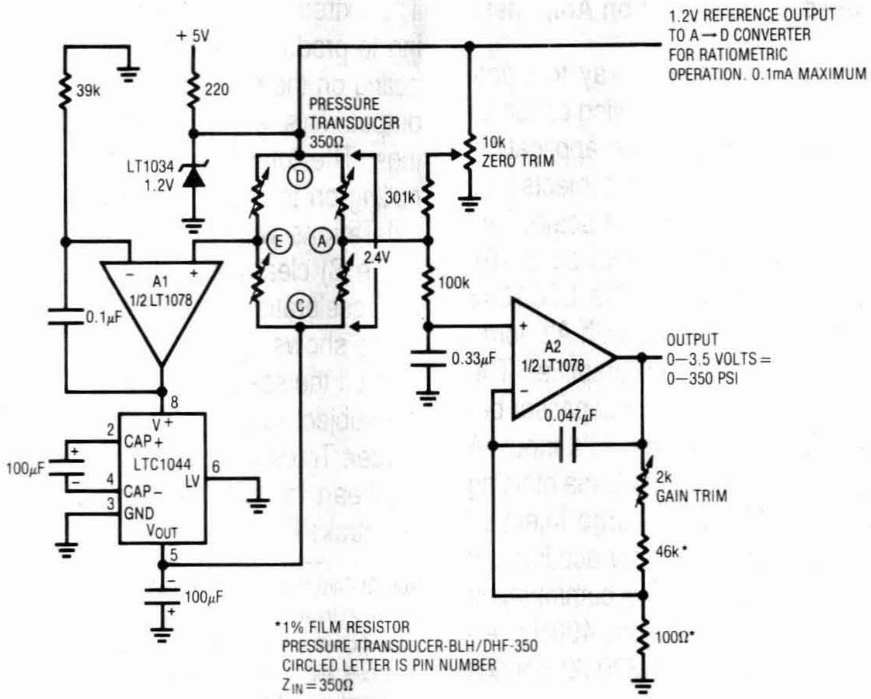

+5V
39k
220
LT1034
1.2V
PRESSURE
TRANSDUCER
350Ω
D
E
A
C
A1
1/2 LT1078
0.1μF
301k
10k
ZERO TRIM
2.4V
100k
1.2V REFERENCE OUTPUT
TO A → D CONVERTER
FOR RATIOMETRIC
OPERATION. 0.1mA MAXIMUM
0.33μF
A2
1/2 LT1078
OUTPUT
0—3.5 VOLTS =
0—350 PSI
0.047μF
2k
GAIN TRIM
46k*
100Ω*
8
2
V+
CAP+
100μF
4
LTC1044
6
LV
CAP−
3
GND
VOUT
5
100μF
*1% FILM RESISTOR
PRESSURE TRANSDUCER-BLH/DHF-350
CIRCLED LETTER IS PIN NUMBER
$Z_{IN} = 350\Omega$

Figure 9. Single Supply Bridge Amplifier with Common Mode Suppression

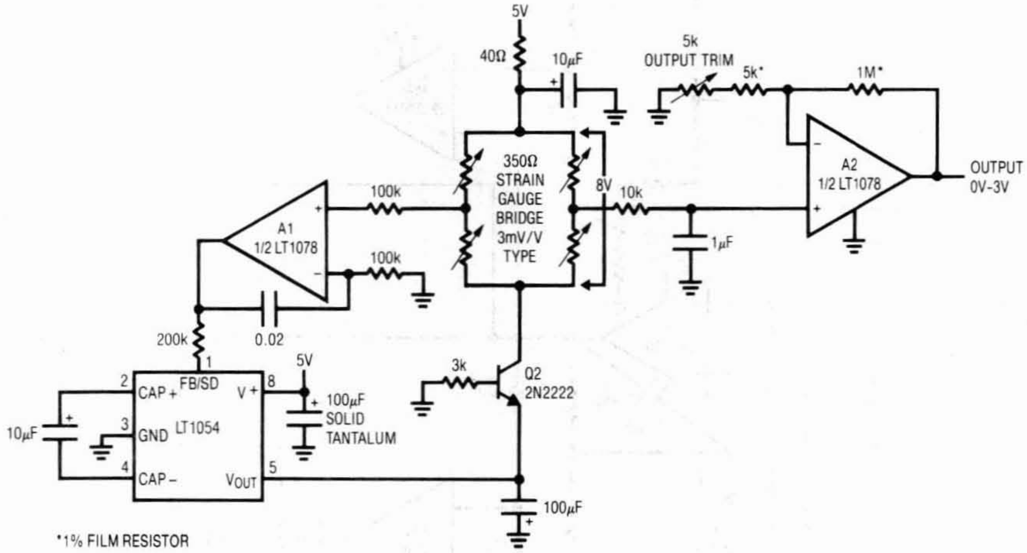

5V
40Ω
10μF
5k
OUTPUT TRIM
5k*
1M*
350Ω
STRAIN
GAUGE
BRIDGE
3mV/V
TYPE
8V
10k
1μF
A2
1/2 LT1078
OUTPUT
0V-3V
100k
100k
A1
1/2 LT1078
0.02
200k
1
FB/SD
2
CAP+
V+
8
5V
100μF
SOLID
TANTALUM
10μF
3
GND
LT1054
4
CAP−
VOUT
5
3k
Q2
2N2222
100μF
*1% FILM RESISTOR

Figure 10. High Resolution Version of Figure 9. Bipolar Voltage Converter Gives Greater Bridge Drive, Increasing Output Signal.

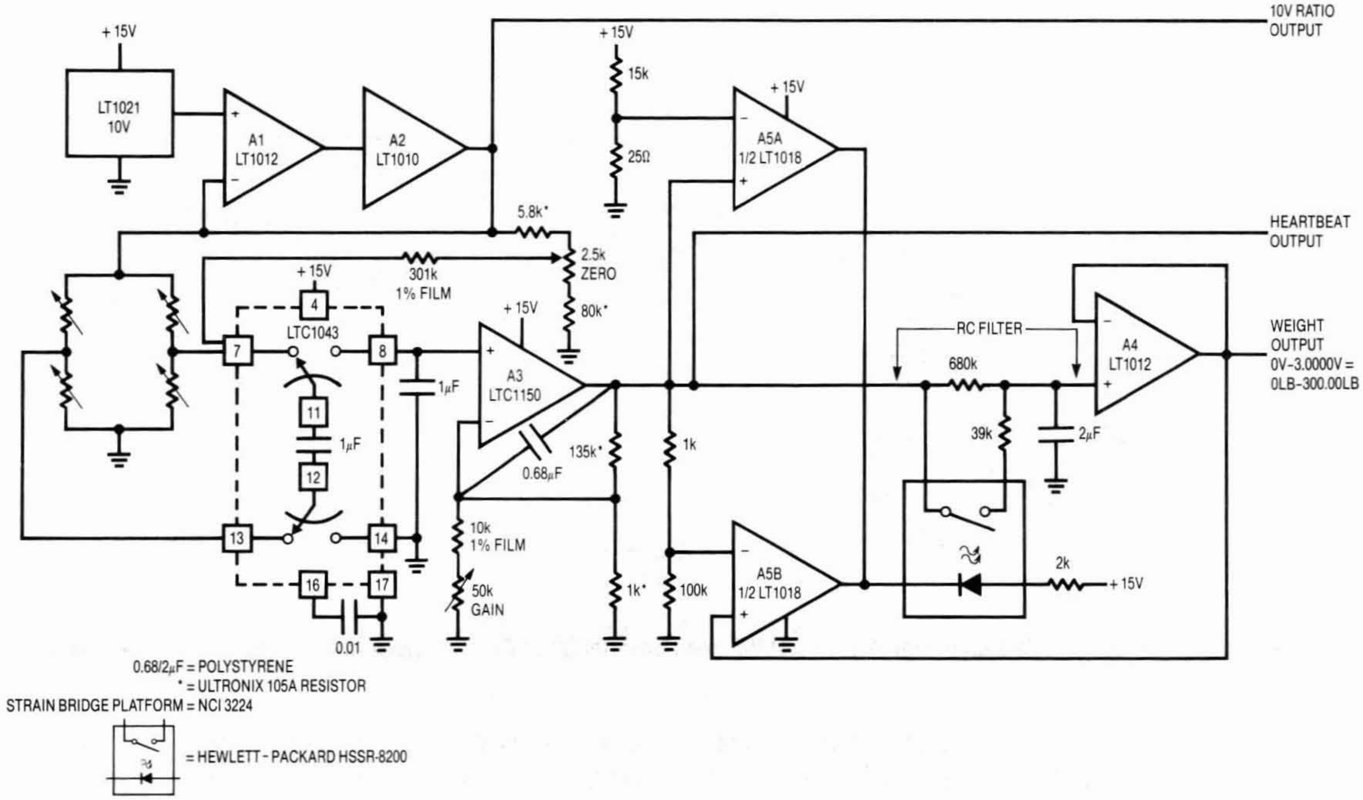
drive results in lower transducer outputs for a given measurand value, effectively magnifying amplifier offset drift terms. The limit on available bridge drive is set by the CMOS LTC1044's output impedance. Figure 10's circuit employs a bipolar positive-to-negative converter which has much lower output impedance. The biasing used permits 8V to appear across the bridge, requiring the 100mA capability LT1054 to sink about 24mA. This increased drive results in a more favorable transducer gain slope, increasing signal-to-noise ratio.

Switched Capacitor Based Instrumentation Amplifiers

Switched capacitor methods are another way to signal condition bridge outputs. Figure 11 uses a flying capacitor configuration in a very high precision scale application. This design, intended for weighing human subjects, will resolve 0 .01 pound at 300.00 pounds full scale. The strain gauge based transducer platform is excited at 10V by the LT1021 reference, A1 and A2. The LTC1043 switched capacitor building block combines with A3, forming a differential input chopper stabilized amplifier. The LTC1043 alternately connects the 1μF flying capacitor between the strain gauge bridge output and A3's input. A second 1μF unit stores the LTC1043 output, maintaining A3's input at DC. The LTC1043's low charge injection maintains differential to single ended transfer accuracy of about 1ppm at DC and low frequency. The commutation rate, set by the 0.01μF capacitor, is about 400Hz. A3 takes scaled gain, providing 3.0000V for 300.00 pounds full scale output.

The extremely high resolution of this scale requires filtering to produce useful results. Very slight body movement acting on the platform can cause significant noise in A3's output. This is dramatically apparent in Figure 12's tracings. The total *force* on the platform is equal to gravity pulling on the body (the "weight") plus any additional accelerations within or acting upon the body. Figure 12 (trace B) clearly shows that each time the heart pumps, the acceleration due to the blood (mass) moving in the arteries shows up as "weight." To prove this, the subject gets off the scale and runs in place for 15 seconds. When the subject returns to the platform the heart should work harder. Trace A confirms this nicely. The exercise causes the heart to work harder, forcing a greater acceleration-per-stroke.[2]

Note 2: Cardiology aficionados will recognize this as a form of *Ballistocardiograph* (from the Greek "ballein" — to throw, hurl or eject and "kardia," heart). A significant amount of effort was expended in attempts to reliably characterize heart conditions via acceleration detection methods. These efforts were largely unsuccessful when compared against the reliability of EKG produced data. See references for further discussion.


+15V
LT1021
10V
A1
LT1012
A2
LT1010
+15V
15k
25Ω
+15V
A5A
1/2 LT1018
10V RATIO
OUTPUT
5.8k*
2.5k
ZERO
80k*
301k
1% FILM
+15V
4
LTC1043
7
8
11
1μF
12
13
14
16
17
0.01
1μF
+15V
A3
LTC1150
0.68μF
135k*
10k
1% FILM
50k
GAIN
1k*
1k
100k
A5B
1/2 LT1018
HEARTBEAT
OUTPUT
RC FILTER
680k
39k
2μF
2k
+15V
A4
LT1012
WEIGHT
OUTPUT
0V-3.0000V =
0LB-300.00LB

0.68/2μF = POLYSTYRENE
* = ULTRONIX 105A RESISTOR
STRAIN BRIDGE PLATFORM = NCI 3224
= HEWLETT - PACKARD HSSR-8200

Figure 11. High Precision Scale for Human Subjects

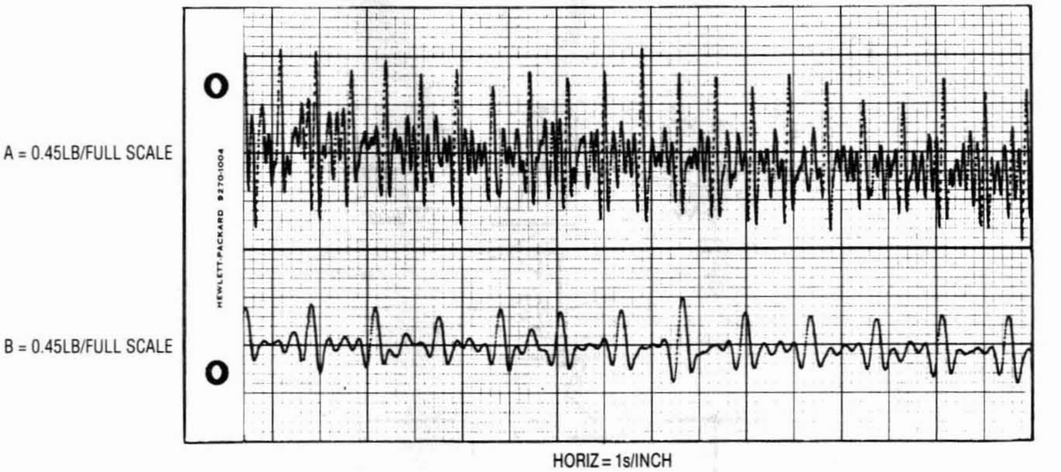


Figure 12. High Precision Scale's Heartbeat Output. Trace B Shows Subject at Rest; Trace A After Exercise. Discontinuous Components in Waveforms Leading Edges Are Due to XY Recorder Slew Limitations.

Another source of noise is due to body motion. As the body moves around, its mass doesn't change but the instantaneous accelerations are picked up by the platform and read as "weight" shifts.

All this seems to make a 0.01 pound measurement meaningless. However, filtering the noise out gives a time averaged value. A simple RC low pass will work, but requires excessively long settling times to filter noise fundamentals in the 1Hz region. Another approach is needed.

A4, A5 and associated components form a filter which switches it's time constant from short to long when the output has nearly arrived at the final value. With no weight on the platform A3's output is zero. A4's output is also zero, A5B's output is indeterminate and A5A's output is low. The MOSFET optocouplers LED comes on, putting the RC filter into short time constant mode. When someone gets on the scale A3's output rises rapidly. A5A goes high, but A5B trips low, maintaining the RC filter in its short time constant mode. The 2μF capacitor charges rapidly, and A4 quickly settles to final value ± body motion and heartbeat noise. A5B's negative input sees 1% attenuation from A3; it's positive input does not. This causes A5B to switch high when A4's output arrives within 1% of final value. The optocoupler goes off and the filter switches into long time constant mode, eliminating noise in A4's output. The 39k resistor prevents overshoot, ensuring monotonic A4 outputs. When the subject steps off the scale A3 quickly returns to zero. A5A goes immediately low, turning on the optocoupler. This quickly discharges the 2μF capacitor, returning A4's output rapidly to zero. The bias string at A5A's input maintains the scale in fast time constant mode for weights below 0.50 pounds. This permits rapid response when small objects (or persons) are placed on the platform. To trim this circuit adjust the zero potentiometer for 0V out with no weight on the platform. Next, set the gain adjustment for 3.0000V out for a 300.00 pound platform weight. Repeat this procedure until both points are fixed.

Optically Coupled Switched Capacitor Instrumentation Amplifier

Figure 13 also uses optical techniques for performance enhancement. This switched capacitor based instrumentation amplifier is applicable to transducer signal conditioning where high common mode voltages exist. The circuit has the low offset and drift of the LTC1150 but also incorporates a novel switched-capacitor "front end" to achieve some specifications not available in a conventional instrumentation amplifier.

Common mode rejection ratio at DC for the front end exceeds 160dB. The amplifier will operate over a ±200V common mode range and gain accuracy and stability are limited only by external resistors. A1, a chopper stabilized unit, sets offset drift at 0.05μV/°C. The high common mode voltage capability of the design allows it to withstand transient and fault conditions often encountered in industrial environments.

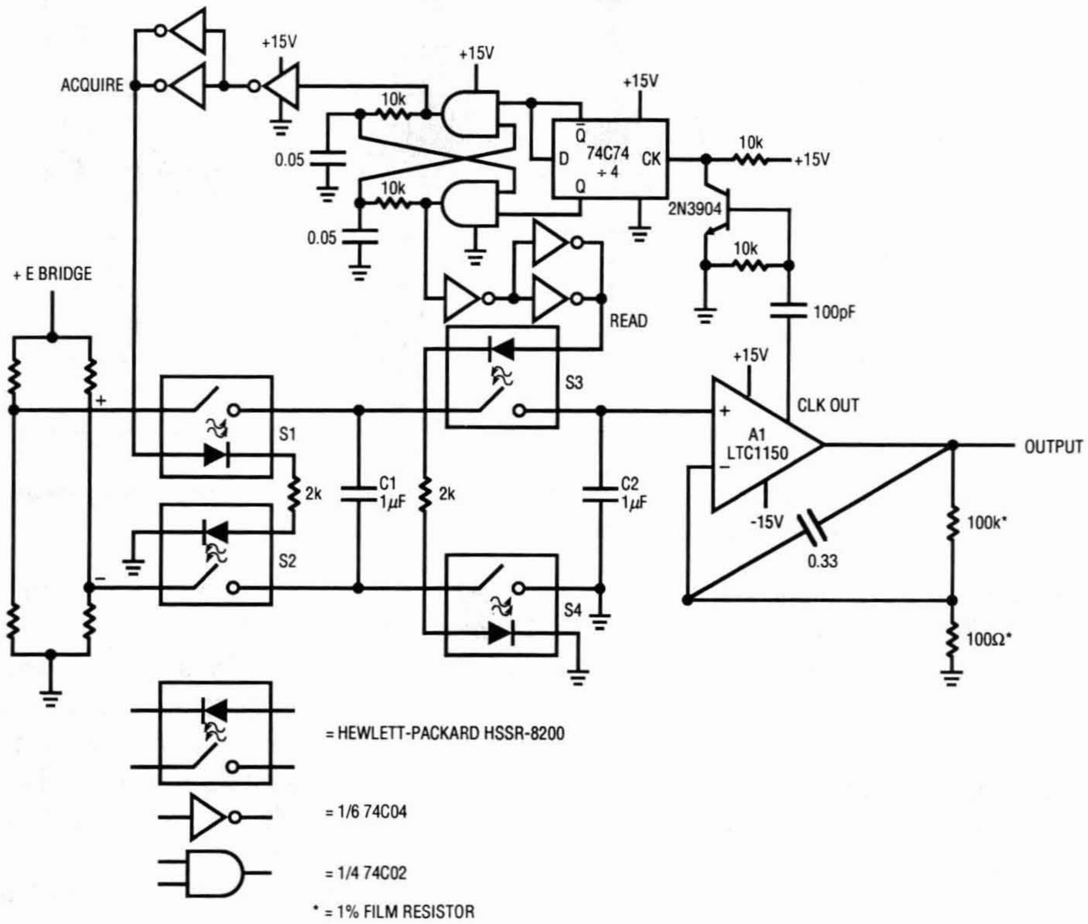
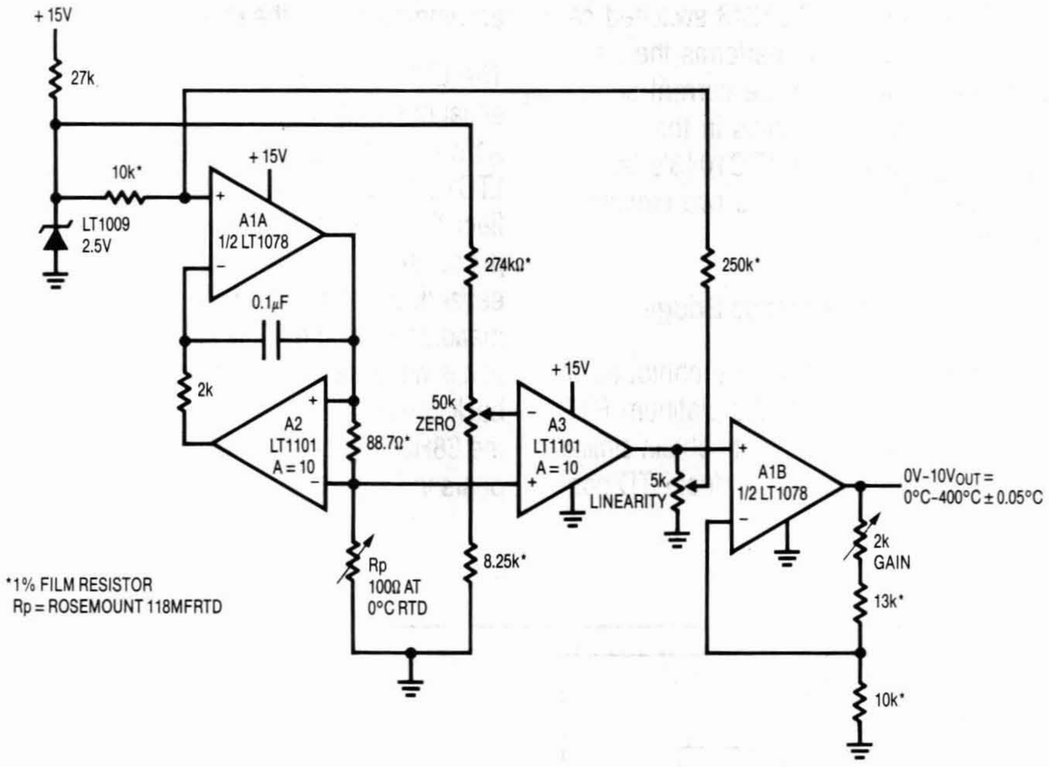


Figure 13. Floating Input Bridge Instrumentation Amplifier with 200V Common Mode Range

The circuit's inputs are fed to LED-driven optically-coupled MOSFET switches, S1 and S2. Two similar switches, S3 and S4, are in series with S1 and S2. CMOS logic functions, clocked from A1's internal oscillator, generate non-overlapping clock outputs which drive the switch's LEDs. When the "acquire pulse" is high, S1 and S2 are on and C2 acquires the differential voltage at the bridge's output. During this interval, S3 and S4 are off. When the acquire pulse falls, S1 and S2 begin to go off. After a delay to allow S1 and S2 to fully open, the "read pulse" goes high, turning on S3 and S4. Now C1 appears as a ground-referred voltage source which is read by A1. C2 allows A1's input to retain C1's value when the circuit returns to the acquire mode. A1 provides the circuit's output. Its gain is set in normal fashion by feedback resistors. The 0.33µF feedback capacitor sets rolloff. The differential-to-single-ended transition performed by the switches and capacitors means that A1 never sees the input's common mode signal. The breakdown specification of the optically-driven MOSFET switch allows the circuit to withstand and operate at common mode levels of ±200V. In addition, the optical drive to the MOSFETs eliminates the charge injection problems common to FET switched capacitive networks.

Platinum RTD Resistance Bridge Circuits

Platinum RTDs are frequently used in bridge configurations for temperature measurement. Figure 14's circuit is highly accurate and features a ground referred RTD. The ground connection is highly desirable for noise rejection. The bridges RTD leg is driven by a current source while the opposing bridge branch is voltage biased. The current drive allows the voltage across the RTD to vary directly with its temperature induced resistance shift. The difference between this potential and that of the opposing bridge leg forms the bridges output.



*1% FILM RESISTOR
Rp = ROSEMOUNT 118MFRTD

Figure 14. Linearized Platinum RTD Bridge. Feedback to Bridge from A3 Linearizes the Circuit.

A1A and instrumentation amplifier A2 form a voltage controlled current source. A1A, biased by the LT1009 reference, drives current through the 88.7Ω resistor and the RTD. A2, sensing differentially across the 88.7Ω resistor, closes a loop back to A1A. The 2k-0.1μF combination sets amplifier rolloff, and the configuration is stable. Because A1A's loop forces a fixed voltage across the 88.7Ω resistor, the current through Rp is constant. A1's operating point is primarily fixed by the 2.5V LT1009 voltage reference.

The RTD's constant current forces the voltage across it to vary with its resistance, which has a nearly linear positive temperature coefficient. The non-linearity could cause several degrees of error over the circuit's 0°C-400°C operating range. The bridges output is fed to instrumentation amplifier A3, which provides differential gain while simultaneously supplying non-linearity correction. The correction is implemented by feeding a portion of A3's output back to A1's input via the 10k-250k divider. This causes the current supplied to Rp to slightly shift with its operating point, compensating sensor non-linearity to within ±0.05°C. A1B, providing additional scaled gain, furnishes the circuit output.

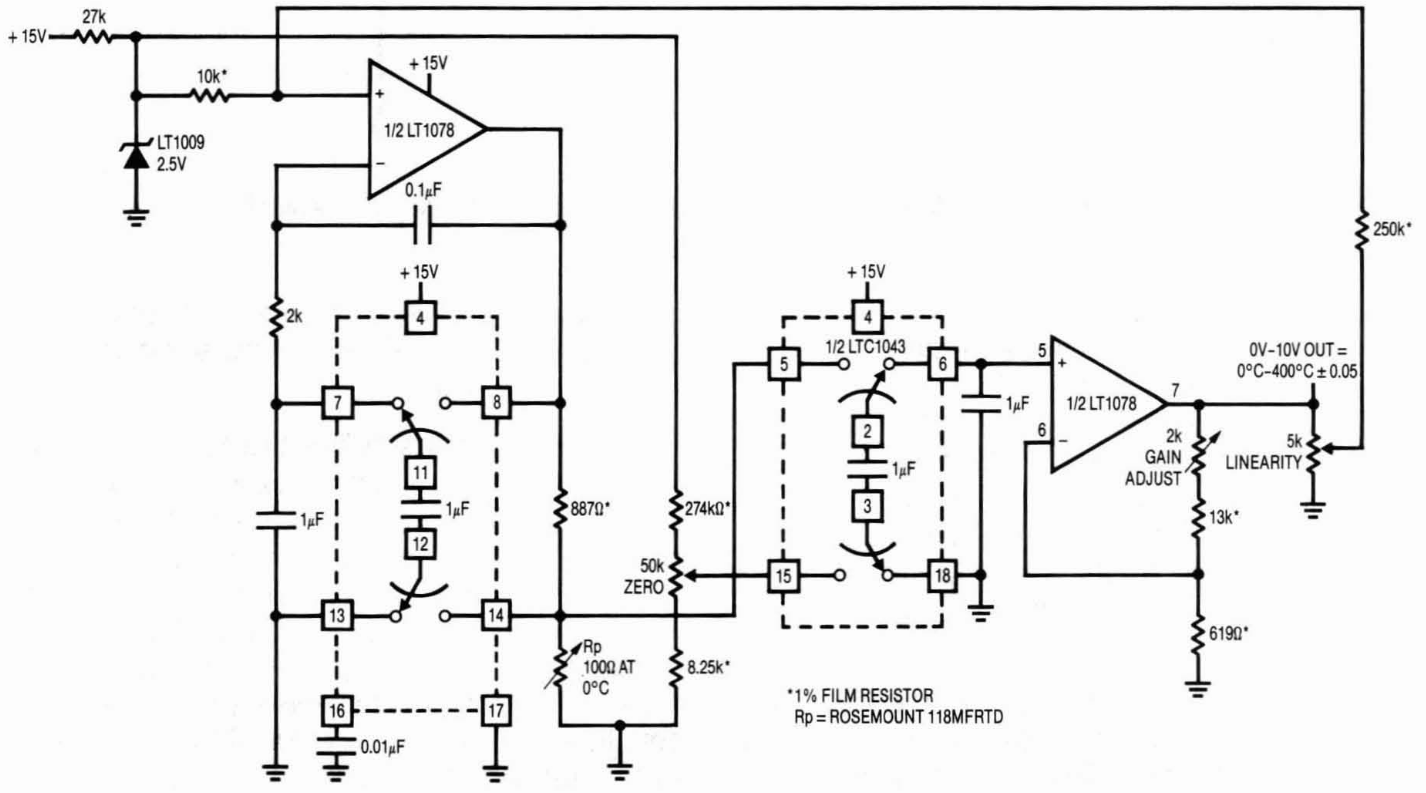
To calibrate this circuit, substitute a precision decade box (e.g., General Radio 1432k) for Rp. Set the box to the 0°C value (100.00Ω) and adjust the offset trim for a 0.00V output. Next, set the decade box for a 140°C output (154.26Ω) and adjust the gain trim for a 3.500V output reading. Finally, set the box to 249.0Ω (400.00°C) and trim the linearity adjustment for a 10.000V output. Repeat this sequence until all three points are fixed. Total error over the entire range will be within ±0.05°C. The resistance values given are for a nominal 100.00Ω (0°C) sensor. Sensors deviating from this nominal value can be used by factoring in the deviation from 100.00Ω. This deviation, which is manufacturer specified for each individual sensor, is an offset term due to winding tolerances during fabrication of the RTD. The gain slope of the platinum is primarily fixed by the purity of the material and has a very small error term.

Figure 15 is functionally identical to Figure 14, except that A2 and A3 are replaced with an LTC1043 switched capacitor building block. The LTC1043 performs the differential-to-single ended transitions in the current source and bridge output amplifier. Value shifts in the current source and output stage reflect the LTC1043's lack of gain. The primary trade-off between the two circuits is component count versus cost.

Digitally Corrected Platinum Resistance Bridge

The previous examples rely on analog techniques to achieve a precise, linear output from the platinum RTD bridge. Figure 16 uses digital corrections to obtain similar results. A processor is used to correct residual RTD non-linearities. The bridges inherent non-linear output is also accommodated by the processor.

The LT1027 drives the bridge with 5V. The bridge differential output is extracted by instrumentation amplifier A1. A1's output, via gain scaling stage A2, is fed to the LTC1290 12-bit A-D. The LTC1290's raw output codes reflect the bridges non-linear output vs temperature. The processor corrects the A-D output and presents linearized, calibrated data out. RTD and resistor tolerances mandate zero and full scale trims, but no linearity correction is necessary. A2's analog output is available for feedback control applications. The complete software code for the 68HC05 processor, developed by Guy M. Hoover, appears in Figure 17.


+15V
27k
10k*
LT1009
2.5V
+15V
1/2 LT1078
0.1µF
2k
+15V
4
7
8
11
1µF
12
1µF
13
14
16
17
0.01µF
887Ω*
274kΩ*
50k
ZERO
Rp
100Ω AT
0°C
8.25k*
+15V
4
1/2 LTC1043
5
6
2
1µF
3
15
18
1µF
5
6
1/2 LT1078
7
2k
GAIN
ADJUST
13k*
619Ω*
250k*
5k
LINEARITY
0V–10V OUT =
0°C–400°C ± 0.05

*1% FILM RESISTOR
Rp = ROSEMOUNT 118MFRTD

Figure 15. Switched Capacitor Based Version of Figure 14

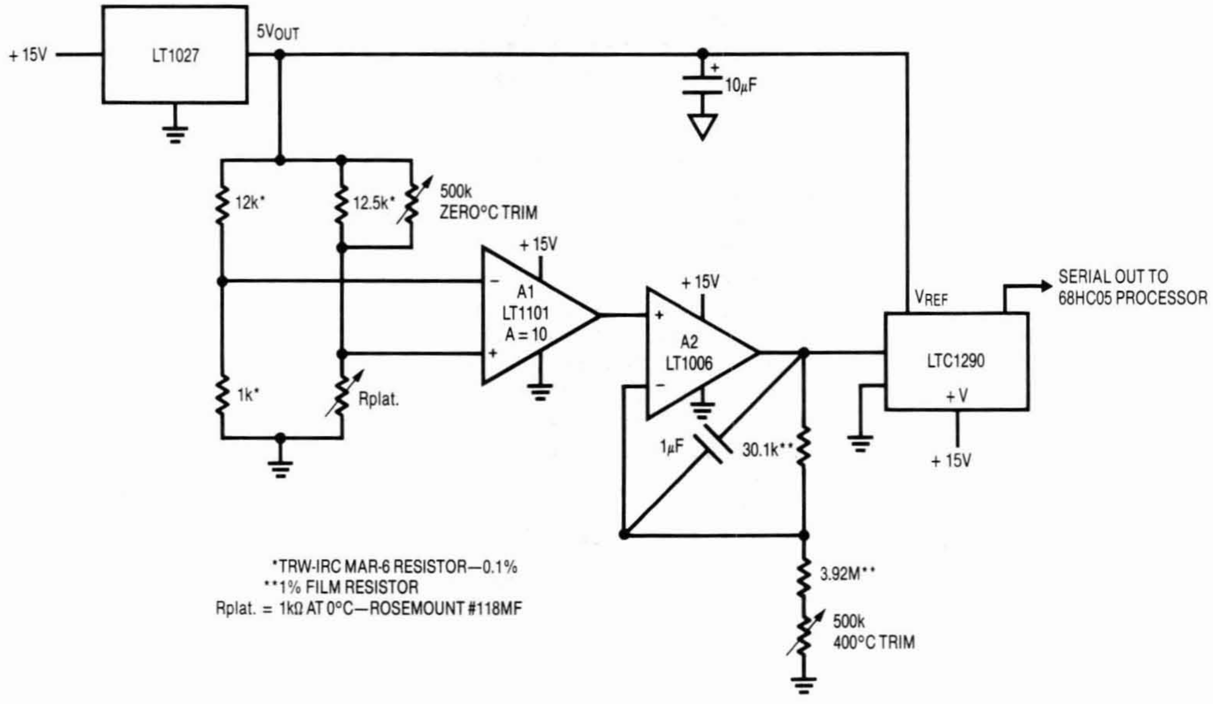
Thermistor Bridge

Figure 18, another temperature measuring bridge, uses a thermistor as a sensor. The LT1034 furnishes bridge excitation. The 3.2k and 6250Ω resistors are supplied with the thermistor sensor. The networks overall response is linearly related to the thermistor's sensed temperature. The network forms one leg of a bridge with resistors furnishing the opposing leg. A trim in this opposing leg sets bridge output to zero at 0°C. Instrumentation amplifier A1 takes gain with A2 providing additional trimmed gain to furnish a calibrated output. Calibration is accomplished in similar fashion to the platinum RTD circuits, with the linearity trim deleted.

Low Power Bridge Circuits

Low power operation of bridge circuits is becoming increasingly common. Many bridge based transducers are low impedance devices, complicating low power design. The most obvious way to minimize bridge power consumption is to restrict drive to the bridge. Figure 19A is identical to Figure 5, except that the bridge excitation has been reduced to 1.2V. This cuts bridge current from nearly 30mA to about 3.5mA. The remaining circuit elements consume negligible power compared to this amount. The trade-off is the sacrifice in bridge output signal. The reduced drive causes commensurately lowered bridge outputs, making the noise and drift floor a greater percentage of the signal. More specifically, a 0.01% reading of a 10V powered 350Ω strain gauge bridge requires $3\mu V$ of stable resolution. At 1.2V drive, this number shrinks to a scary 360nV.

Figure 19B is similar, although bridge current is reduced below $700\mu A$. This is accomplished by using a semiconductor based bridge transducer. These devices have significantly higher input resistance, minimizing power dissipation. Semiconductor based pressure transducers have major cost advantages over bonded strain gauge types, although accuracy and stability are reduced. Appendix A, "Strain Gauge Bridges," discusses trade-offs and theory of both technologies.



*TRW-IRC MAR-6 RESISTOR—0.1%
**1% FILM RESISTOR
Rplat. = 1kΩ AT 0°C—ROSEMOUNT #118MF

Figure 16. Digitally Linearized Platinum RTD Signal Conditioner

```
*          PLATINUM RTD LINEARIZATION PROGRAM (0.0 TO 400.0 DEGREES C)
*             WRITTEN BY GUY HOOVER LINEAR TECHNOLOGY CORPORATION
*                                 3/14/90
*        N IS THE NUMBER OF SEGMENTS THAT RTD RESPONSE IS DIVIDED INTO
*                       TEMPERATURE (DEG. C*10)=M*X+B
*              M IS SLOPE OF RTD RESPONSE FOR A GIVEN SEGMENT
*                 X IS A/D OUTPUT MINUS SEGMENT END POINT
*              B IS SEGMENT START POINT IN DEGREES C *10.
*
*****************************************************************************
*                           LOOK UP TABLES
*
        ORG  $1000
*                 TABLE FOR SEGMENT END POINTS IN DECIMAL
*   X IS FORMED BY SUBTRACTING PROPER SEGMENT END POINT FROM A/D OUTPUT
        FDB  60,296,527,753,976,1195,1410,1621,1829,2032
        FDB  2233,2430,2623,2813,3000,3184,3365,3543,3718,3890
        ORG  $1030
*                         TABLE FOR M IN DECIMAL
*            M IS SLOPE OF RTD OVER A GIVEN TEMPERATURE RANGE
        FDB  3486,3535,3585,3685,3735,3784,3884,3934,3984,4083
        FDB  4133,4232,4282,4382,4432,4531,4581,4681,4730,4830
        ORG  $1060
*                         TABLE FOR B IN DECIMAL
*                        B IS DEGREES C TIMES TEN
        FDB  0,200,400,600,800,1000,1200,1400,1600,1800
        FDB  2000,2200,2400,2600,2800,3000,3200,3400,3600,3800
        ORG  $10FF
        FCB  39        (N*2)-1 IN DECIMAL
*
*                           END LOOK UP TABLES
*****************************************************************************
*                           BEGIN MAIN PROGRAM
*
        ORG  $0100
        LDA  #$F7      CONFIGURATION DATA FOR PORT C DDR
        STA  $06       LOAD CONFIGURATION DATA INTO PORT C
        BSET 0,$02     INITIALIZE B0 PORT C
MES90L  NOP
        LDA  #$2F      DIN WORD FOR 1290 CH4 WITH RESPECT
*                      TO CH5, MSB FIRST, UNIPOLAR,16 BITS
        STA  $50       STORE DIN WORD IN DIN BUFFER
        JSR  READ90    CALL READ90 SUBROUTINE (DUMMY READ)
        JSR  READ90    CALL READ90 SUBROUTINE (MSBS IN $61 LSBS IN $62)
        LDX  $10FF     LOAD SEGMENT COUNTER INTO X \ FOR N=20 TO 1
DOAGAIN LDA  $1000,X   LOAD LSBS OF SEGMENT N        \
        STA  $55       STORE LSBS IN $55              \
        DECX           DECREMENT X                     \
        LDA  $1000,X   LOAD MSBS OF SEGMENT N           \
        STA  $54       STORE MSBS IN $54                 \ FIND B
        JSR  SUBTRCT   CALL SUBTRCT SUBROUTINE           /
        BPL  SEGMENT   IF RESULT IS PLUS GOTO SEGMENT   /
        JSR  ADDB      CALL ADDB SUBROUTINE            /
        DECX           DECREMENT X                    /
        JMP  DOAGAIN   GOTO CODE AT LABEL DOAGAIN    / NEXT N
```

Figure 17. Software Code for 68HC05 Processor Based RTD Linearization

```
*
*
*
*
*
SEGMENT LDA  $1030,X   LOAD MSBS OF SLOPE              \
        STA  $54       STORE MSBS IN $54                \
        INCX           INCREMENT X                       \ M*X
        LDA  $1030,X   LOAD LSBS OF SLOPE                /
        STA  $55       STORE LSBS IN $55                /
        JSR  TBMULT    CALL TBMULT SUBROUTINE          /
        LDA  $1060,X   LOAD LSBS OF BASE TEMP          \
        STA  $55       STORE LSBS IN $55                \
        DECX           DECREMENT X                       >B ADDED TO M*X
        LDA  $1060,X   LOAD MSBS OF BASE TEMP           /
        STA  $54       STORE MSBS IN $54               /
        JSR  ADDB      CALL ADDB SUBROUTINE
*                      TEMPERATURE IN DEGREES C * 10 IS IN $61 AND $62
*                        END MAIN PROGRAM
****************************************************************************
*
*
        JMP  MES90L    RUN MAIN PROGRAM IN CONTINUOUS LOOP
*
****************************************************************************
*                      SUBROUTINES BEGIN HERE
*
****************************************************************************
*       READ90 READS THE LTC1290 AND STORES THE RESULT IN $61 AND $62
*
READ90  LDA  #$50      CONFIGURATION DATA FOR SPCR \
        STA  $0A       LOAD CONFIGURATION DATA      > CONFIGURE PROCESSOR
        LDA  $50       LOAD DIN WORD INTO THE ACC  /
        BCLR 0,$02     BIT 0 PORT C GOES LOW (CS GOES LOW)         \
        STA  $0C       LOAD DIN INTO SPI DATA REG. START TRANSFER. |
BACK90  TST  $0B       TEST STATUS OF SPIF                         |
        BPL  BACK90    LOOP TO PREVIOUS INSTRUCTION IF NOT DONE    |
        LDA  $0C       LOAD CONTENTS OF SPI DATA REG. INTO ACC     |
        STA  $0C       START NEXT CYCLE                            |
        STA  $61       STORE MSBS IN $61                           | XFER
BACK92  TST  $0B       TEST STATUS OF SPIF                         | DATA
        BPL  BACK92    LOOP TO PREVIOUS INSTRUCTION IF NOT DONE    |
        BSET 0,$02     SET BIT 0 PORT C (CS GOES HIGH)             |
        LDA  $0C       LOAD CONTENTS OF SPI DATA REG INTO ACC      |
        STA  $62       STORE LSBS IN $62                          /
        LDA  #$04      LOAD COUNTER WITH NUMBER OF SHIFTS     \
SHIFT   CLC            CLEAR CARRY                             \
        ROR  $61       ROTATE MSBS RIGHT THROUGH CARRY          \ RIGHT
        ROR  $62       ROTATE LSBS RIGHT THROUGH CARRY          / JUSTIFY
        DECA           DECREMENT COUNTER                       /  DATA
        BNE  SHIFT     IF NOT DONE SHIFTING THEN REPEAT LOOP  /
        RTS            RETURN TO MAIN PROGRAM
*
*                          END READ90
****************************************************************************
```

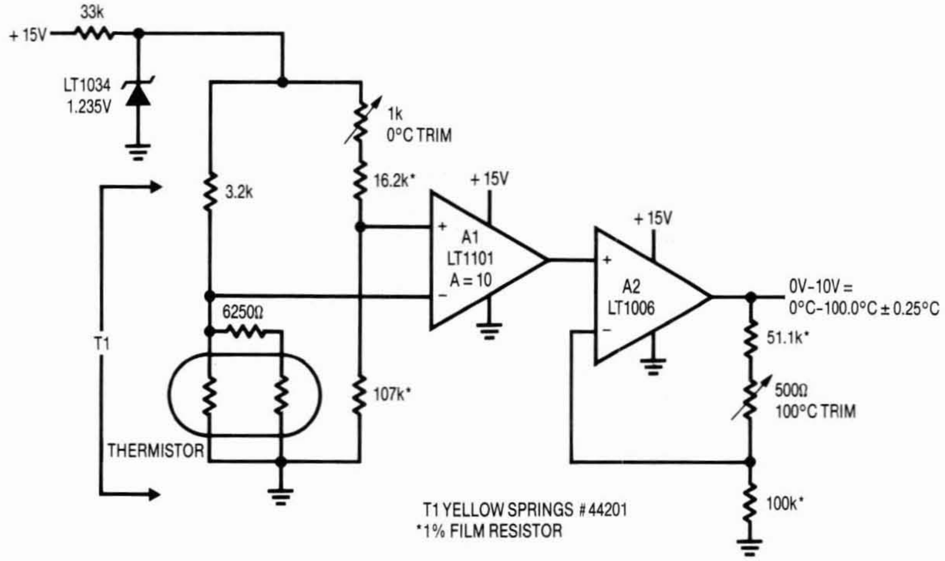
Figure 17. Software Code for 68HC05 Processor Based RTD Linearization (Continued)

```
***************************************************************************
*
*  SUBTRCT SUBTRACTS $54 AND $55 FROM $61 AND $62. RESULTS IN $61 AND $62
*
SUBTRCT LDA  $62       LOAD LSBS
        SUB  $55       SUBTRACT LSBS
        STA  $62       STORE REMAINDER
        LDA  $61       LOAD MSBS
        SBC  $54       SUBTRACT W/CARRY MSBS
        STA  $61       STORE REMAINDER
        RTS            RETURN TO MAIN PROGRAM
*
*                            END SUBTRCT
****************************************************************************
****************************************************************************
*
*ADDB RESTORES $61 AND $62 TO ORIGINAL VALUES AFTER SUBTRCT HAS BEEN PERFORMED
*
ADDB    LDA  $62       LOAD LSBS
        ADD  $55       ADD LSBS
        STA  $62       STORE SUM
        LDA  $61       LOAD MSBS
        ADC  $54       ADD W/CARRY MSBS
        STA  $61       STORE SUM
        RTS            RETURN TO MAIN PROGRAM
*
*                         END ADDB
****************************************************************************
****************************************************************************
*
*TBMULT MULTIPLIES CONTENTS OF $61 AND $62 BY CONTENTS OF $54 AND $55.
*16 MSBS OF RESULT ARE PLACED IN $61 AND $62
*
TBMULT  CLR  $68       CLEAR CONTENTS OF $68   \
        CLR  $69       CLEAR CONTENTS OF $69    \ RESET TEMPORARY
        CLR  $6A       CLEAR CONTENTS OF $6A    / RESULT REGISTERS
        CLR  $6B       CLEAR CONTENTS OF $6B   /
        STX  $58       STORE CONTENTS OF X IN $58. TEMPORARY HOLD REG. FOR X
        LSL  $62       MULTIPLY LSBS BY 2 \
        ROL  $61       MULTIPLY MSBS BY 2   \
        LSL  $62       MULTIPLY LSBS BY 2     \
        ROL  $61       MULTIPLY MSBS BY 2       \ MULTIPLY $61 AND $62 BY 16
        LSL  $62       MULTIPLY LSBS BY 2       / FOR SCALING PURPOSES
        ROL  $61       MULTIPLY MSBS BY 2     /
        LSL  $62       MULTIPLY LSBS BY 2   /
        ROL  $61       MULTIPLY MSBS BY 2 /
        LDA  $62       LOAD LSBS OF 1290 INTO ACC
        LDX  $55       LOAD LSBS OF M INTO X
        MUL            MULTIPLY CONTENTS OF $55 BY CONTENTS OF $62
        STA  $6B       STORE LSBS IN $6B
        STX  $6A       STORE MSBS IN $6A
        LDA  $62       LOAD LSBS OF 1290 INTO ACC
        LDX  $54       LOAD MSBS OF M INTO X
        MUL            MULTIPLY CONTENTS OF $54 BY CONTENTS OF $62
        ADD  $6A       LSBS OF MULTIPLY ADDED TO $6A
        STA  $6A       STORE BYTE
        TXA            TRANSFER X TO ACC
        ADC  $69       ADD NEXT BYTE
        STA  $69       STORE BYTE
```

Figure 17. Software Code for 68HC05 Processor Based RTD Linearization (Continued)

```
         LDA   $61        LOAD MSBS OF 1290 INTO ACC
         LDX   $55        LOAD LSBS OF M INTO X
         MUL              MULTIPLY CONTENTS OF $55 BY CONTENTS OF $61
         ADD   $6A        ADD NEXT BYTE
         STA   $6A        STORE BYTE
         TXA              TRANSFER X TO ACC
         ADC   $69        ADD NEXT BYTE
         STA   $69        STORE BYTE
         LDA   $61        LOAD MSBS OF 1290 INTO ACC
         LDX   $54        LOAD MSBS OF M INTO X
         MUL              MULTIPLY CONTENTS OF $54 BY CONTENTS OF $61
         ADD   $69        ADD NEXT BYTE
         STA   $69        STORE BYTE
         TXA              TRANSFER X TO ACC
         ADC   $68        ADD NEXT BYTE
         STA   $68        STORE BYTE
         LDA   $6A        LOAD CONTENTS OF $6A INTO ACC
         BPL   NNN        IF NO CARRY FROM $6A GOTO LABEL NNN
         LDA   $69        LOAD CONTENTS OF $69 INTO ACC
         ADD   #$01       ADD 1 TO ACC
         STA   $69        STORE IN $69
         LDA   $68        LOAD CONTENTS OF $68 INTO ACC
         ADC   #$00       FLOW THROUGH CARRY
         STA   $68        STORE IN $68
NNN      LDA   $68        LOAD CONTENTS OF $68 INTO ACC
         STA   $61        STORE MSBS IN $61
         LDA   $69        LOAD CONTENTS OF $69 INTO ACC
         STA   $62        STORE IN $62
         LDX   $58        RESTORE X REGISTER FROM $58
         RTS              RETURN TO MAIN PROGRAM
*
*                          END TBMULT
*****************************************************************************
*
*                            END
*****************************************************************************
```

Figure 17. Software Code for 68HC05 Processor Based RTD Linearization (Continued)


33k
+15V
LT1034
1.235V
1k
0°C TRIM
16.2k*
+15V
3.2k
A1
LT1101
A = 10
+15V
A2
LT1006
0V–10V =
0°C–100.0°C ± 0.25°C
6250Ω
T1
51.1k*
500Ω
100°C TRIM
107k*
THERMISTOR
100k*

T1 YELLOW SPRINGS #44201
*1% FILM RESISTOR

Figure 18. Linear Output Thermistor Bridge. Thermistor Network Provides Linear Bridge Output.

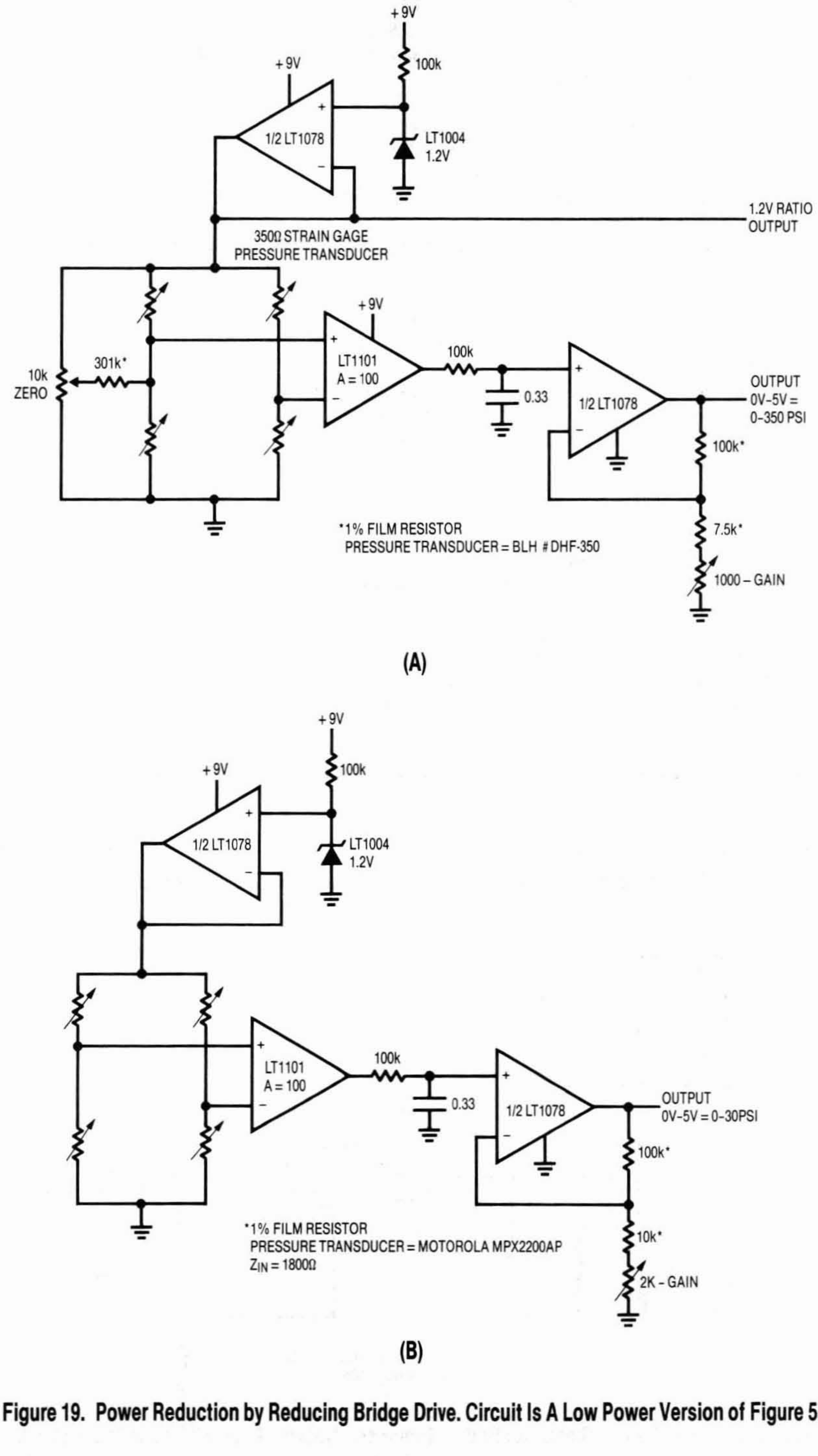

+9V
+9V
100k
1/2 LT1078
LT1004
1.2V
1.2V RATIO
OUTPUT
350Ω STRAIN GAGE
PRESSURE TRANSDUCER
+9V
LT1101
A = 100
100k
10k
ZERO
301k*
0.33
1/2 LT1078
OUTPUT
0V–5V =
0–350 PSI
100k*
*1% FILM RESISTOR
PRESSURE TRANSDUCER = BLH # DHF-350
7.5k*
1000 – GAIN
(A)
+9V
+9V
100k
1/2 LT1078
LT1004
1.2V
LT1101
A = 100
100k
0.33
1/2 LT1078
OUTPUT
0V–5V = 0–30PSI
100k*
*1% FILM RESISTOR
PRESSURE TRANSDUCER = MOTOROLA MPX2200AP
Z_{IN} = 1800Ω
10k*
2K – GAIN
(B)

Figure 19. Power Reduction by Reducing Bridge Drive. Circuit Is A Low Power Version of Figure 5.

Strobed Power Bridge Drive

Figure 20, derived directly from Figure 10, is a simple way to reduce power without sacrificing bridge signal output level. The technique is applicable where continuous output is not a requirement. This circuit is designed to sit in the quiescent state for long periods with relatively brief on-times. A typical application would be remote weight information in storage tanks where weekly readings are sufficient. Quiescent current is about 150µA with on-state current typically 50mA. Bridge power is conserved by simply turning it off.

With Q1's base unbiased, all circuitry is off except the LT1054 plus-to-minus voltage converter, which draws a 150µA quiescent current. When Q1's base is pulled low, its collector supplies power to A1 and A2. A1's output goes high, turning on the LT1054. The LT1054's output (pin 5) heads toward -5V and Q2 comes on, permitting bridge current to flow. To balance its inputs, A1 servo controls the LT1054 to force the bridge's midpoint to 0V. The bridge ends up with about 8V across it, requiring the 100mA capability LT1054 to sink about 24mA. The 0.02µF capacitor stabilizes the loop. The A1-LT1054 loop's negative output sets the bridge's common mode voltage to zero, allowing A2 to take a simple single ended measurement. The "output trim" scales the circuit for 3mV/V type strain bridge transducers, and the 100k-0.1µF combination provides noise filtering.

Sampled Output Bridge Signal Conditioner

Figure 21, an obvious extension of Figure 20, automates the strobing into a clocked sequence. Circuit on-time is restricted to 250µs, at a clock rate of about 2Hz. This keeps average power consumption down to about 200µA. Oscillator A1A produces a 250µs clock pulse every 500ms (trace A, Figure 22). A filtered version of this pulse is fed to Q1, whose emitter (trace B) provides slew limited bridge drive. A1A's output also triggers a delayed pulse produced by the 74C221 one-shot output (trace C). The timing is arranged so the pulse occurs well after the A1B-A2 bridge amplifier output (trace D) settles. A monitoring A-D converter, triggered by this pulse, can acquire A1B's output.

The slew limited bridge drive prevents the strain gauge bridge from seeing a fast rise pulse, which could cause long term transducer degradation. To calibrate this circuit trim zero and gain for appropriate outputs.

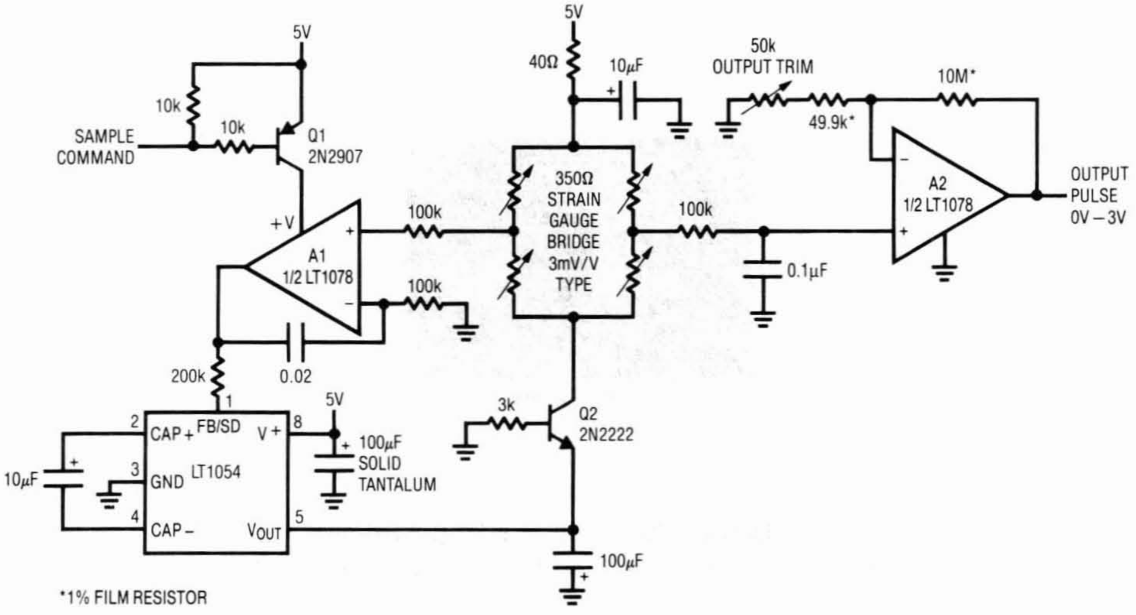
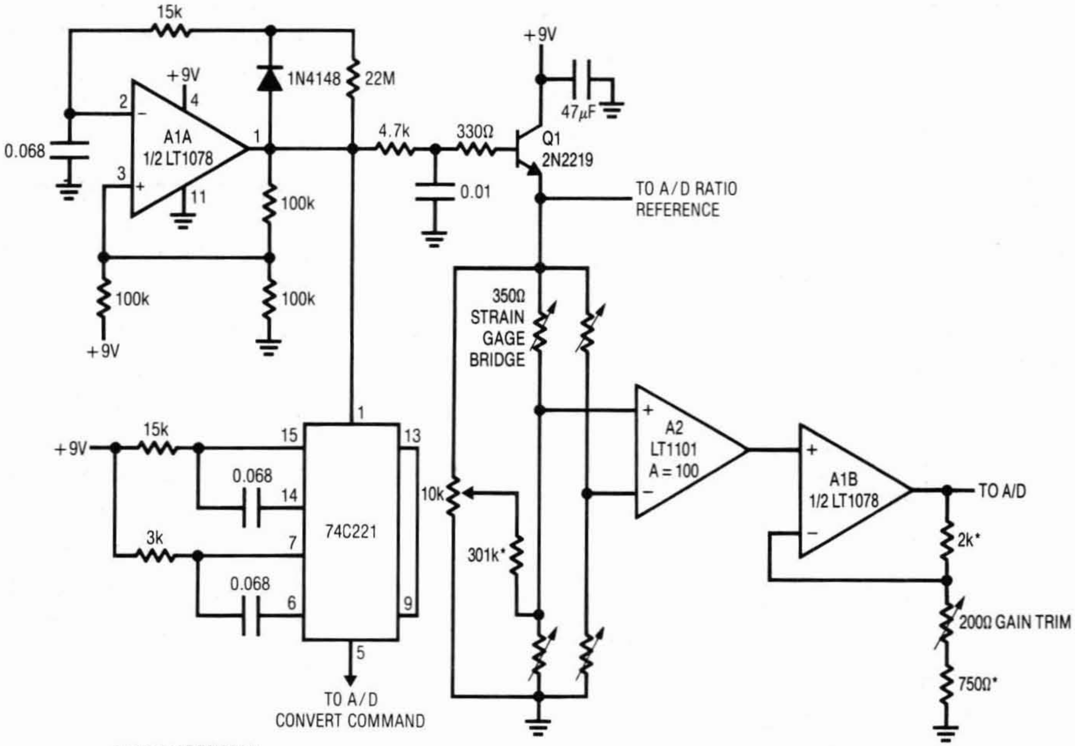

5V
10k
10k
SAMPLE COMMAND
Q1
2N2907
+V
A1
1/2 LT1078
100k
100k
0.02
200k
1
2
3
4
8
5
CAP+
FB/SD
V+
GND
LT1054
CAP−
VOUT
10µF
5V
100µF
SOLID
TANTALUM
3k
Q2
2N2222
100µF
5V
40Ω
10µF
350Ω
STRAIN
GAUGE
BRIDGE
3mV/V
TYPE
50k
OUTPUT TRIM
49.9k*
10M*
100k
0.1µF
A2
1/2 LT1078
OUTPUT
PULSE
0V – 3V
*1% FILM RESISTOR

Figure 20. Strobed Power Strain Gauge Bridge Signal Conditioner


15k
+9V
1N4148
22M
0.068
2
4
A1A
1/2 LT1078
1
3
11
100k
100k
100k
+9V
4.7k
330Ω
0.01
+9V
47µF
Q1
2N2219
TO A/D RATIO
REFERENCE
350Ω
STRAIN
GAGE
BRIDGE
A2
LT1101
A = 100
A1B
1/2 LT1078
TO A/D
2k*
200Ω GAIN TRIM
750Ω*
+9V
15k
0.068
3k
0.068
15
14
7
6
1
13
9
5
74C221
10k
301k*
TO A/D
CONVERT COMMAND

*1% FILM RESISTOR

Figure 21. Sampled Output Bridge Signal Conditioner Uses Pulsed Excitation to Save Power

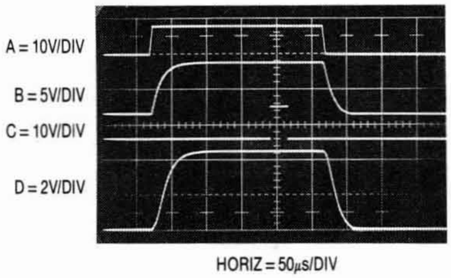
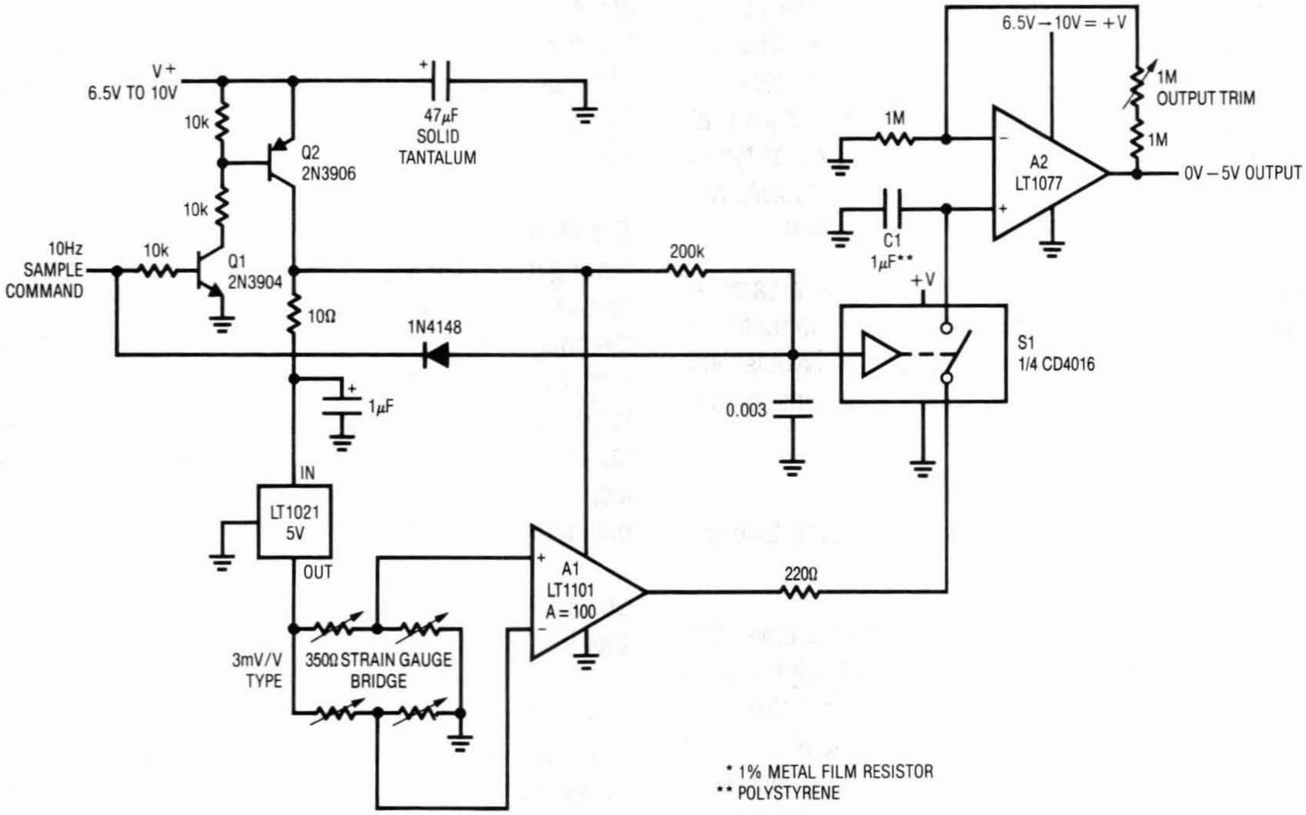


Figure 22. Figure 21's Waveforms. Trace C's Delayed Pulse Ensures A→D Converter Sees Settled Output Waveform (Trace D).

Continuous Output Sampled Bridge Signal Conditioner

Figure 23 extends the sampling approach to include a continuous output. This is accomplished by adding a sample-hold stage at the circuit output. In this circuit, Q2 is off when the "sample command" is low. Under these conditions only A2 and S1 receive power, and current drain is inside 60μA. When the sample command is pulsed high, Q2's collector (trace A, Figure 24) goes high, providing power to all other circuit elements. The 10Ω-1μF RC at the LT1021 prevents the strain bridge from seeing a fast rise pulse, which could cause long term transducer degradation. The LT1021-5 reference output (trace B) drives the strain bridge, and instrumentation amplifier A1 output responds (trace C). Simultaneously, S1's switch control input (trace D) ramps toward Q2's collector.



V+
6.5V TO 10V
10k
Q2
2N3906
47µF
SOLID
TANTALUM
10k
10Hz
SAMPLE
COMMAND
10k
Q1
2N3904
10Ω
1N4148
200k
1µF
IN
LT1021
5V
OUT
A1
LT1101
A = 100
3mV/V
TYPE
350Ω STRAIN GAUGE
BRIDGE
0.003
S1
1/4 CD4016
+V
C1
1µF**
1M
A2
LT1077
6.5V – 10V = +V
1M
OUTPUT TRIM
1M
0V – 5V OUTPUT
220Ω
* 1% METAL FILM RESISTOR
** POLYSTYRENE

Figure 23. Pulsed Excitation Bridge Signal Conditioner. Sample-Hold Stage Gives DC Output.

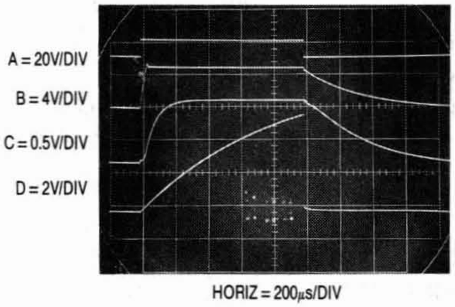


Figure 24. Waveforms for Figure 23's Sampled Strain Gauge Signal Conditioner

At about one-half Q2's collector voltage (in this case just before mid-screen) S1 turns on, and A1's output is stored in C1. When the sample command drops low, Q2's collector falls, the bridge and its associated circuitry shut down and S1 goes off. C1's stored value appears at gain scaled A2's output. The RC delay at S1's control input ensures glitch free operation by preventing C1 from updating until A1 has settled. During the 1ms sampling phase, supply current approaches 20mA but a 10Hz sampling rate cuts effective drain below 250μA. Slower sampling rates will further reduce drain, but C1's droop rate (about 1mV/100ms) sets an accuracy constraint. The 10Hz rate provides adequate bandwidth for most transducers. For 3mV/V slope factor transducers the gain trim shown allows calibration. It should be rescaled for other types. This circuit's effective current drain is about 250μA, and A2's output is accurate enough for 12-bit systems.

It is important to remember that this circuit is a sampled system. Although the output is continuous, information is being collected at a 10Hz rate. As such, the Nyquist limit applies, and must be kept in mind when interpreting results.

High Resolution Continuous Output Sampled Bridge Signal Conditioner

Figure 25 is a special case of sampled bridge drive. It is intended for applications requiring extremely high resolution outputs from a bridge transducer. This circuit puts 100V across a 10V, 350Ω strain gauge bridge for short periods of time. The high pulsed voltage drive increases bridge output proportionally, without forcing excessive dissipation. In fact, although this circuit is not intended for power reduction, average bridge power is far below the normal 29mA obtained with $10V_{DC}$ excitation.

Combining the 10x higher bridge gain (300mV full scale vs the normal 30mV) with a chopper stabilized amplifier in the sample-hold output stage is the key to the high resolution obtainable with this circuit.

When oscillator A1A's output is high Q6 is turned on and A2's negative input is pulled above ground. A2's output goes negative, turning on Q1. Q1's collector goes low, robbing Q3's base drive and cutting it off. Simultaneously, A3 enforces it's loop by biasing Q2 into conduction, softly turning on Q4. Under these conditions the voltage across the bridge is essentially zero. When A1A oscillates low (trace A, Figure 26) RC filter driven Q6 responds by cutting off slowly. Now, A2's negative input sees current only through the 3.6k resistor. The input begins to head negative, causing A2's output to rise. Q1 comes out of saturation, and Q3's emitter (trace B) rises. Initially this action is rapid (fast rise slewing is just visible at the start of Q3's ascent), but feedback to A2's negative input closes a control loop, with the 1000pF capacitor restricting rise time. The 72k resistor sets A2's gain at 20 with respect to the LT1004 2.5V reference, and Q3's emitter servo controls to 50V.

Simultaneously, A3 responds to the bridges biasing by moving its output negatively. Q2 tends towards cut-off, increasing Q4's conduction. A3 biases it's loop to maintain the bridge mid-point at zero. To do this, it must produce a complimentary output to A2's loop, which trace C shows to be the case. Note that A3's loop rolloff is considerably faster than A2's,ensuring that it will faithfully track A2's loop action. Similarly, A3's loop is slaved to A2's loop output, and produces no other outputs.

Under these conditions the bridge sees 100V drive across it for the 1ms duration of the clock pulse.

A1A's clock output also triggers the 74C221 one-shot. The one-shot delivers a delayed pulse (trace D) to Q5. Q5 comes on, charging the 1μF capacitor to the bridges output voltage. With A3 forcing the bridges left side mid-point to zero, Q5, the 1μF capacitor and A4 see a single-ended, low voltage signal. High transient common mode voltages are avoided by the control loops complimentary controlled rise times. A4 takes gain and provides the circuit output. The 74C221's pulse width ends during the bridges on-time, preserving sampled data integrity. When the A1A oscillator goes high the control loops remove bridge drive, returning the circuit to quiescence. A4's output is maintained at DC by the 1μF capacitor. A1A's 1Hz clock rate is adequate to prevent deleterious droop of the 1μF capacitor, but slow enough to limit bridge power dissipation. The

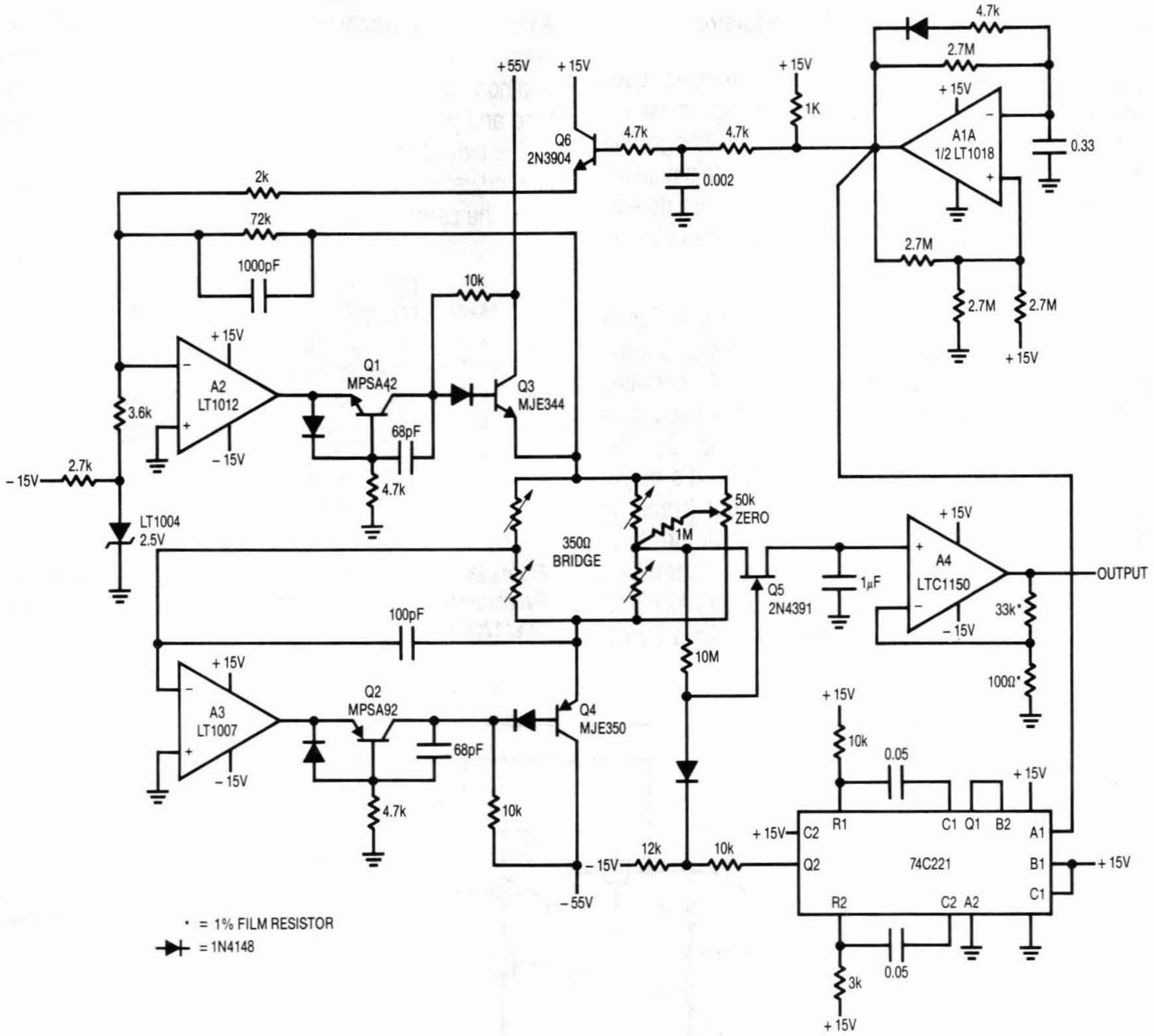

+55V
+15V
Q6
2N3904
4.7k
4.7k
0.002
+15V
1K
4.7k
2.7M
+15V
A1A
1/2 LT1018
0.33
2.7M
2.7M
2.7M
+15V
2k
72k
1000pF
10k
+15V
A2
LT1012
Q1
MPSA42
Q3
MJE344
3.6k
68pF
–15V
–15V
2.7k
4.7k
LT1004
2.5V
350Ω
BRIDGE
50k
ZERO
1M
Q5
2N4391
1µF
+15V
A4
LTC1150
–15V
OUTPUT
33k*
100Ω*
100pF
10M
+15V
A3
LT1007
Q2
MPSA92
Q4
MJE350
68pF
–15V
4.7k
10k
+15V
10k
0.05
+15V
R1
C1
Q1
B2
A1
+15V
C2
Q2
74C221
B1
+15V
R2
C2
A2
C1
–15V
12k
10k
–55V
0.05
3k
+15V
* = 1% FILM RESISTOR
= 1N4148

Figure 25. High Resolution Pulsed Excitation Bridge Signal Conditioner. Complementary 50V Drive Increases Bridge Output Signal.

controlled rise and fall times across the bridge prevent possible long term transducer degradation by eliminating high ΔV/ΔT induced effects.

When using this circuit it is important to remember that it is a sampled system. Although the output is continuous, information is being collected at a 1Hz rate. As such, the Nyquist limit applies, and must be kept in mind when interpreting results.

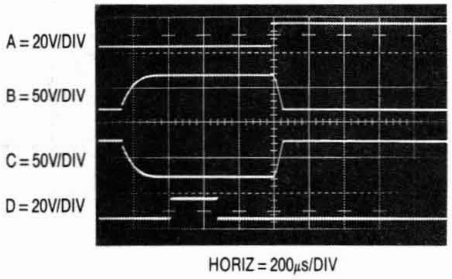


Figure 26. Figure 25's Waveforms. Drive Shaping Results in Controlled, Complementary Bridge Drive Waveforms. Bridge Power Is Low Despite 100V Excitation.

AC Driven Bridge/Synchronous Demodulator

Figure 27, an extension of pulse excited bridges, uses synchronous demodulation to obtain very high noise rejection capability. An AC carrier excites the bridge and synchronizes the gain stage demodulator. In this application, the signal source is a thermistor bridge which detects extremely small temperature shifts in a biochemical microcalorimetry reaction chamber.

The 500Hz carrier is applied at T1's input (trace A, Figure 28). T1's floating output drives the thermistor bridge, which presents a single-ended output to A1. A1 operates at an AC gain of 1000. A 60Hz broadband noise source is also deliberately injected into A1's input (trace B). The carrier's zero crossings are detected by C1. C1's output clocks the LTC1043 (trace C). A1's output (trace D) shows the desired 500Hz signal buried within the 60Hz noise source. The LTC1043's zero-cross-synchronized switching at A2's positive input (trace E) causes A2's gain to alternate between plus and minus one. As a result, A1's output is synchronously demodulated by A2. A2's output (trace F) consists of demodulated carrier signal and non-coherent components. The desired carrier amplitude and polarity information is discernible in A2's output and is extracted by filter-averaging at A3. To trim this circuit, adjust the phase potentiometer so that C1 switches when the carrier crosses through zero.

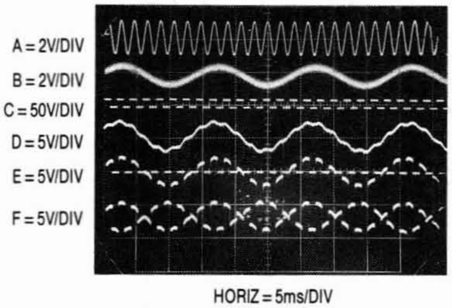
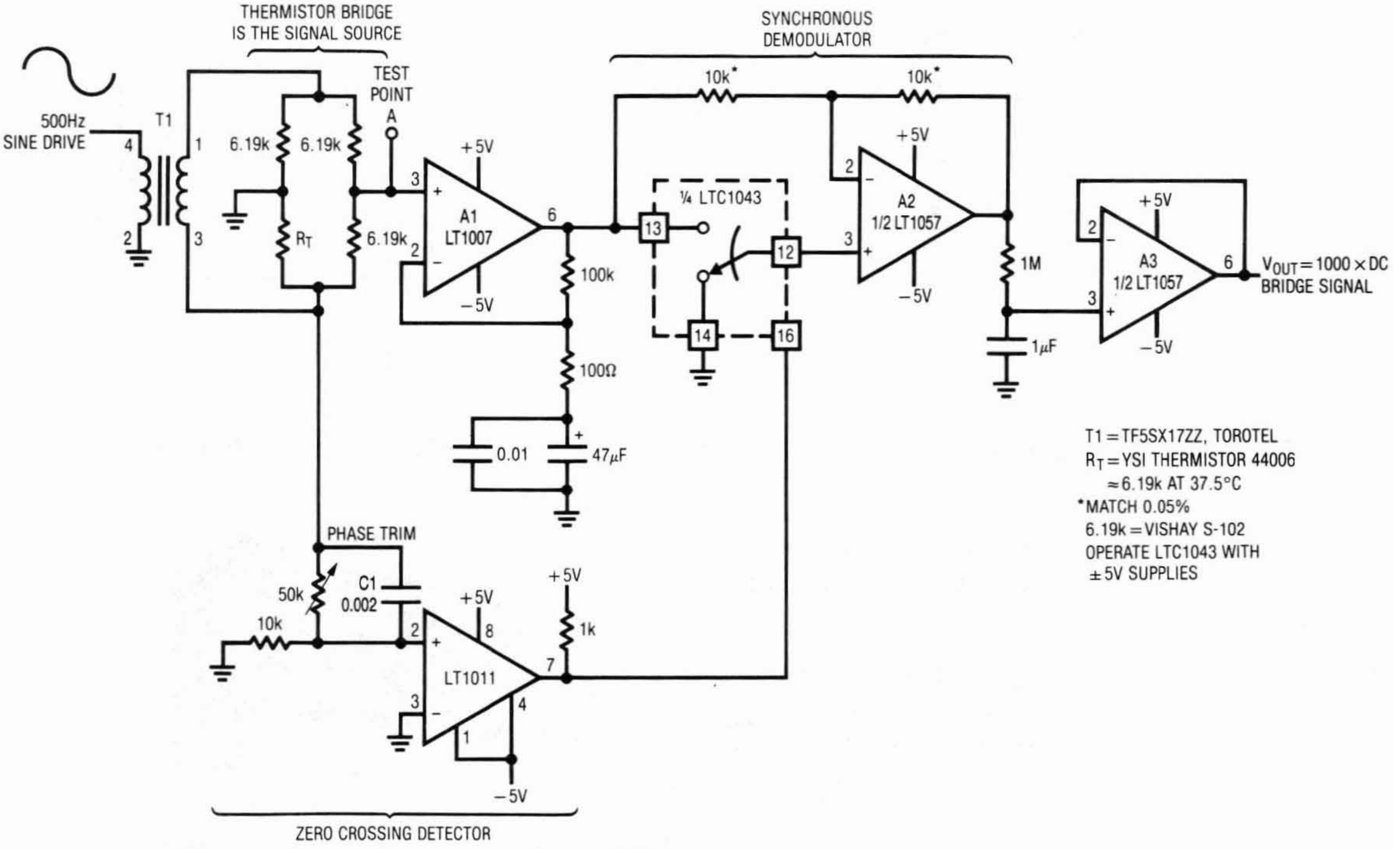


Figure 28. Details of Lock-In Amplifier Operation. Narrowband Synchronous Detection Permits Extraction of Coherent Signals Over 120dB Down.



THERMISTOR BRIDGE IS THE SIGNAL SOURCE
SYNCHRONOUS DEMODULATOR
500Hz SINE DRIVE
T1
4
2
1
3
6.19k
6.19k
6.19k
R_T
TEST POINT A
3
2
A1 LT1007
6
+5V
–5V
100k
100Ω
0.01
47µF
10k*
10k*
¼ LTC1043
13
12
14
16
2
3
A2 1/2 LT1057
+5V
–5V
1M
1µF
2
3
A3 1/2 LT1057
6
+5V
–5V
V_OUT = 1000 × DC BRIDGE SIGNAL
PHASE TRIM
50k
10k
C1 0.002
+5V
8
2
3
LT1011
7
4
1
+5V
1k
–5V
ZERO CROSSING DETECTOR
T1 = TF5SX17ZZ, TOROTEL
R_T = YSI THERMISTOR 44006
≈ 6.19k AT 37.5°C
*MATCH 0.05%
6.19k = VISHAY S-102
OPERATE LTC1043 WITH ±5V SUPPLIES

Figure 27. "Lock-In" Bridge Amplifier. Synchronous Detection Achieves Extremely Narrow Band Gain, Providing Very High Noise Rejection.

AC Driven Bridge for Level Transduction

Level transducers which measure angle from ideal level are employed in road construction, machine tools, inertial navigation systems and other applications requiring a gravity reference. One of the most elegantly simple level transducers is a small tube nearly filled with a partially conductive liquid. Figure 29A shows such a device. If the tube is level with respect to gravity, the bubble resides in the tube's center and the electrode resistances to common are identical. As the tube shifts away from level, the resistances increase and decrease proportionally. By controlling the tube's shape at manufacture it is possible to obtain a linear output signal when the transducer is incorporated in a bridge circuit.

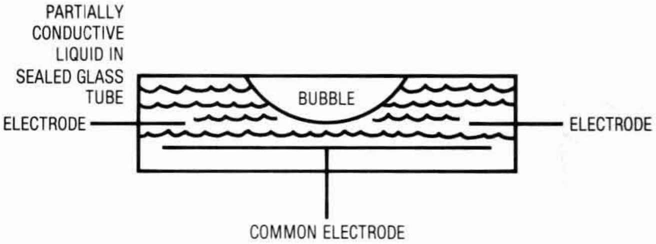


Figure 29A. Bubble Based Level Transducer

Transducers of this type must be excited with an AC waveform to avoid damage to the partially conductive liquid inside the tube. Signal conditioning involves generating this excitation as well as extracting angle information and polarity determination (e.g., which side of level the tube is on). Figure 29B shows a circuit which does this, directly producing a calibrated frequency output corresponding to level. A sign bit, also supplied at the output, gives polarity information.

The level transducer is configured with a pair of 2kΩ resistors to form a bridge. The required AC bridge excitation is developed at C1A, which is configured as a multi-vibrator. C1A biases Q1, which switches the LT1009's 2.5V potential through the 100µF capacitor to provide the AC bridge drive. The bridge differential output AC signal is converted to a current by A1, operating as a Howland current pump. This current, whose polarity reverses as bridge drive polarity switches, is rectified by the diode bridge. Thus, the 0.03µF capacitor receives unipolar charge. Instrumentation amplifier A2 measures the voltage across the capacitor and presents its single-ended output to C1B. When the voltage across the 0.03µF capacitor becomes high enough, C1B's output goes high, turning on the LTC201A switch. This discharges the capacitor. When C1B's AC positive feedback ceases, C1B's output goes low and the switch goes off. The 0.03µF unit again receives constant current charging and the entire cycle repeats. The frequency of this oscillation is determined by the magnitude of the constant current delivered to the bridge-capacitor configuration. This current's magnitude is set by the transducer bridge's offset, which is level related.

Figure 30 shows circuit waveforms. Trace A is the AC bridge drive, while trace B is A1's output. Observe that when the bridge drive changes polarity, A1's output flips sign rapidly to maintain a constant current into the bridge-capacitor configuration. A2's output (trace C) is a unipolar, ground-referred ramp. Trace D is C1B's output pulse and the circuit's output. The diodes at C1B's positive input provide temperature compensation for the sensor's positive tempco, allowing C1B's trip voltage to ratiometrically track bridge output over temperature.

A3, operating open loop, determines polarity by comparing the rectified and filtered bridge output signals with respect to ground.

To calibrate this circuit, place the level transducer at a known 40 arc-minute angle and adjust the 5kΩ trimmer at C1B for a 400Hz output. Circuit accuracy is limited by the transducer to about 2.5%.

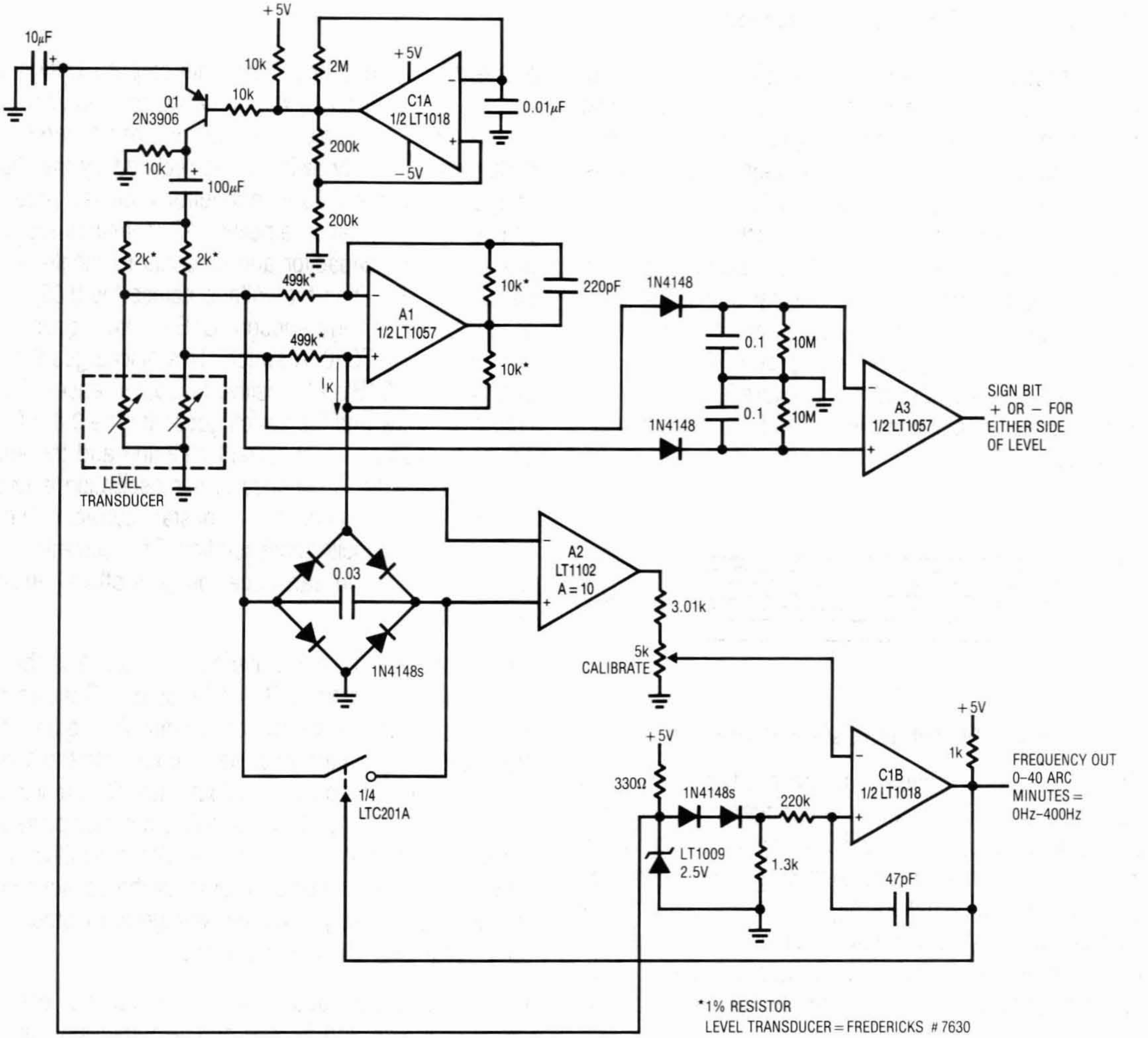

10μF
+5V
10k
2M
+5V
Q1
2N3906
10k
C1A
1/2 LT1018
0.01μF
10k
100μF
200k
−5V
200k
2k*
2k*
499k*
A1
1/2 LT1057
10k*
220pF
1N4148
499k*
0.1
10M
10k*
I_K
0.1
10M
1N4148
A3
1/2 LT1057
SIGN BIT
+ OR − FOR
EITHER SIDE
OF LEVEL
LEVEL
TRANSDUCER
A2
LT1102
A = 10
0.03
3.01k
1N4148s
5k
CALIBRATE
+5V
+5V
1k
C1B
1/2 LT1018
FREQUENCY OUT
0–40 ARC
MINUTES =
0Hz–400Hz
330Ω
1N4148s
220k
1/4
LTC201A
LT1009
2.5V
1.3k
47pF
*1% RESISTOR
LEVEL TRANSDUCER = FREDERICKS #7630

Figure 29B. Level Transducer Digitizer Uses AC Bridge Technique

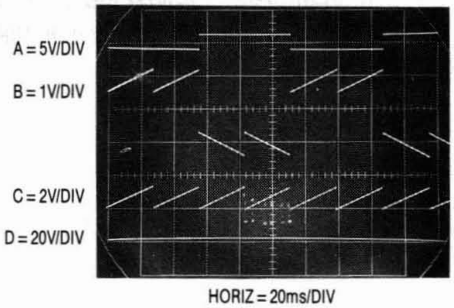
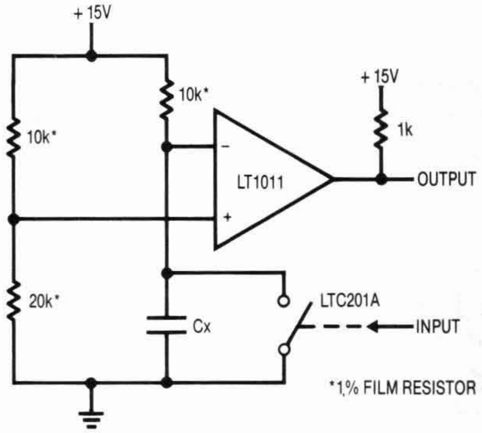


Figure 30. Level Transducer Bridge Circuits Waveforms

Time Domain Bridge

Figure 31 is another AC based bridge, but works in the time domain. This circuit is particularly applicable to capacitance measurement. Operation is straightforward. With S1 closed the comparators output is high. When S1 opens, capacitor Cx charges. When Cx's potential crosses the voltage established by the bridge's left side resistors the comparator trips low. The elapsed time between the switch opening and the comparator going low is proportionate to Cx's value. This circuit is insensitive to supply



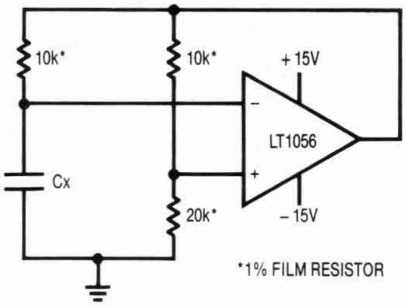
*1% FILM RESISTOR

Figure 31. Time Domain Bridge

and repetition rate variations and can provide good accuracy if time constants are kept much larger than comparator and switch delays. For example, the LT1011's delay is about 200ns and the LTC201A contributes 450ns. To ensure 1% accuracy the bridges right side time constant should not drop below 65μs. Extremely low values of capacitance may be influenced by switch charge injection. In such cases switching should be implemented by alternating the bridge drive between ground and +15.

Bridge Oscillator — Square Wave Output

Only an inattentive outlook could resist folding Figure 31's bridge back upon itself to make an oscillator. Figure 32 does this, forming a bridge oscillator. This circuit will also be recognized as the classic op amp multi-vibrator. In this version the 10k-20k bridge leg provides switching point hysteresis with Cx charged via the remaining 10k resistor. When Cx reaches the switching point the amplifier's output changes state, abruptly reversing the sign of its positive input voltage. Cx's charging direction also reverses, and oscillations continue. At frequencies that are low compared to amplifier delays output frequency is almost entirely dependent on the bridge components. Amplifier input errors tend to ratiometrically cancel, and supply shifts are similarly rejected. The duty cycle is influenced by output saturation and supply asymmetrys.



*1% FILM RESISTOR

Figure 32. "Bridge Oscillator" (Good Old Op Amp Multivibrator with A Fancy Name)

Quartz Stabilized Bridge Oscillator

Figure 33, generically similar to Figure 32, replaces one of the bridge arms with a resonant element. With the crystal removed the circuit is a familiar non-inverting gain of two with a grounded input. Inserting the crystal closes a positive feedback path at the crystal's resonant frequency. The amplifier output (trace A, Figure 34) swings in an attempt to maintain input balance. Excessive circuit gain prevents linear operation, and oscillations commence as the amplifier repeatedly overshoots in it's attempts to null the bridge. The crystal's high Q is evident in the filtered waveform (trace B) at the amplifiers positive input.

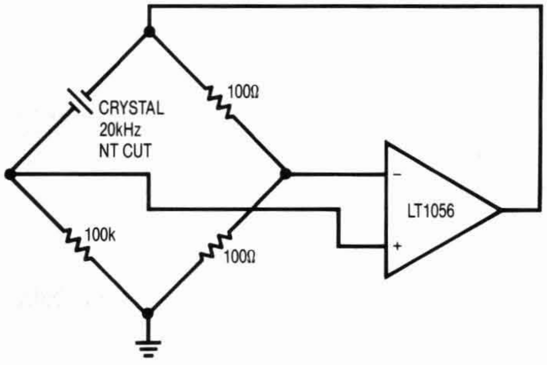


Figure 33. Bridge Based Crystal Oscillator

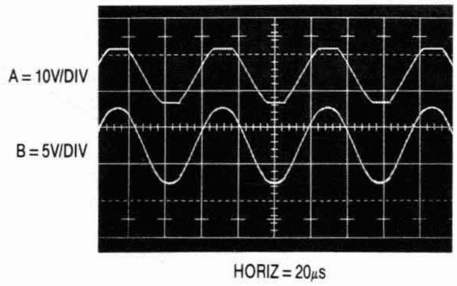


Figure 34. Bridge Based Crystal Oscillator's Waveforms. Excessive Gain Causes Output Saturation Limiting.

Sine Wave Output Quartz Stabilized Bridge Oscillator

Figure 35 takes the previous circuit into the linear region to produce a sine wave output. It does this by continuously controlling the gain to maintain linear operation. This arrangement uses a classic technique first described by Meacham in 1938 (see References).

In any oscillator it is necessary to control the gain as well as the phase shift at the frequency of interest. If gain is too low, oscillation will not occur. Conversely, too much gain produces saturation limiting, as in Figure 33. Here, gain control comes from the positive temperature coefficient of the lamp. When power is applied, the lamp is at a low resistance value, gain is high and oscillation amplitude builds. As amplitude builds, the lamp current increases, heating occurs and its resistance goes up. This causes a reduction in amplifier gain and the circuit finds a stable operating point. The 15pF capacitor suppresses spurious oscillation.

Operating waveforms appear in Figure 36. The amplifiers output (trace A, Figure 36) is a sine wave, with about 1.5% distortion (trace B). The relatively high distortion content is almost entirely due to the common mode swing seen by the amplifier. Op amp common mode rejection suffers at high frequency, producing output distortion. Figure 37 eliminates the common mode swing by using a second amplifier to force the bridge's midpoint to virtual ground.[3] It does this by measuring the midpoint value, comparing it to ground and controlling the formerly grounded end of the bridge to maintain its inputs at zero. Because the bridge drive is complementary the oscillator amplifier now sees no common mode swing, dramatically reducing distortion. Figure 38 shows less than 0.005% distortion (trace B) in the output (trace A) waveform.

Note 3: Sharp eyed readers will recognize this as an AC version of the DC common mode suppression technique introduced back in Figure 6.

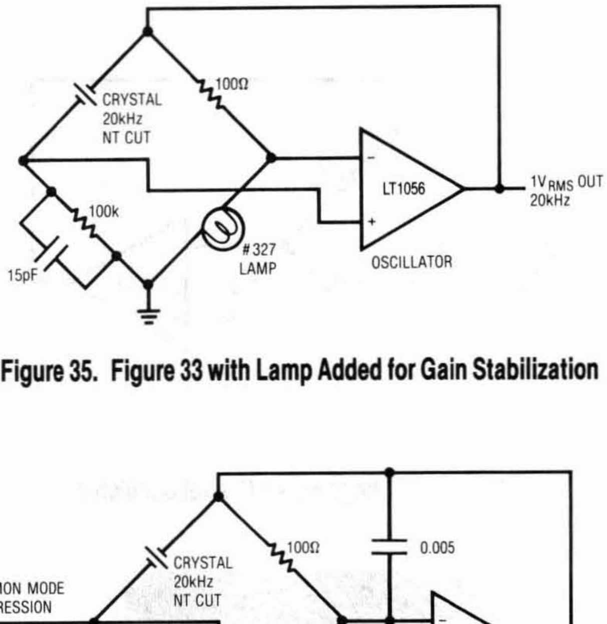


Figure 35. Figure 33 with Lamp Added for Gain Stabilization

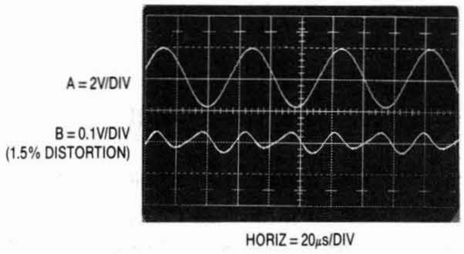


Figure 36. Lamp Based Amplitude Stabilization Produces Sine Wave Output

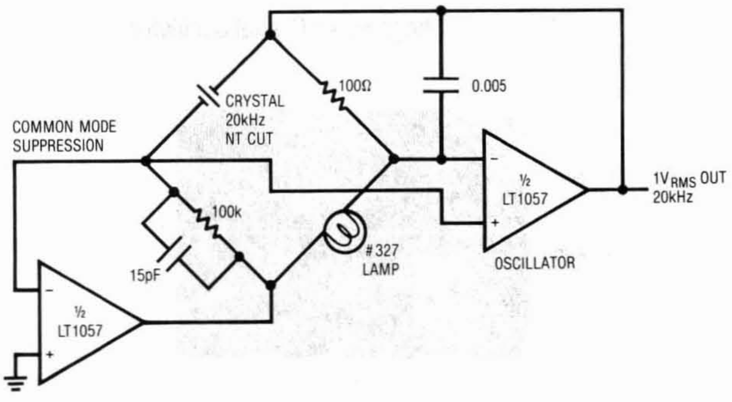


Figure 37. Common Mode Suppression for Quartz Oscillator Lowers Distortion

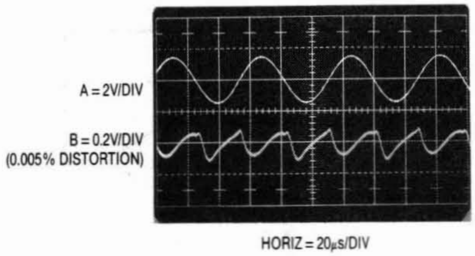


Figure 38. Distortion Measurements for Figure 37. Common Mode Suppression Permits 0.005% Distortion.

Wien Bridge Based Oscillators

Crystals are not the only resonant elements that can be stabilized in a gain controlled bridge. Figure 39 is a Wien bridge (see References) based oscillator. The configuration shown was originally developed for telephony applications. The circuit is a modern adaptation of one described by a Stanford University student, William R. Hewlett,[4] in his 1939 masters thesis (see Appendix C, "The Wien Bridge and Mr. Hewlett").

The Wien network provides phase shift governed by the equation listed, and the lamp regulates amplitude in accordance with Figure 35's description. Figure 40 is a variable frequency version of the basic circuit. Output frequency range spans 20Hz to 20kHz in three decade ranges, with 0.25dB amplitude flatness.

Note 4: History records that Hewlett and his friend David Packard made a number of these type oscillators. Then they built some other kinds of instruments.

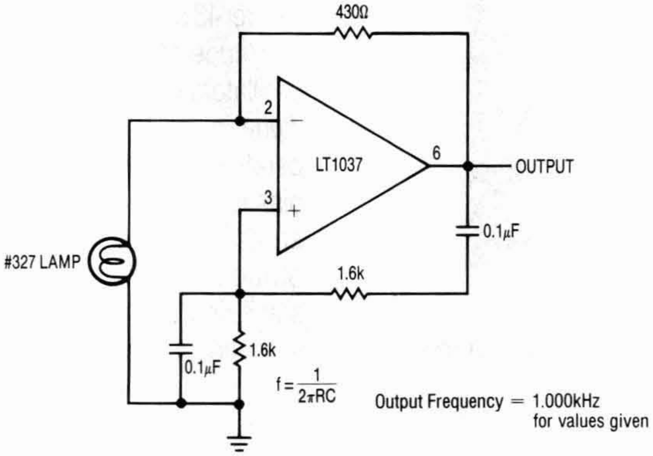

430Ω
2
−
LT1037
6
OUTPUT
3
+
0.1μF
#327 LAMP
1.6k
0.1μF
1.6k
$f = \frac{1}{2\pi RC}$
Output Frequency = 1.000kHz
for values given

Figure 39. Wien Bridge Based Sine Wave Oscillator. Simple, Modern Version of an Old Circuit Has 0.0025% Distortion.

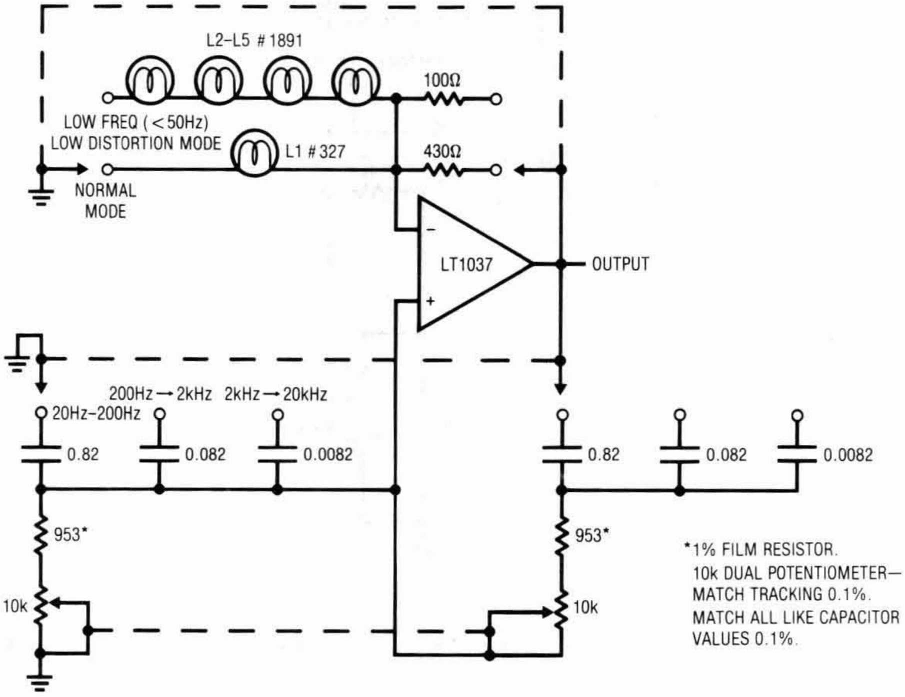

L2–L5 #1891
100Ω
LOW FREQ (<50Hz)
LOW DISTORTION MODE
L1 #327
430Ω
NORMAL
MODE
−
LT1037
+
OUTPUT
200Hz→2kHz
2kHz→20kHz
20Hz–200Hz
0.82
0.082
0.0082
0.82
0.082
0.0082
953*
953*
10k
10k
*1% FILM RESISTOR.
10k DUAL POTENTIOMETER—
MATCH TRACKING 0.1%.
MATCH ALL LIKE CAPACITOR
VALUES 0.1%.

Figure 40. Multi-Range Wien Bridge Based Oscillator. Multiple Lamps Provide Lowered Distortion at Low Frequencies.

The smooth, limiting nature of the lamp's operation, in combination with its simplicity, gives good results. Trace A, Figure 41, shows circuit output at 10kHz. Harmonic distortion, shown in trace B, is below 0.003%. The trace shows that most of the distortion is due to second harmonic content and some crossover disturbance is noticeable. The low resistance values in the Wien network and the $3.8\text{nV}\sqrt{\text{Hz}}$ noise specification of the LT1037 eliminate amplifier noise as an error term.

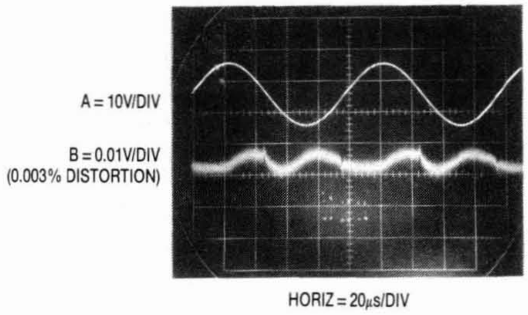

A = 10V/DIV
B = 0.01V/DIV
(0.003% DISTORTION)
HORIZ = 20µs/DIV

Figure 41. Figure 40's Distortion Characteristic at 10kHz

At low frequencies, the thermal time constant of the small normal mode lamp begins to introduce distortion levels above 0.01%. This is due to "hunting" as the oscillator's frequency approaches the lamp thermal time constant. This effect can be eliminated, at the expense of reduced output amplitude and longer amplitude settling time, by switching to the low frequency, low distortion mode. The four large lamps give a longer thermal time constant and distortion is reduced. Figure 42 plots distortion versus frequency for the circuit.

Figure 43's version replaces the lamp with an electronic amplitude stabilization loop. The LT1055 compares the oscillators positive output peaks with a DC reference. The diode in series with the LT1004 reference provides temperature compensation for the rectifier diode. The op amp biases Q1, controlling its channel resistance. This influences loop gain, which is reflected in oscillator output amplitude. Loop closure around the LT1055 occurs, stabilizing oscillator amplitude. The 15µF capacitor stabilizes the loop, with the 22k resistor settling its gain.

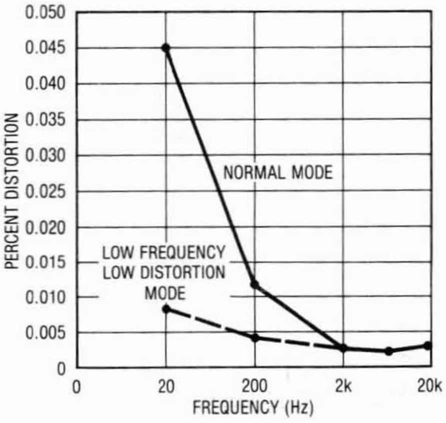


Figure 42. Figure 40's Distortion vs Frequency

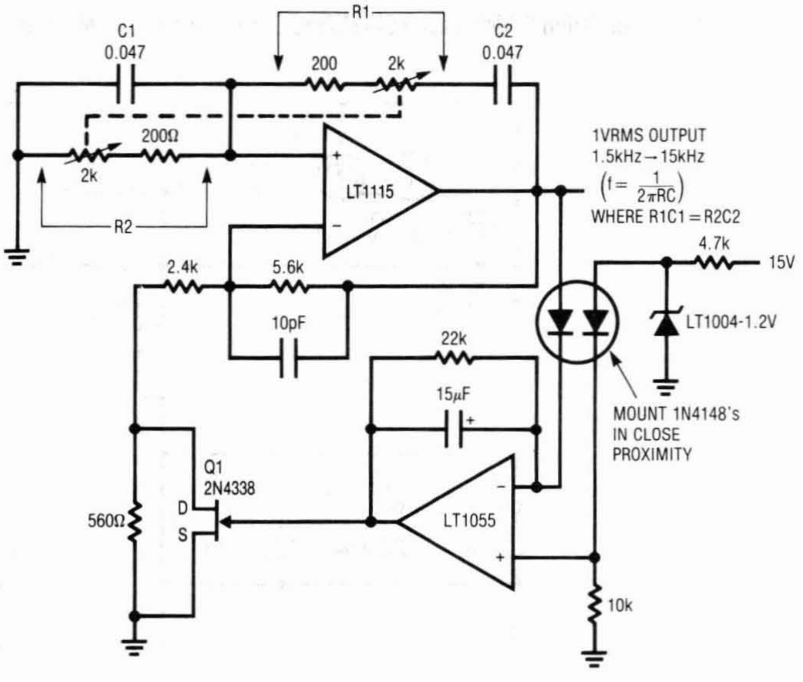

R1
C1
0.047
200
2k
C2
0.047
2000Ω
2k
R2
LT1115
1VRMS OUTPUT
1.5kHz → 15kHz
(f = 1/2πRC)
WHERE R1C1 = R2C2
4.7k
15V
2.4k
5.6k
10pF
22k
LT1004-1.2V
15µF
MOUNT 1N4148's
IN CLOSE
PROXIMITY
Q1
2N4338
D
S
560Ω
LT1055
10k

Figure 43. Replacing the Lamp with an Electronic Equivalent

Distortion performance for this circuit is quite disappointing. Figure 44 shows 0.15% 2f distortion (trace B) in the output (trace A), a huge increase over the lamp based approach.[5] This distortion does not correlate with the rectifier peaking residue present at Q1's gate (trace C). Where is the villain in this scheme?

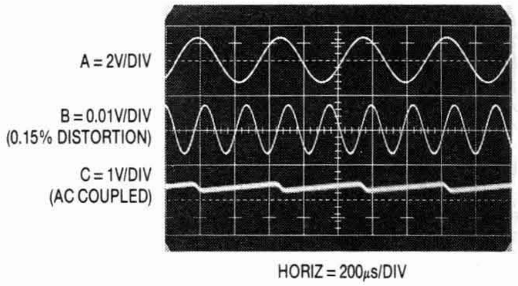


Figure 44. Figure 43 Produces Excessive Distortion Due to Q1's Channel Resistance Modulation

The culprit turns out to be Q1. In a FET, gate voltage theoretically sets channel resistance. In fact, channel voltage also slightly modulates channel resistance. In this circuit Q1's channel sees large swings at the fundamental. This swing combines with the channel voltage-resistance modulation effect, producing distortion.

The cure for this difficulty is local feedback around Q1. Properly scaled, this feedback nicely cancels out the parasitic. Figure 45 shows the circuit re-drawn with the inclusion of Q1's local loop. The 20k trimmer allows adjustment to optimize distortion performance. Figure 46 shows results. Distortion (trace B) drops to 0.0018% and is composed of 2f, some gain loop rectification artifacts and noise. For reference the circuit's output (trace A) and the LT1055 output (trace C) are shown.

Figure 47 eliminates the trim, provides increased voltage and current output, and slightly reduces distortion. Q1 is replaced with an optically driven CdS photocell. This device has no parasitic resistance modulation effects. The LT1055 has been replaced with a ground sensing op amp

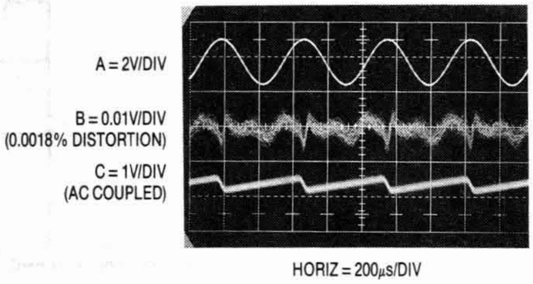


Figure 46. Figure 45's 0.0018% Distortion Characteristic

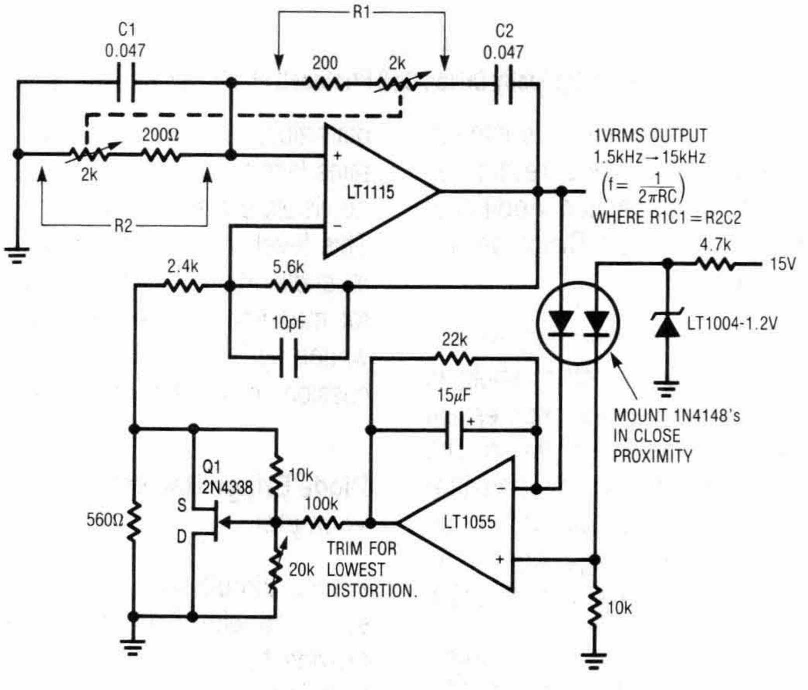
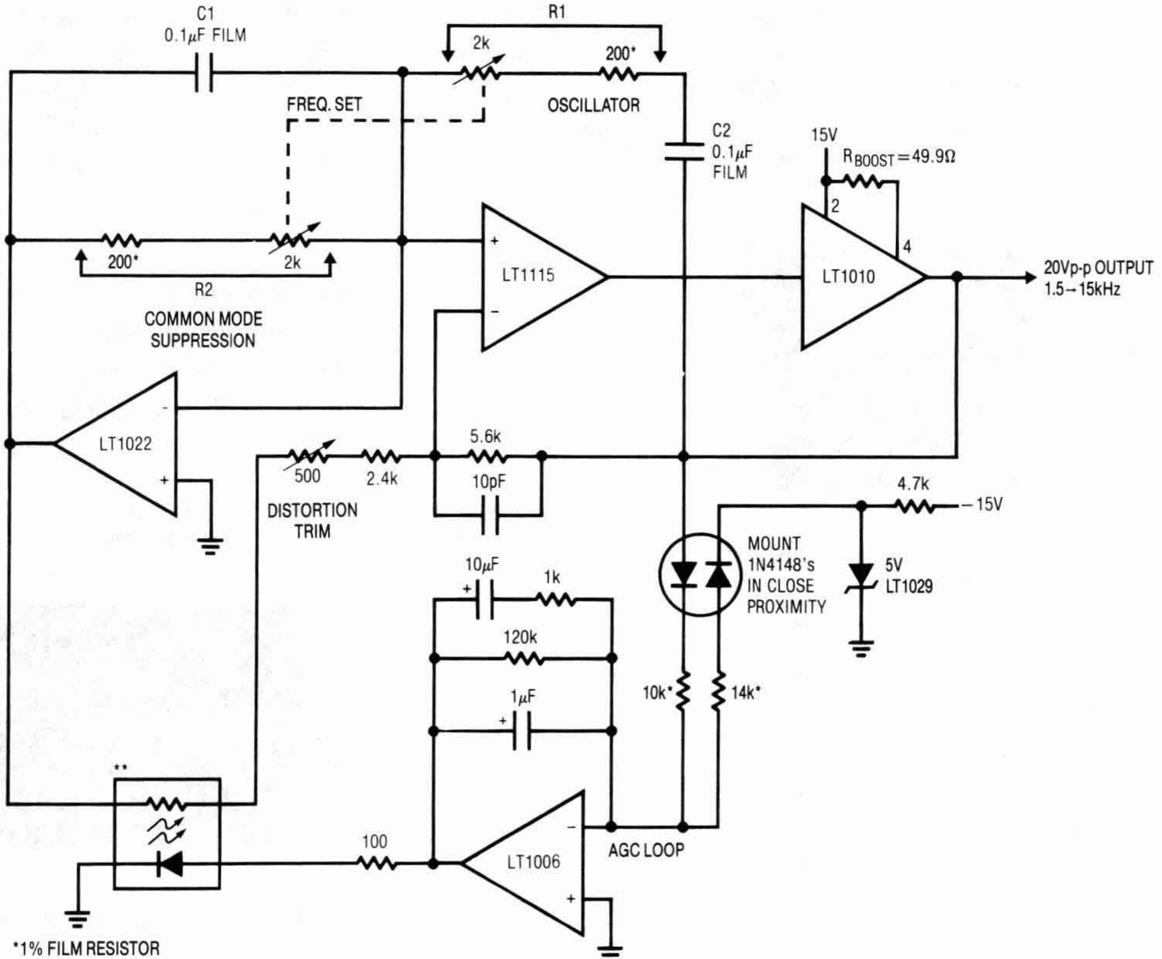

C1
0.047
R1
200
2k
C2
0.047
200Ω
2k
R2
LT1115
1VRMS OUTPUT
1.5kHz → 15kHz
(f = 1/2πRC)
WHERE R1C1 = R2C2
4.7k
15V
2.4k
5.6k
10pF
22k
LT1004-1.2V
15μF
MOUNT 1N4148's
IN CLOSE
PROXIMITY
Q1
2N4338
10k
S
D
560Ω
100k
LT1055
TRIM FOR
LOWEST
DISTORTION.
20k
10k

Figure 45. Local Feedback Around Q1 Cures Channel Resistance Modulation, Reducing Distortion to 0.0018%

Note 5: What else should be expected when trying to replace a single light bulb with a bunch of electronic components? I can hear Figure 39's #327 lamp laughing.


C1
0.1μF FILM
R1
2k
200*
FREQ. SET
OSCILLATOR
C2
0.1μF
FILM
15V
R_{BOOST}=49.9Ω
2
4
200*
2k
R2
COMMON MODE
SUPPRESSION
LT1115
LT1010
20Vp-p OUTPUT
1.5→15kHz
LT1022
500
2.4k
DISTORTION
TRIM
5.6k
10pF
4.7k
–15V
10μF
1k
120k
1μF
MOUNT
1N4148's
IN CLOSE
PROXIMITY
5V
LT1029
10k*
14k*
**
100
LT1006
AGC LOOP

*1% FILM RESISTOR
**VACTEC VTL5C10 OR CLAREX CLM410
LT1022, LT1115, LT1010 = ±15V SUPPLY
LT1006 = +15V SUPPLY

Figure 47. Replacing Q1 with an Optically Driven CdS Photocell Eliminates Resistance Modulation Trim

running in single supply mode. This permits true integrator operation and eliminates any possibility of reverse biasing the (downsized) feedback capacitor. Additional feedback components aid step response.[6] Distortion performance improves slightly to 0.0015%.

The last Wien bridge based circuit borrows Figure 37's common mode suppression technique (which is simply an AC version of Figure 6's DC common mode suppression loop) to reduce distortion to vanishingly small levels. The LT1022 amplifier appears in Figure 48. This amplifier forces the midpoint of the bridge to virtual ground by servo biasing the formerly grounded bridge legs. As in Figure 37, common mode swing is eliminated, reducing distortion. The circuit's output (trace A, Figure 49) contains less than 0.0003% (3ppm) distortion (trace B), with no visible correlation to gain loop ripple residue (trace C). This level of distortion is below the uncertainty floor of most distortion analyzers, requiring specialized equipment for meaningful measurement. (See Appendix D, guest written by Bruce Hofer of Audio Precision, Inc., for a discussion on distortion measurement considerations.)

Diode Bridge Based 2.5MHz Precision Rectifier/AC Voltmeter

A final circuit shows a way to achieve low AC error switching with diode bridge techniques. Diode bridges provide faster, cleaner signal switching than any other technique.

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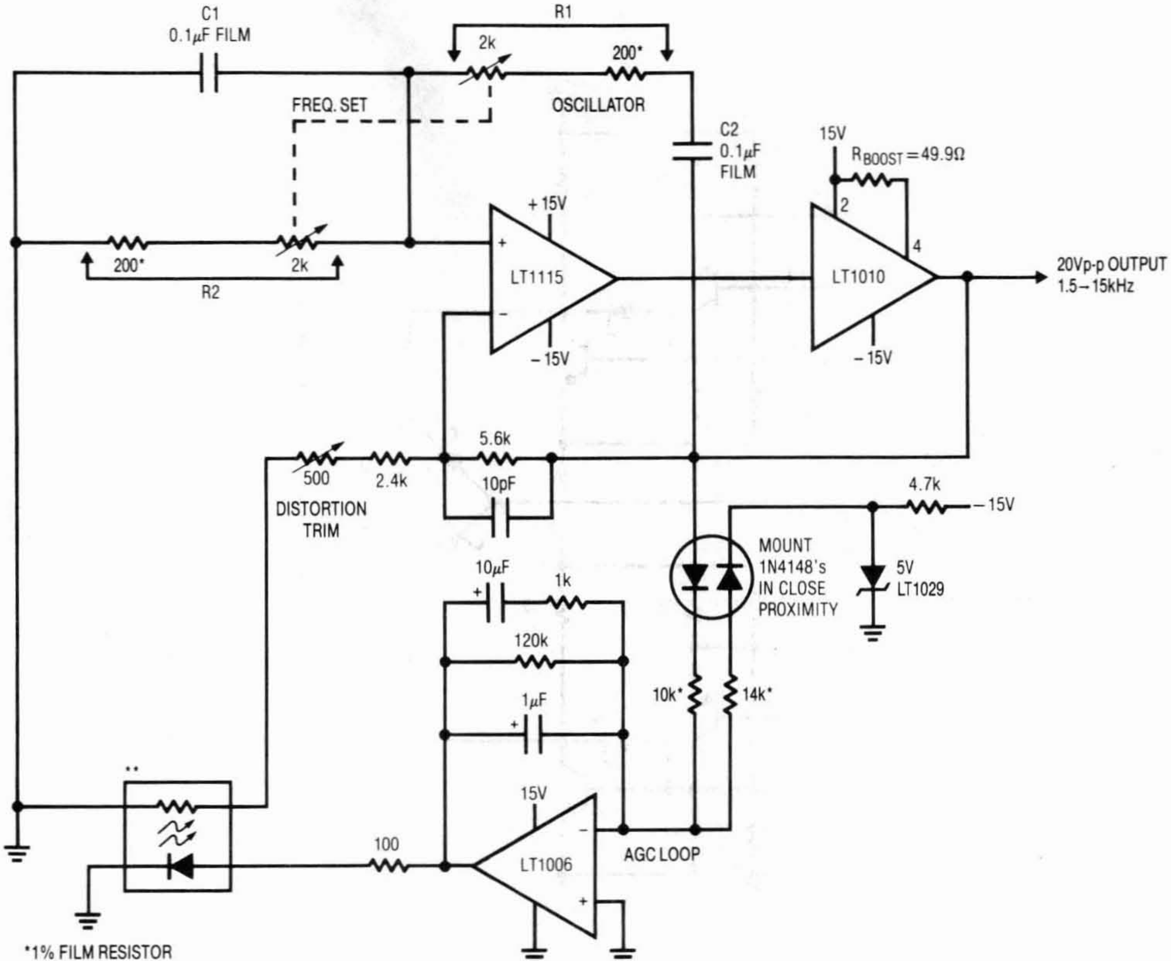
[6] **Note 6:** A much better scheme for a low ripple, fast response gain control loop is nicely detailed in the operating and service manual supplied with the Hewlett-Packard HP339A Distortion Analyzer.


C1
0.1μF FILM
R1
2k
200*
FREQ. SET
OSCILLATOR
C2
0.1μF
FILM
15V
R_BOOST = 49.9Ω
2
4
+15V
+
–
LT1115
–15V
LT1010
–15V
20Vp-p OUTPUT
1.5 – 15kHz
200*
2k
R2
5.6k
500
2.4k
10pF
DISTORTION
TRIM
4.7k
–15V
MOUNT
1N4148's
IN CLOSE
PROXIMITY
5V
LT1029
10μF
1k
120k
1μF
10k*
14k*
**
15V
100
LT1006
AGC LOOP

*1% FILM RESISTOR
**VACTEC VTL5C10 OR CLAREX CLM410
LT1115, LT1010 = ± 15V SUPPLY
LT1006 = + 15V SUPPLY

Figure 48. Adding Common Mode Suppression Lowers Distortion to 0.0003%

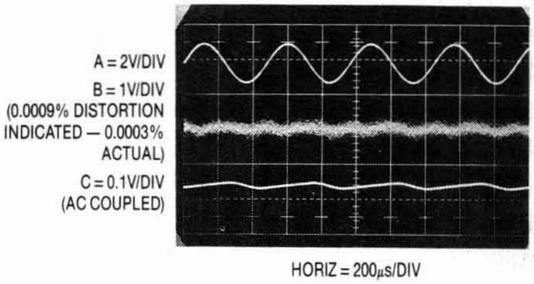


Figure 49. Figure 48's 3ppm Distortion Is Below the Noise Floor of Most Analyzers

Most precision rectifier circuits rely on operational amplifiers to correct for diode drops. Although this scheme works well, bandwidth limitations usually restrict these circuits to operation below 100kHz. Figure 50 shows the LT1016 comparator in an open-loop, synchronous rectifier configuration which has high accuracy out to 2.5MHz. An input 1MHz sine wave (trace A, Figure 51) is zero cross detected by C1. Both of C1's outputs drive identical level shifters with fast (delay = 2ns-3ns), ±5V outputs. These outputs bias a Schottky diode switching bridge (traces B and C are the switched corners of the bridge). The input signal is fed to the left-midsection of the bridge. Because C1 drives the bridge synchronously with the input signal, a half-wave rectified sine appears at the AC output (trace D). The RMS value appears at the DC output. The Schottky bridge gives fast switching without charge pump-through. This is evident in trace E, which is an expanded version of trace D. The waveform is clean with the exception of very small disturbances where bridge switching occurs. To calibrate this circuit, apply a 1MHz-2MHz 1Vp-p sine wave and adjust the delay compensation so bridge

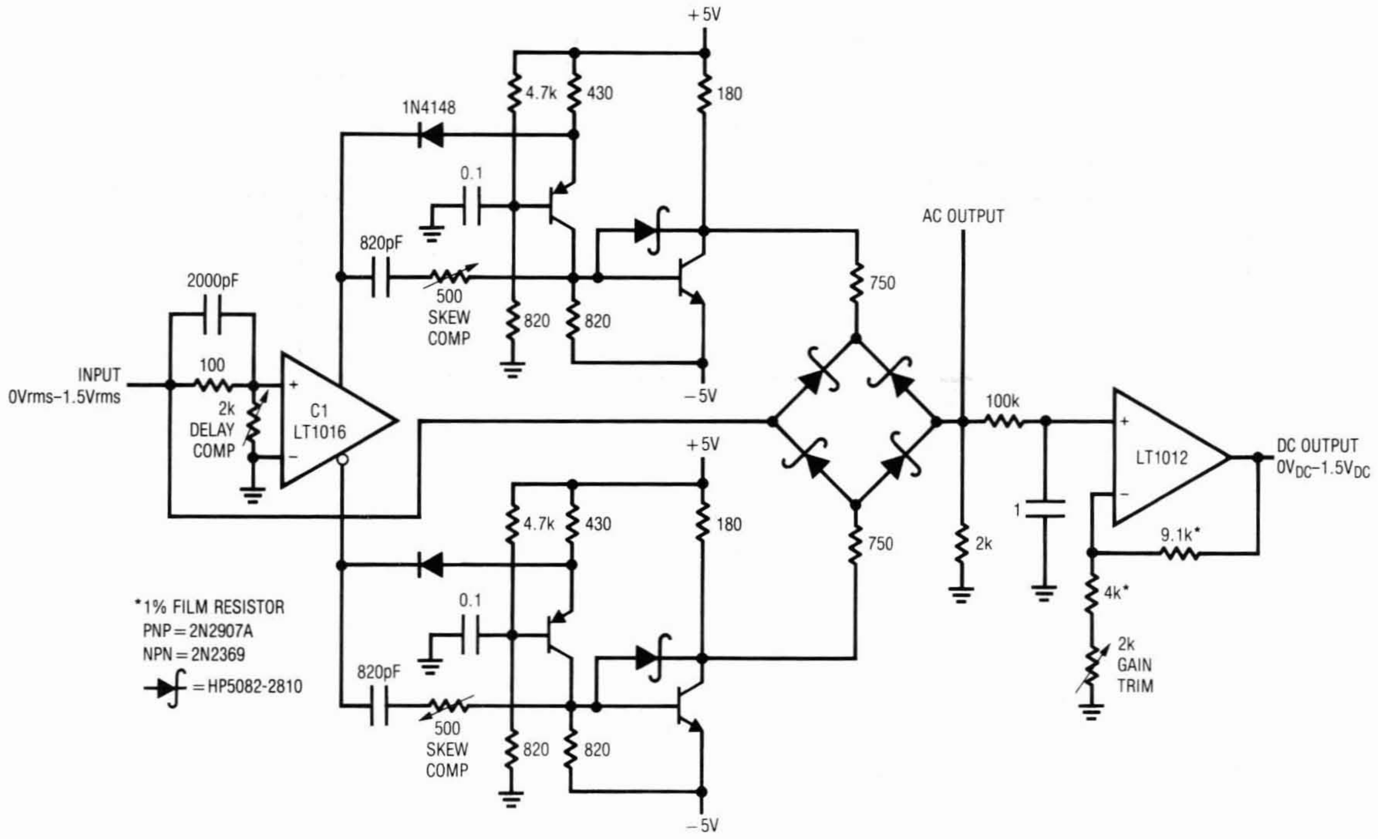
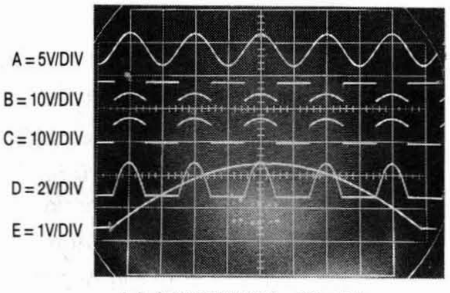

+5V
4.7k
430
180
1N4148
0.1
AC OUTPUT
820pF
2000pF
750
500
SKEW
COMP
820
820
INPUT
0Vrms–1.5Vrms
100
2k
DELAY
COMP
+
–
C1
LT1016
–5V
100k
+5V
LT1012
DC OUTPUT
$0V_{DC}$–$1.5V_{DC}$
4.7k
430
180
750
2k
1
9.1k*
*1% FILM RESISTOR
PNP = 2N2907A
NPN = 2N2369
= HP5082-2810
0.1
4k*
2k
GAIN
TRIM
820pF
500
SKEW
COMP
820
820
–5V

Figure 50. Fast, Bridge Switched Synchronous Rectifier-Based AC-DC Converter



A, B, C, D HORIZONTAL = 500ns/DIV
E HORIZONTAL = 50ns/DIV (UNCALIBRATED)

Figure 51. Fast AC-DC Converter Operating at 1MHz. Clean Switching Is Due to Bridge Symmetry and Compensations for Delay and Switching Skew.

switching occurs when the sine crosses zero. This adjustment corrects for the small delays through the LT1016 and the level shifters. Next, adjust the skew compensation potentiometers for minimum aberrations in the AC output signal. These trims slightly shift the phase of the rising output edge of their respective level shifter. This allows skew in the complementary bridge drive signals to be kept within 1ns-2ns, minimizing output disturbances when switching occurs. A 100mV sine input will produce a clean output with a DC output accuracy of better than 0.25%.

Note: *This application note was derived from a manuscript originally prepared for publication in EDN magazine.*

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APPENDIX A

STRAIN GAUGE BRIDGES

In 1856 Lord Kelvin discovered that applying strain to a wire shifted its resistance. This effect is repeatable, and is the basis for electrical output strain measurement. Early devices were simply wires suspended between two insulated points (Figure A1). The force to be measured mechanically biased the wire, changing its resistance. Modern devices utilize foil based designs. The conductive material is deposited on an insulated carrier (Figure A2). Physically they take many forms, allowing for a variety of applications. The gages[1] are usually configured in a bridge and mounted on a beam (Figure A3), forming a transducer.

A useful transducer must be trimmed for zero and gain, and compensated for temperature sensitivity. Figure A4 shows a typical arrangement. Zero is set with a parallel trim, with similar treatment used to set gain. The gain trims include modulus gages to compensate beam material temperature sensitivity. Arranging these trims and completing the mechanical integration involves a fair amount of artistry, and is usually best left to specialists.[2]

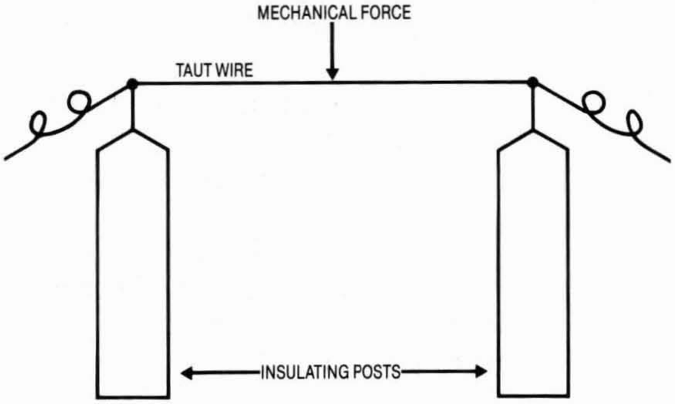

Figure A1. A Very Basic Strain Gage

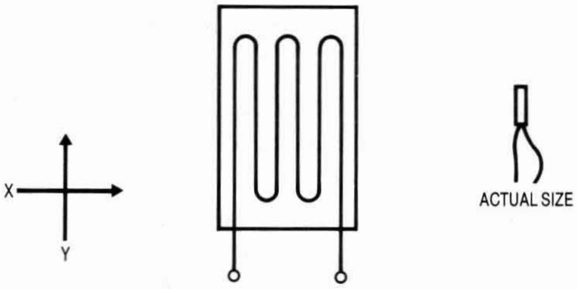

Figure A2. A Conceptual Strain Gage. Maximum Device Sensitivity is with Y-Axis Flexing Into the Page. Practical Devices Utilize Denser Patterns with Optimized Distribution of Conductive Material.

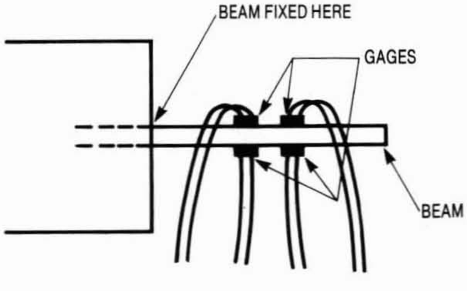

Figure A3. A Conceptual Strain Gage Transducer. Bending Force on the Beam Causes Resistance Shifts.

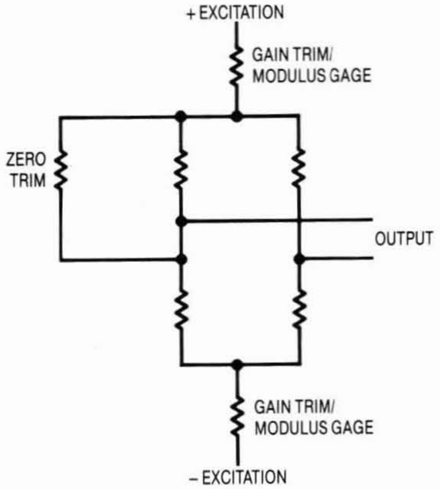

Figure A4. Simplified Strain Gage Transducer Schematic

Note 1: The correct spelling is gauge, but prolonged grammatical assaults have assassinated the "u." Hence, "gage" assumes a claim to legitimacy.

Note 2: Those finding their sense of engineering prowess unalterably offended are referred to "SR-4 Strain Gage Handbook," available from BLH Electronics, Canton, Massachusetts. Have fun.

Semiconductor based strain gage transducers utilize resistive shift in semiconducting materials. These devices, built in monolithic IC form, are considerably less expensive than manually assembled foil based strain gage transducers. They have over ten times the sensitivity of foil based devices, but are more sensitive to temperature and other effects. As such, they are best suited to somewhat less demanding applications than foil based gages. Their monolithic construction and small size offer price and convenience advantages in many applications. Electrical form is similar to foil based designs (e.g., a bridge configuration), although impedance levels are about ten times higher. The following guest written section details their characteristics.

SEMICONDUCTOR BASED STRAIN GAGES

Daniel A. Artusi
Randy K. Frank
Motorola Semiconductor Products Sector
Discrete and Special Technologies Group

Strain gage technology, while based on a phenomena which dates back to the nineteenth century, has been of major importance in the areas of stress analysis, structural testing and transducer fabrication for more than 40 years.

First reports on semiconductor piezoresistive technology dates back to the observation by C.S. Smith[3] in the early 1950's of large piezoresistive coefficients in Silicon and Germanium.

There are several advantages to implementing strain gages using semiconductor technology. The immediate one is the very high gage factors of approximately two orders of magnitude higher than metallic gages. These higher gage factors allow improved signal to noise ratios for the measurement of small dynamic stresses and simplifies the signal conditioning circuitry.

Another advantage is the precise control of the piezoresistive coefficients including magnitude, sign, and the possibility of transverse and shear responses. Additional advantages are low cost, small size, and compatibility with semiconductor processing technology which allows for integration of additional circuit elements (i.e. operational amplifiers) on the same chip. The first phase of integration for silicon pressure sensors occurred when the strain gage and the diaphragm were combined into one monolithic structure. This was accomplished using the piezoresistive effect in semiconductors. A strain gage can be diffused or ion-implanted into a thin silicon diaphragm which has been chemically etched into a silicon substrate.

Piezoresistivity

In order to understand the implementation in silicon of strain gages, it is necessary to review the piezoresistive effect in silicon.

The analytic description of the piezoresistive effect in cubic silicon can be reduced to two equations which demonstrate the first order effects.

$$\Delta E_1 = P_O\, I_1(\pi_{11}X_1 + \pi_{12}X_2) \qquad [1]$$

$$\Delta E_2 = P_O\, I_2\pi_{44}X_6 \qquad [2]$$

Where ΔE_1 and ΔE_2 are electric field flux density, P_O is the unstressed bulk resistivity of silicon, I's are the excitation current density, π's are piezoresistive coefficients and X's are stress tensors due to the applied force.

The effect described by equation [1] is that utilized in a pressure transducer of the Wheatstone bridge type. Regardless of whether the designer chooses N-type or P-type layers for the diffused sensing element, the piezoresistive coefficients π_{11} and π_{12} of equation [1] will be oppose in sign.

This implies that through careful placement, and orientation with respect to the crystallographic axis, as well as a sufficiently large aspect ratio for the resistors themselves, it is possible to fabricate resistors on the same diaphragm which both increase and decrease respectively from their nominal values with the application of stress.

The effect described by equation [2] is typically neglected as a parasitic in the design of a Wheatstone bridge device. A closer look at its form, however, reveals that the incremental electrical field flux density, ΔE_2, due to the applied stress, X_6, is monotonically increasing for increasing X_6.

Note 3: Smith C.S., "Piezoresistance Effect in Germanium and Silicon," Physical Review, Volume 94, November 1, 1954 Pages 42-49.

In fact, equation [2] predicts an extremely linear output since it depends on only one piezoresistive coefficient and one applied stress. Futhermore, the incremental electric field can be measured by a single stress sensitive element. This forms the theoretical basis for the design of the transverse voltage or shear stress piezoresistive strain gage.

Shear Stress Strain Gage

Figure A5 shows the construction of a device which optimizes the piezoresistive effect of equation [2].[4] The diaphragm is anisotropically etched from a silicon substrate. The piezoresistive element is a single, four terminal strain gage that is located at the midpoint of the edge of the square diaphragm at an angle of 45 degrees as shown in Figure A5. The orientation of 45 degrees and location at the center of the edge of the diaphragm maximizes the sensitivity to shear stress, X_6, and the shear stress being sensed by the transducer by maximizing the piezoresistive coefficient, π_{44}.

Excitation current is passed longitudinally through the resistor (pins 1 and 3) and the pressure that stresses the diaphragm is applied at a right angle to the current flow. The stress establishes a transverse electric field in the resistor that is sensed as an output voltage at pins 2 and 4, which are the taps located at the midpoint of the resistor. The single element shear stress strain gage can be viewed as the mechanical analog of a Hall effect device. Figure A6 shows a cross section of a pressure transducer implemented in silicon and using the technique described. A differential pressure sensor chip is accomplished by opening the back side of the wafer.

Temperature Compensation and Calibration

The transverse voltage shear stress piezoresistive pressure transducer has been shown to present certain advantages over the Wheatstone bridge configuration. Specifically, improved linearity, and a more consistent reproducible offset (since it is defined by a single photolithographic step), as well as the added advantage of integrating stresses over a smaller percentage of the flexural element.

Very predictably, the transducer exhibits a negative temperature coefficient of span with a nominal value of 0.19%/°C, as well as a temperature coefficient of offset that can be in the range of $\pm 15\mu V/°C$ or slightly larger before compensation. TC of span is due to the decrease of the piezoresistive coefficients with temperature due to increased thermal scattering in the lattice structure.

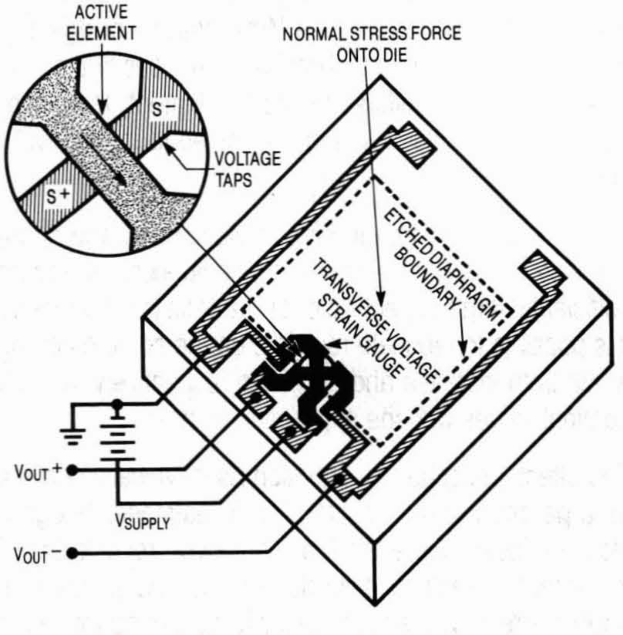
ACTIVE ELEMENT
NORMAL STRESS FORCE ONTO DIE
S−
S+
VOLTAGE TAPS
ETCHED DIAPHRAGM BOUNDARY
TRANSVERSE VOLTAGE STRAIN GAUGE
$V_{OUT}+$
V_{SUPPLY}
$V_{OUT}-$

Figure A5. Basic Sensor Element — Top View

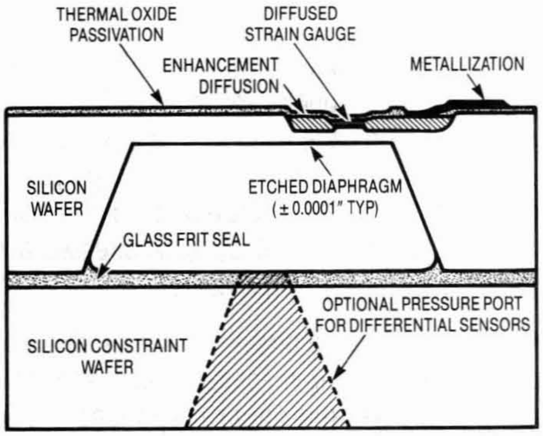
THERMAL OXIDE PASSIVATION
DIFFUSED STRAIN GAUGE
ENHANCEMENT DIFFUSION
METALLIZATION
SILICON WAFER
ETCHED DIAPHRAGM (± 0.0001″ TYP)
GLASS FRIT SEAL
OPTIONAL PRESSURE PORT FOR DIFFERENTIAL SENSORS
SILICON CONSTRAINT WAFER

Figure A6. Cross Section of Pressure Transducer

Note 4: J.E. Gragg, U.S. Patent 4,317,126

First let's consider the relationship of output voltage, ΔV_O, with excitation voltage, V_{EX}, as predicted by equation [2].

$$\Delta V_O = w/l\ (\pi_{44} X_6)\ V_{EX} \qquad [3]$$

It is apparent that the output voltage varies directly with excitation, by a factor $w/l(\pi_{44}X_6)$, or conversely that the output is ratiometric to the excitation, V_{EX}.

A typical output characteristic for an uncompensated transducer with a constant V_{EX} applied is shown in Figure A7. Hence, it is apparent that by increasing the supply voltage at the same rate that the full scale span is decreasing, the undesired temperature dependence of span may be eliminated. This is accomplished by means of a very low TCR resistor placed in series with the transducer excitation legs which, by design, have a TCR of 0.24%/°C (Figure A8). If the value of the zero-TCR span resistor is appropriately chosen, it will decrease the "net" TCR of the combination to the ideal +0.19%/°C required to exactly compensate the negative TC of SPAN. This technique is known as "self-compensation," and can be utilized in the described manner or with a constant current excitaion and a parallel TC span compensation resistor.

The passive circuit utilized to achieve calibration and temperature compensation is shown in Figure A8. Since the single element design uses only one resistor for both the input and the output, a self-compensation scheme can be employed. This technique utilizes the temperature coefficient of the input resistance (TCR) to generate a temperature dependent voltage. The TCR of the strain gage has been specifically designed to be greater in absolute value than the temperature coefficient of the span, so placing additional passive resistive elements in series with the strain gage modifies the effective TCR and allows temperature compensation based on the input resistance value at room temperature. A constant voltage source is all that is necessary external to the device to ensure accurate operation over a wide temperature range.

The self-compensation technique eliminates the requirement for thermistors which are used in most externally compensated Wheatstone bridge pressure sensors. In addition to the cost and nonlinearity characteristics of thermistors, their negative temperature coefficient precludes their integration on silicon. Thin film resistors, on the other hand, are easily deposited on the strain gage substrate using techniques similar to those required for the metallization of wire bond pads used to make connection to external leads. The laser trimming technique is similar to that used in the manufacturing of high accuracy, monolithic, 16-bit analog-to-digital and digital-to-analog data converters, except that in the case of a pressure transducer, the silicon diaphragm is exercised over the pressure range during the trimming procedure.

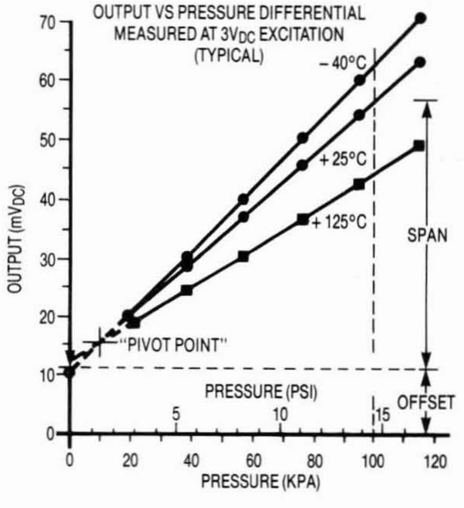

Figure A7. Output Span for Uncompensated Transducer

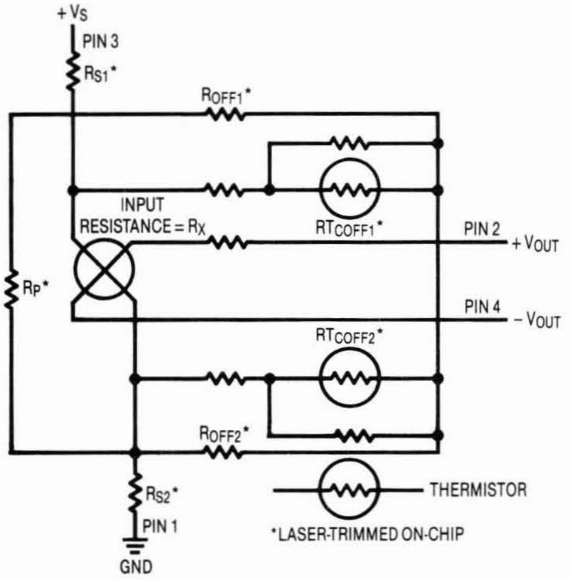

Figure A8. On-Chip Temperature Compensation and Calibration

Four separate functions are accomplished by the laser trimming operation:

1) Zero calibration
2) Zero temperature compensation
3) Full scale span temperature compensation
4) Full scale span calibration

The sequence in which the trimming operation is performed is important to avoid interaction of components and the addition of several iterations to the trimming process. The main factor that allows high volume manufacturing techniques, however, is the ability to achieve temperature compensation in the single element sensor without the necessity to change the temperature during the trim operation. Measurements of the sensor parameters are made prior to the laser trim operation. Computer calculations determine which resistors must be trimmed and the amount of trimming required. Resistor R_{OFF1} and R_{OFF2} act as part of a voltage divider used to calibrate the offset. The output voltage is set to zero with zero pressure applied by trimming either offset resistor R_{OFF1} or R_{OFF2}.

To temperature compensate the offset, thermistors RTC_{OFF1} and RTC_{OFF2}, a series of diffused silicon resistors with positive temperature coefficient and different values, are added as required to the circuit by cutting aluminum shorting links.

Full scale span temperature compensation is accomplished by utilizing self temperature compensation — the addition of a single, series resistor to the input circuit when a constant voltage supply is used. The resistor is adjusted to compensate for changes in span with temperature by adjusting the magnitude of the excitation voltage applied to the active element. In order to minimize common mode errors, the "resistor" is actually split between the supply and ground side of the input so that RS1=RS2. The span is adjusted to meet the specification by trimming resistor R_p, which is in parallel with the input resistance of the active element. The parallel resistor actually interacts with the series self compensation network to provide a series-parallel temperature compensation which enhances the performance over the temperature range.

Performance of Compensated Sensors

The specification for key parameters of a 30PSI on-chip temperature compensated pressure sensor is shown in Figure A9. The excellent linearity is a result of the small active area of the single element strain gage — essentially a point condition. The temperature compensation which is achieved over 0°C to 85°C can be compared to commonly available alternatives.

PARAMETER	MIN	TYP	MAX
Pressure Range (in kPA)	-	-	100
Full Scale Span (in mV)	38.5	40	41.5
Zero Pressure Offset (in mV)	-	+0.05	+1.0
Sensitivity (mV/PSI)	-	1.38	-
Linearity (% FS)	-	+0.1	+0.25
TEMPERATURE EFFECT FOR 0°C TO 85°C			
Full Scale Span (% FS)	-	+0.5	+1.0
Offset (in mV)	-	+0.5	+1.0

Figure A9. Specifications for a Typical Pressure Transducer

APPENDIX B

BRIDGE READOUT — THEN AND NOW

The contemporary monolithic components used to read bridge signals are the beneficiaries of almost 150 years of dedicated work in bridge readout mechanisms. Some early schemes made fiendishly ingenious use of available technology to achieve remarkable performance. Figure B1 shows a light beam galvanometer. This device easily resolved currents in the nanoampere range. The unknown current passed through a coil, producing a magnetic field. The coil is mounted within a static magnetic field. The two field's interactions mechanically biased a small mirror, which was centrally mounted on a tautly suspended wire. The mirror may be thought of as the elastically constrained shaft of a DC motor. The amplitude and sign of the coil current produced corresponding torque — like mirror movements. A collimated light source was bounced off the mirror, and its reflection collected on a surface equipped with calibrated markings. The instruments high inherent sensitivity, combined with the gain in the optical angle, provided excellent results.

The tangent galvanometer (Figure B2) achieved similar nanoampere resolution. The actual meter movement was a compass, centrally mounted within a circular coil. Coil current is measured by noting compass deflection from the earths magnetic north. Current flow is proportional to the tangent of the measured deflection angle.

These and similar devices were referred to as "null detectors." This nomenclature was well chosen, and reflected the fact that bridges were almost always read at null. This was so because the only technology available to accurately digitize electrical measurements was passive. "Bridge balances," including variable resistors, resistance decade boxes and Kelvin-Varley dividers, were cornerstones of absolute measurements. No source of stable, calibrated gain was available; although the null detectors provided high sensitivity. As such, bridge measurement depended on highly accurate balancing technology and sensitive null detectors.

Lee DeForest's triode (1908) began the era of electronic gain. Harold S. Black attempted to patent negative feedback in 1928, but the U.S. Patent Office, in their governmental wisdom, treated him as a crackpot. Black published in the 1930's, and the notion of feedback stabilized gain was immediately utilized by more enlightened

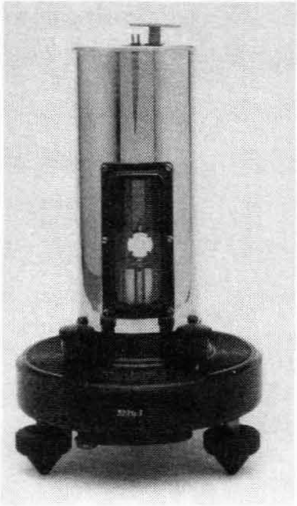

Figure B1. The Light Beam Galvanometer Is Essentially A Sensitive Meter Movement. It Takes Gain in the Optical Angle of A Mirror Reflected, Collimated Light Source (Courtesy The J.M. Williams Collection).

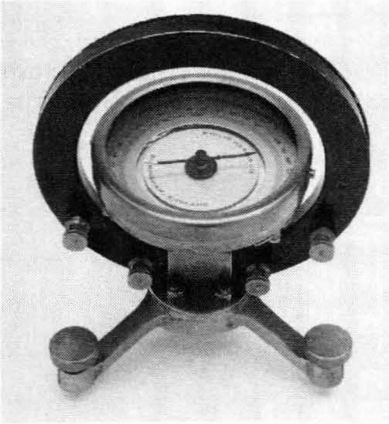

Figure B2. A Tangent Galvanometer Measures Small Currents by Indicating the Interaction Between Applied Current and the Earth's Magnetic Field. Absolute Current Value Is Proportional to the Tangent of the Compass Deflection Angle (Courtesy The J.M. Williams Collection).

types. The technology of the day did not permit development of feedback based amplifiers which could challenge conventional bridge techniques. While Hewlett could use feedback to build a dandy sinewave oscillator, it simply was not good enough to replace Kelvin-Varley dividers and null detectors. Doing so required amplifiers with very high open loop gains and low zero drift. The second requirement was notably difficult and elusive.

E.A. Goldberg invented the chopper stabilized amplifier in 1948, finally making stable zero performance practical. Electronic analog computers quickly followed, and historic George A. Philbrick Researches produced the first commercially available general purpose op amps in the 1950's.

Null detectors were the first bridge components to feel the impact of all this. A number of notable chopper stabilized bridge null detectors were produced during the 1950's and 1960's. All of these were essentially chopper based operational amplifiers configured as complete instruments. Notable among these was the Julie Research Laboratories sub-microvolt sensitivity ND-103, which featured a 93Hz mechanical chopper (to avoid any interaction with 60Hz noise components). The Hewlett-Packard HP-425 had similar sensitivity, and used a small synchronous clock motor, photocells and incandescent lamps[1] in an elegantly simple photo-chopping scheme. Latter versions of this instrument (the HP-419A) were completely solid-state, although retaining a neon lamp-photocell chopping arrangement. Battery operation permitted floating the instrument across the bridge.

Concurrent to all this was the development of rackmounting based devices called "instrumentation amplifiers." These devices, designed to be applied at the system level, featured settable gain and bandwidth, differential inputs, and good zero point stability. Some were chopper stabilized while others utilized transistorized differential connections. Sold by a number of concerns, they were quite popular for transducer signal conditioning. These devices were the forerunners of modern IC instrumentation amplifiers. Their ability to supply low errors at zero and stable gain made accurate off-null bridge measurement possible.

The development of analog-digital converters during the 1960's[2] provided the last ingredient necessary for practical, digitized output, off-null bridge measurement. It had required over 100 years of technological progress to replace the null detectors and bridge balances. This is something to think about when soldering in IC instrumentation amps and A-D converters. What Lord Kelvin would have given for a single mini-DIP!

Note 1: The Hewlett-Packard Company and light bulbs have had a long and successful association.

Note 2: The first fully electronic analog-digital converter was developed by D.H. Wilkinson in 1949 (see References). The first analog-digital converters available as standard product were probably those produced by Pastoriza Electronics in the late 1960's.

APPENDIX C

THE WIEN BRIDGE AND MR. HEWLETT

The Wien bridge is easily the most popular basis for constructing sinewave oscillators. Circuits constructed around the Wien network offer wide dynamic range, ease of tuning, amplitude stability, low distortion and simplicity. Wien described his network (Figure C1) in 1891. Unfortunately, he had no source of electronic gain available, and couldn't have made it oscillate even if he wanted to. Wien developed the network for AC bridge measurement, and went off and used it for that.

Forty-eight years later William R. Hewlett combined Wiens network with controlled electronic gain in his masters thesis. The results were the now familiar "Wien bridge oscillator" architecture and the Hewlett-Packard Company. Hewlett's circuit (Figure C2) utilized the relatively new tools of feedback theory (see References) to support stable oscillation. Two loops were required. A positive feedback loop from the amplifier's output (6F6 plate) back to its positive input (6J7 first grid) via the Wien bridge provided oscillation. Oscillation amplitude was stabilized by a second, negative, feedback loop. This loop was closed from the output (again, the 6F6 plate) back to the amplifiers negative input (the 6J7 cathode). The now famous lamp supplied a slight positive temperature coefficient to maintain gain at the proper value. For reference in interpreting the vacuum tube[1] configuration, a modern version (text Figure 39) of Hewlett's circuit appears as an insert.

Contemporary oscillators usually replace the lamps action with electronic equivalents to control loop settling time (see text).

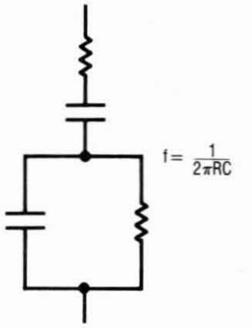

Figure C1. Wiens Network

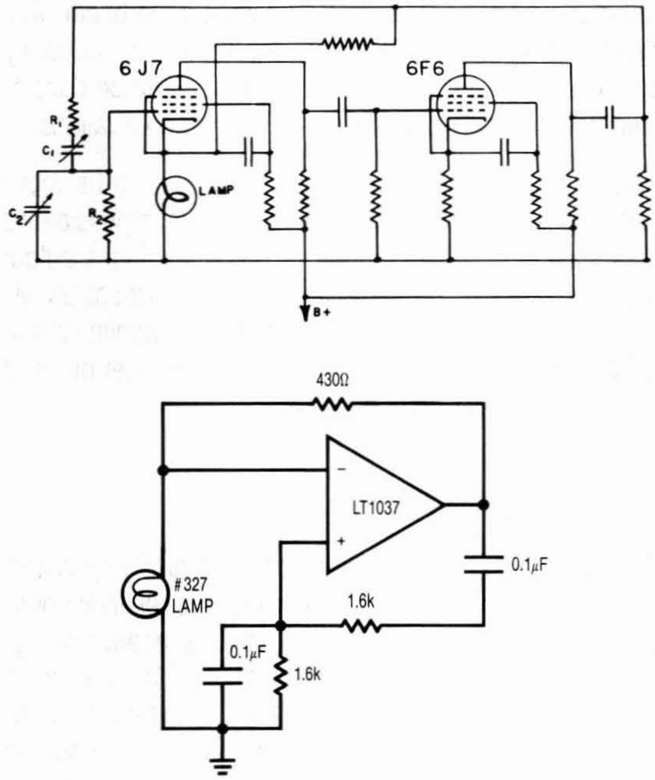

Figure C2. A Copy of Hewletts Thesis "Figure 3" Showing His Original Circuit. Modern Version Shown for Reference (Hewlett's Figure Courtesy Stanford University Archives).

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[1] **Note 1:** For those tender in years, "vacuum tubes" are thermionically activated FET's, descended from Lee DeForest.

APPENDIX D

UNDERSTANDING DISTORTION MEASUREMENTS

Bruce E. Hofer
Audio Precision, Inc.

Introduction

Analog signal distortion is unavoidable in the real world. It can be defined as any effect or process that causes the signal to deviate from ideal. Because "distortion" means significantly different things to different people let us distinguish between two general categories based upon frequency domain effect.

A *linear* distortion changes the amplitude and phase relationship between the existing spectral components of a signal without adding new ones. Frequency and phase response errors are the most common examples. Both can cause significant alteration of the time domain waveform.

A *nonlinear* distortion adds frequency components to the signal that were never there, nor should be to begin with. Nonlinear distortion alters both the time and frequency domain representations of a signal. Noise can be considered a form of nonlinear distortion in some applications.

Nonlinear distortion is generally considered to be more serious than linear distortion because it is impossible to determine if a specific frequency component in the output signal was present in the input. This brief discussion will focus on the measurement and meaning of nonlinear distortion only.The word "distortion" shall hereinafter be used accordingly.

Measures of Distortion

One of the best and oldest methods of quantifying distortion is to excite a circuit or system with a relatively pure sinewave and analyze the output for the presence of signal components at frequencies other than the input sinewave. The sinewave is an ideal test signal for measuring nonlinear distortion because it is virtually immune to linear forms of distortions. With the exception of a perfectly tuned notch filter, the output of any linear distortion process will still be a sinewave!

"N-th" harmonic distortion is defined as the amplitude of any output signal at exactly N times the sinewave fundamental frequency. If the input sinewave is 400Hz any second harmonic distortion will show up at 800Hz, third harmonic at 1200Hz, etc. Spectrum analyzers, wave analyzers, and FFT analyzers are the typical instruments used to measure harmonic distortion. These instruments function by acting as highly selective voltmeters measuring the signal amplitude over a very narrow bandwidth centered at a specific frequency.

"THD" or Total Harmonic Distortion is defined as the RMS summation of the amplitudes of *all* possible harmonics, although it is often simplified to include only the second through the fifth (or somewhat higher) harmonics. The assumption that higher order harmonic content is insignificant in the computation of THD can be quite invalid. The sinewave distortion of many function generators is usually dominated by high order harmonic products with only relatively small amounts of products below the fifth harmonic. The crossover distortion characteristic of class AB and B amplifiers can often exhibit significantly high harmonic content above the fifth order.

A far better definition of THD is to include *all* harmonics up to some prescribed frequency limit. Usually the specific application will suggest a relevant upper harmonic frequency limit. In audio circuits a justifiable upper frequency limit might be 20kHz–25kHz because few people can perceive signals above that range. In practice it has proven desirable to use a somewhat higher limit (typically 80kHz) because nonlinear distortion products above 20kHz can provoke intermodulation problems in subsequent audio stages. In the world of FM and TV broadcast measurements it is common practice to use a 30kHz bandwidth limit even though the signals are inherently limited to 15kHz.

"THD+N" or Total Harmonic Distortion plus Noise is defined as the RMS summation of *all signal components*, excluding the fundamental, over some prescribed bandwidth. Distortion analyzers perform this measurement by removing the fundamental sinewave with a notch filter and measuring the leftover signal. Unfortunately some popular analyzers have excessive measurement bandwidth (>1MHz) with no provision for limiting. For the vast majority of applications a measurement bandwidth of >500kHz serves little purpose other than to increase noise contribution and sensitivity to AM radio stations. Today's better distortion analyzers offer a selection of measurement bandwidths typically including 20kHz–22kHz, 30kHz, 80kHz, and wideband (300kHz–500kHz).

At first glance it might appear that THD+N measurements are inferior to THD only measurements because of the sensitivity to wideband noise. Even with their noise contribution today's distortion analyzers offer the lowest residual distortion, hence the most accuracy in making ultra-low distortion measurements. The typical residual contribution of spectrum analyzers is usually limited by their internal mixer stages to about 0.003% (-90dB). FFT analyzers do not fare much better due to A-D converter nonlinearities. The very best 16-bit converters available today do not guarantee residual distortion below about 0.002% although future developments promise to improve this situation. Distortion analyzers offer the lowest residual performance with at least one manufacturer claiming 0.0001% (typical).

"IMD" or InterModulation Distortion is yet another technique for quantifying nonlinearity. It is a much more specialized form of testing requiring a multi-tone test signal. IMD tests can be more sensitive than THD or THD+N tests because the specific test frequencies, ratios, and analyzer measurement technique can be chosen to optimize response to only certain forms of nonlinearity. Unfortunately this is also one of the biggest disadvantages of IMD testing because there are so many tests that have been suggested: SMPTE, CCIF, TIM, DIM, MTM, to name a few.

Distortion Measurement Accuracy

Nonlinear distortion is not a traceable characteristic in the sense that an unbroken chain of comparisons can be made to a truly distortion-*less* standard. Such a standard does not exist! Real world distortion measurements will always include the non-zero contributions from both the sinewave source and the analyzer.

It is a truly challenging task to *accurately* measure distortion below about 0.01% (-80dB). Indeed, distortion measurement errors can become quite large near residual levels. Harmonic contributions from the original sinewave and the analyzer can add algebraically, vectorially, or even cancel depending upon their relative phase. There are no general assumptions that can be made regarding how two residual contributions will add or subtract.

In the following equation let "M" be the measured value of the N-th harmonic, let "X" be the magnitude of the distortion contributed by the analyzer, and let "D" be the true distortion magnitude of some signal. The measured distortion will be influenced by the residual analyzer contribution:

$$M^* \sin(2\pi Nft+\phi)=D^* \sin(2\pi Nft)+X^* \sin(2\pi Nft+\Theta)$$

$$M=\begin{cases} (D+X) & \text{if } \Theta=0^\circ \\ (D^2+X^2)^{1/2} & \text{if } \Theta=\pm 90^\circ \\ (D-X) & \text{if } \Theta=180^\circ \end{cases} \qquad [4]$$

Depending upon the relative phase between the distortion components (Θ) a true distortion factor (D) of 0.0040% could be read as anything between 0.0025% to 0.0055% if the analyzer's internal distortion contribution (X) was 0.0015%. Conversely a 0.0040% reading could have resulted from a true distortion factor of anything from 0.0025% to 0.0055% with the same 0.0015% analyzer contribution.

It is very important to understand this concept when making distortion readings near the specified residual levels of the test equipment. A lower reading may not always signify lower distortion. A low reading could be the result of a fortuitous cancellation of two larger contributions. It is also illogical to conclude that the true value of distortion is always less than the reading because the non-zero residual contributions of the analyzer and sinewave. The service manual of one test equipment manufacturer incredibly states that a 0.0040% reading *verifies* their residual distortion guarantee of 0.0020% for both oscillator and analyzer!

All of the distortion measurement techniques give 0.5dB–1.0dB (5%–10%) reading accuracies at higher reading levels. Some distortion analyzers additionally provide average versus true RMS detection. Average detection is a carryover from the past and should be avoided because it will give erroneously low readings when multiple harmonics are present.

The Ultimate Meaning of THD and THD+N Measurements

Both THD and THD+N are measures of signal *impurity*. Distortion analyzers measure THD+N, not THD. Spectrum, wave, and FFT analyzers measure individual harmonic distortion from which THD can be calculated, but not THD+N. Is one better than the other?

For most applications THD+N is the more meaningful measurement because it quantifies total signal impurity. Particularly as we enter the age of A-D and D-A based systems (for example, digital audio) the engineer is increasingly confronted with effects and imperfections that introduce non-harmonic components to a signal. Wideband noise itself can be viewed as an imperfection to be minimized. It is truly myopic to exclude other potentially serious and undesirable signal components in the determination of signal quality just because they do not happen to be a harmonic of the test signal. Why should a 60Hz component be acceptable in the calculation of 20Hz THD but be excluded when testing with a 1kHz fundamental?

On the other hand THD measurements are distinctly better than THD+N measurements if the application is to quantify a simple transfer function nonlinearity. Noise, hum, and other interference products are not introduced by these simple forms of nonlinearity and should not influence the measurement. Examples include the distortion due to component voltage coefficient effects and non-ohmic contact behavior.

Given that all real signals contain some distortion, how much THD or THD+N is acceptable? Only the designer can make that determination.

APPENDIX E

SOME PRACTICAL CONSIDERATIONS FOR BRIDGE INTERFACES

It is often desirable to route bridge outputs over considerable cable lengths. Cable driving should always be approached with caution. Even shielded cables are susceptible to noise pick-up, and input protection is often in order. Figure E1 shows some options. Simple RC filters often suffice for filtering. The upper limit on resistor value is set by amplifier bias current. FET input amplifiers allow large values, useful for minimizing capacitance size and input protection. Leakage eliminates electrolytic capacitors as candidates, and the largest practical non-electrolytic devices are about 1µF Often, a single capacitor (dashed lines) is all that is required. Diode clamps prevent high voltage spikes or faults (common in industrial environments) from damaging the amplifier. Figure E2 summarizes some clamp alternatives.

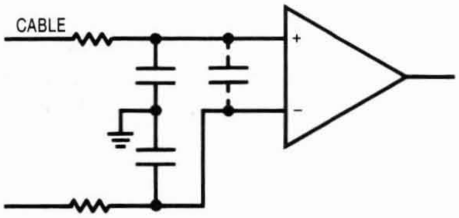


Figure E1. RC Filter Alternatives

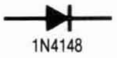
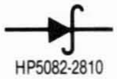
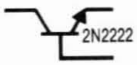
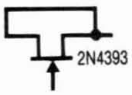
CLAMP TYPE	FORWARD DROP	LEAKAGE @ 25°C (15V REVERSE)
 1N4148	≈0.6V	≈10^{-9}A
 HP5082-2810	≈400mV	≈10^{-7}A
 2N2222  2N4393	≈0.6V	≈10^{-11}A

Figure E2. Various Devices Offer Different Clamp Characteristics

Figure E3 shows a high order switched capacitor based filter. The LTC1062 has no DC error, and offers much better roll-off characteristics than the simple RC types. LTC Application Note 20, "Application Considerations for an Instrumentation Lowpass Filter," presents details.

Figure E4 shows a pre-amplifier used ahead of the remotely located instrumentation amplifier. The pre-amp raises cable signal level while lowering drive impedance. The assymmetrical bridge loading should be evaluated when using this circuit. Usually, the amplifiers input resistor can be made large enough to minimize it's effect.

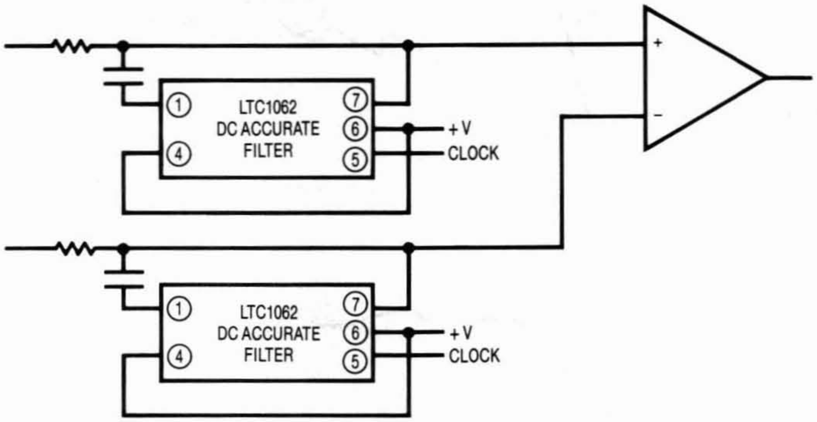


Figure E3. Switched Capacitor Techniques Permit a DC Accurate 5th Order Lowpass Filter

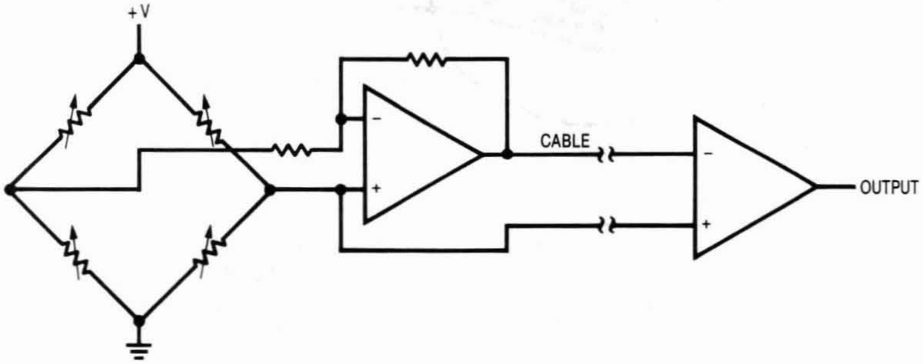
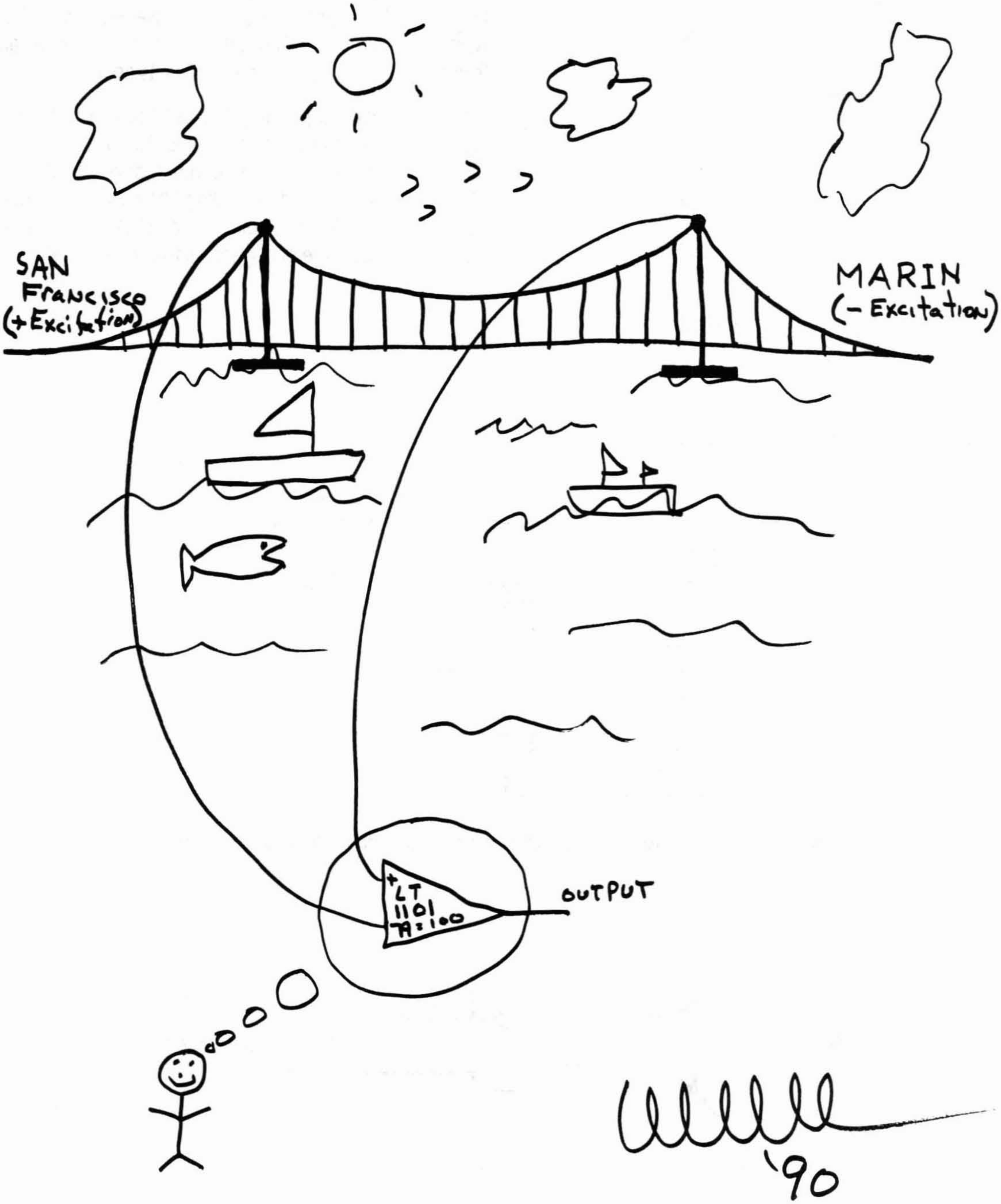


Figure E4. Pre-Amplifier Provides Gain and Low Impedance Drive to Cable


SAN Francisco (+Excitation)
MARIN (– Excitation)
+
LT 1101 A=100
OUTPUT
'90

Application Note 44
September 1991

LT1074/LT1076 Design Manual

Carl Nelson

INTRODUCTION

The use of switching regulators increased dramatically in the 1980's and this trend remains strong going into the 90s. The reasons for this are simple; heat and efficiency. Today's systems are shrinking continuously, while simultaneously offering greater electronic "horsepower." This combination would result in unacceptably high internal temperatures if low efficiency linear supplies were used. Heat sinks do not solve the problem in general because most systems are closed, with low thermal transfer from "inside" to "outside."

Battery powered systems need high efficiency supplies for long battery life. Topological considerations also require switching technology. For instance, a battery cannot generate an output higher than itself with linear supplies. The availability of low cost rechargeable batteries has created a spectacular rise in the number of battery powered systems, and consequently a matching rise in the use of switching regulators.

The LT1074 and LT1076 switching regulators are designed specifically for ease of use. They are close to the ultimate "three terminal box" concept which simply requires an input, output and ground connection to deliver power to the load. Unfortunately, switching regulators are not horseshoes, and "close" still leaves room for egregious errors in the final execution. This Application Note is intended to eliminate the most common errors that customers make with switching regulators as well as offering some insight into the inner workings of switching designs. There is also an entirely new treatment of inductor design based on the mathematical models of core loss and peak current. This allows the customer to quickly see the allowable limits for inductor value and make an intelligent decision based on the need for cost, size, etc. The procedure differs greatly from previous design techniques and many experienced designers at first think it can't work. They quickly become silent after standard laborious trial-and-error techniques yield identical results.

There is an old adage in woodworking — "Measure twice, cut once." This advice holds for switching regulators, also. Read AN44 through quickly to familiarize yourself with the contents. Then reread the pertinent sections carefully to avoid "cutting" the design two, three, or four times. Some switching regulator errors, such as excessive ripple current in capacitors, are time bombs best fixed *before* they are expensive field failures.

Since this paper was originally written, Linear Technology has produced a CAD program for switching regulators called SwitcherCAD. This program uses the ideas presented in this application note, but adds an extra level of accuracy by factoring in more second order effects. It also takes the drudgery out of the iterative design procedure, allowing rapid "what if" exploration. I highly recommend using SwitcherCAD after absorbing the basic concepts presented here. It cuts design time considerably, presents detailed information on operating conditions, and has many safeguards to prevent unreliable designs. One caution, however; SwitcherCAD has an initial run sequence, called Novice Mode, which generates a very conservative design from database components. The results of this initial design may not correlate with AN44 procedures because of assumptions used in SwitcherCAD and because of the limited number of components in the database. Changing to Expert Mode allows all components to be changed at will.

SwitcherCAD does not calculate components for loop stability. Linear Technology will be creating several separate programs for this purpose during 1993. Contact our Application department for details.

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ABSOLUTE MAXIMUM RATINGS

Input Voltage
- LT1074/ LT1076 .... 45V
- LT1074HV/76HV 64V

Switch Voltage with Respect to Input Voltage
- LT1074/ 76 .... 64V
- LT1074HV/76HV 75V

Switch Voltage with Respect to Ground Pin (V_{SW} **Negative**)
- LT1074/76 (Note 6) 35V
- LT1074HV/76HV (Note 6) 45V

Feedback Pin Voltage .... −2V, +10V

Shutdown Pin Voltage (Not to Exceed V_{IN}) 40V

Status Pin Voltage 30V
- (Current Must Be Limited to 5mA When Status Pin Switches "On")

I_{LIM} Pin Voltage (Forced) 5.5V

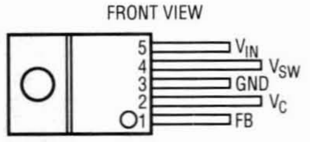
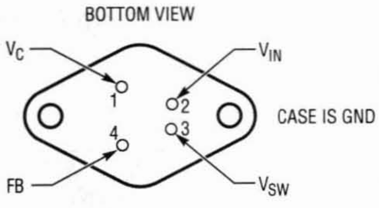
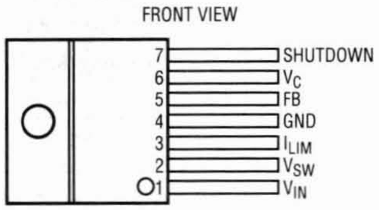
Maximum Operating Ambient Temperature Range
- LT1074C/76C, LT1074HVC/76HVC .... 0°C to 70°C
- LT1074M/76M, LT1074HVM/76HVM .. −55°C to 125°C

Maximum Operating Junction Temperature Range
- LT1074C/76C, LT1074HVC/76HVC .... 0°C to 125°C
- LT1074M/76M, LT1074HVM/76HVM ... −55°C to 150°C

Maximum Storage Temperature .... −65°C to 150°C

Lead Temperature (Soldering, 10 sec.) .... 300°C

PACKAGE/ORDER INFORMATION

	ORDER PART NUMBER
 FRONT VIEW 5 V_{IN} 4 V_{SW} 3 GND 2 V_C 1 FB T PACKAGE 5-LEAD TO-220 LEADS ARE FORMED STANDARD FOR STRAIGHT LEADS, ORDER FLOW 06	LT1074CT LT1074HVCT LT1076CT LT1076HVCT
 BOTTOM VIEW V_C V_{IN} 1 2 4 3 CASE IS GND FB V_{SW} K PACKAGE 4-LEAD TO-3 METAL CAN	LT1074MK LT1074HVMK LT1074CK LT1074HVCK LT1076MK LT1076HVMK LT1076CK LT1076HVCK
 FRONT VIEW 7 SHUTDOWN 6 V_C 5 FB 4 GND 3 I_{LIM} 2 V_{SW} 1 V_{IN} Y PACKAGE 7-LEAD TO-220	LT1074CY

ELECTRICAL CHARACTERISTICS

T_j = 25°C, V_{IN} = 25V, unless otherwise noted.

PARAMETER	CONDITIONS			MIN	TYP	MAX	UNITS
Switch "On" Voltage (Note 1)	LT1074	I_{SW} = 1A, $T_j \geq 0°C$				1.85	V
		I_{SW} = 1A, $T_j < 0°C$				2.1	V
		I_{SW} = 5A, $T_j \geq 0°C$				2.3	V
		I_{SW} = 5A, $T_j < 0°C$				2.5	V
	LT1076	I_{SW} = 0.5A	●			1.2	V
		I_{SW} = 2A	●			1.7	V
Switch "Off" Leakage	LT1074	$V_{IN} \leq 25V$, $V_{SW} = 0$			5	300	µA
		$V_{IN} = V_{MAX}$, $V_{SW} = 0$ (Note 7)			10	500	µA
	LT1076	V_{IN} = 25V, $V_{SW} = 0$				150	µA
		$V_{IN} = V_{MAX}$, $V_{SW} = 0$ (Note 7)				250	µA
Supply Current (Note 2)	V_{FB} = 2.5V, $V_{IN} \leq 40V$		●		8.5	11	mA
	40V < V_{IN} < 60V		●		9	12	mA
	V_{SHUT} = 0.1V (Device Shutdown) (Note 8)		●		140	300	µA

ELECTRICAL CHARACTERISTICS $T_j = 25°C$, $V_{IN} = 25V$, unless otherwise noted.

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Minimum Supply Voltage	Normal Mode	●		7.3	8	V
	Startup Mode (Note 3)	●		3.5	4.8	V
Switch Current Limit (Note 4)	LT1074 I_{LIM} Open	●	5.5	6.5	8.5	A
	$R_{LIM} = 10k$ (Note 5)			4.5		A
	$R_{LIM} = 7k$ (Note 5)			3		A
	LT1076 I_{LIM} Open	●	2	2.6	3.2	A
	$R_{LIM} = 10k$ (Note 5)			1.8		A
	$R_{LIM} = 7k$ (Note 5)			1.2		A
Maximum Duty Cycle		●	85	90		%
Switching Frequency			90	100	110	kHz
	$T_j \leq 125°C$	●	85		120	kHz
	$T_j > 125°C$	●	85		125	kHz
	$V_{FB} = 0V$ through 2kΩ (Note 4)			20		kHz
Switching Frequency Line Regulation	$8V \leq V_{IN} \leq V_{MAX}$ (Note 7)	●		0.03	0.1	%/V
Error Amplifier Voltage Gain (Note 6)	$1V \leq V_C \leq 4V$			2000		V/V
Error Amplifier Transconductance			3700	5000	8000	µmho
Error Amplifier Source and Sink Current	Source ($V_{FB} = 2V$)		100	140	225	µA
	Sink ($V_{FB} = 2.5V$)		0.7	1	1.6	mA
Feedback Pin Bias Current	$V_{FB} = V_{REF}$	●		0.5	2	µA
Reference Voltage	$V_C = 2V$	●	2.155	2.21	2.265	V
Reference Voltage Tolerance	V_{REF} (Nominal) = 2.21V			±0.5	±1.5	%
	All Conditions of Input Voltage, Output Voltage, Temperature and Load Current	●		±1	±2.5	%
Reference Voltage Line Regulation	$8V \leq V_{IN} \leq V_{MAX}$ (Note 7)	●		0.005	0.02	%/V
V_C Voltage at 0% Duty Cycle				1.5		V
	Over Temperature	●		−4		mV/°C
Multiplier Reference Voltage				24		V
Shutdown Pin Current	$V_{SH} = 5V$	●	5	10	20	µA
	$V_{SH} \leq V_{THRESHOLD}$ (≅2.5V)	●			50	µA
Shutdown Thresholds	Switch Duty Cycle = 0	●	2.2	2.45	2.7	V
	Fully Shut Down	●	0.1	0.3	0.5	V
Status Window	As a Percent of Feedback Voltage		4	±5	6	%
Status High Level	$I_{STATUS} = 10µA$ Sourcing	●	3.5	4.5	5.0	V
Status Low Level	$I_{STATUS} = 1.6mA$ Sinking	●		0.25	0.4	V
Status Delay Time				9		µs
Status Minimum Width				30		µs
Thermal Resistance Junction to Case	LT1074				2.5	°C/W
	LT1076				4.0	°C/W

The ● denotes the specifications which apply over the full operating temperature range.

Note 1: To calculate maximum switch "on" voltage at currents between low and high conditions, a linear interpolation may be used.

Note 2: A feedback pin voltage (V_{FB}) of 2.5V forces the V_C pin to its low clamp level and the switch duty cycle to zero. This approximates the zero load condition where duty cycle approaches zero.

Note 3: Total voltage from V_{IN} pin to ground pin must be ≥ 8V after startup for proper regulation.

Note 4: Switch frequency is internally scaled down when the feedback pin voltage is less than 1.3V to avoid extremely short switch on times. During testing, V_{FB} is adjusted to give a minimum switch on time of 1µs.

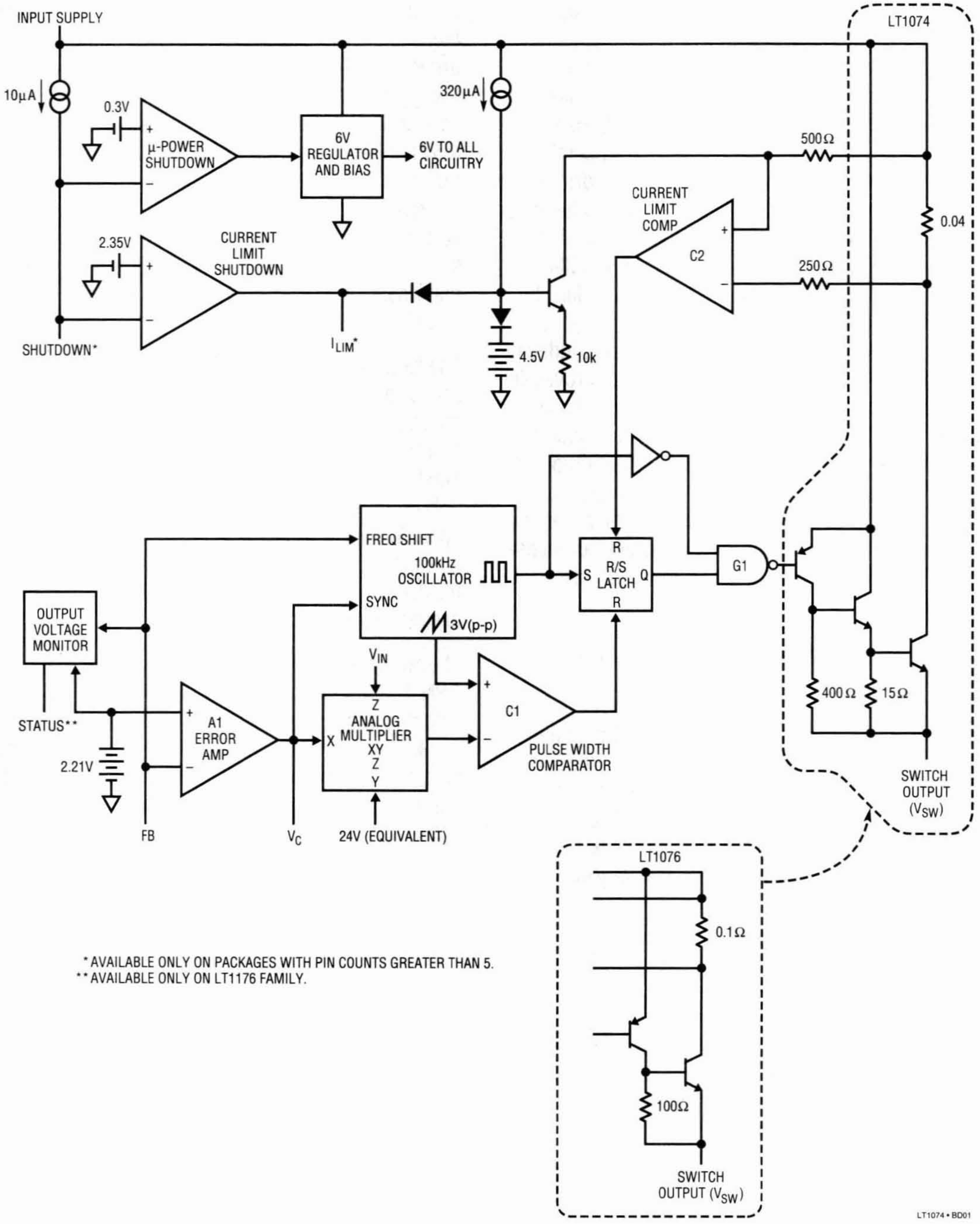
Note 5: $I_{LIM} \approx \frac{R_{LIM} - 1k}{2k}$ (LT1074), $I_{LIM} \approx \frac{R_{LIM} - 1k}{5.5k}$ (LT1076).

Note 6: Switch to input voltage limitation must also be observed.

Note 7: $V_{MAX} = 40V$ for the LT1074/76 and 60V for the LT1074HV/76HV.

Note 8: Does not include switch leakage.

BLOCK DIAGRAM


INPUT SUPPLY
LT1074
10μA
320μA
0.3V
+
μ-POWER SHUTDOWN
–
6V REGULATOR AND BIAS
6V TO ALL CIRCUITRY
500Ω
CURRENT LIMIT COMP
C2
0.04
2.35V
CURRENT LIMIT SHUTDOWN
250Ω
SHUTDOWN*
I_{LIM}*
4.5V
10k
FREQ SHIFT
100kHz OSCILLATOR
SYNC
3V(p-p)
R
S
R/S LATCH
Q
G1
OUTPUT VOLTAGE MONITOR
STATUS**
V_{IN}
A1 ERROR AMP
2.21V
Z
ANALOG MULTIPLIER
X
XY
Y
C1
PULSE WIDTH COMPARATOR
400Ω
15Ω
SWITCH OUTPUT (V_{SW})
FB
V_C
24V (EQUIVALENT)
LT1076
0.1Ω
100Ω
SWITCH OUTPUT (V_{SW})
LT1074 • BD01

* AVAILABLE ONLY ON PACKAGES WITH PIN COUNTS GREATER THAN 5.
** AVAILABLE ONLY ON LT1176 FAMILY.

BLOCK DIAGRAM DESCRIPTION

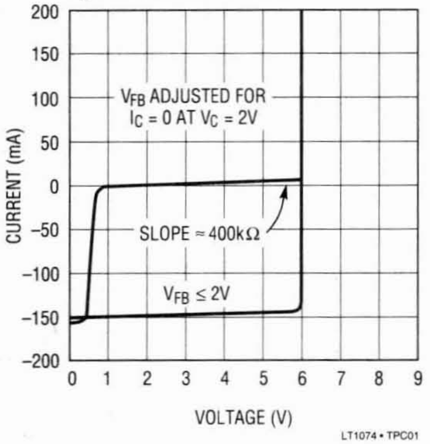
A switch cycle in the LT1074 is initiated by the oscillator setting the R/S latch. The pulse that sets the latch also locks out the switch via gate G1. The effective width of this pulse is approximately 700ns, which sets the maximum switch duty cycle to approximately 93% at 100kHz switching frequency. The switch is turned off by comparator C1, which resets the latch. C1 has a sawtooth waveform as one input and the output of an analog multiplier as the other input. The multiplier output is the product of an internal reference voltage, and the output of the error amplifier, A1, divided by the regulator input voltage. In standard buck regulators, this means that the output voltage of A1 required to keep a constant regulated output is independent of regulator input voltage. This greatly improves line transient response, and makes loop gain independent of input voltage. The error amplifier is a transconductance type with a G_M at null of approximately 5000μmho. Slew current going positive is 140μA, while negative slew current is about 1.1mA. This asymmetry helps prevent overshoot on startup. Overall loop frequency compensation is accomplished with a series RC network from V_C to ground.

Switch current is continuously monitored by C2, which resets the R/S latch to turn the switch off if an overcurrent condition occurs. The time required for detection and switch turn-off is approximately 600ns. So minimum switch "on" time in current limit is 600ns. Under dead shorted output conditions, switch duty cycle may have to be as low as 2% to maintain control of output current. This would require switch on time of 200ns at 100kHz switching frequency, so frequency is reduced at very low output voltages by feeding the FB signal into the oscillator and creating a linear frequency downshift when the FB signal drops below 1.3V. Current trip level is set by the voltage on the I_{LIM} pin which is driven by an internal 320μA current source. When this pin is left open, it self-clamps at about 4.5V and sets current limit at 6.5A for the LT1074 and 2.6A for the LT1076. In the 7-pin package an external resistor can be connected from the I_{LIM} pin to ground to set a lower current limit. A capacitor in parallel with this resistor will soft start the current limit. A slight offset in C2 guarantees that when the I_{LIM} pin is pulled to within 200mV of ground, C2 output will stay high and force switch duty cycle to zero.

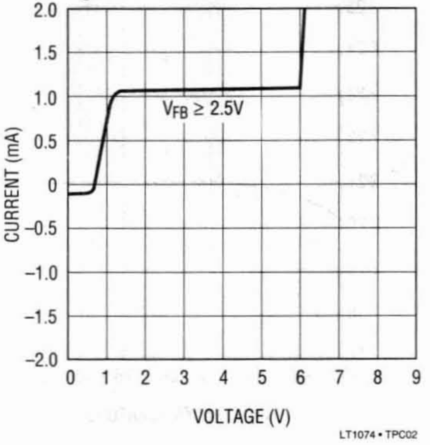
The "Shutdown" pin is used to force switch duty cycle to zero by pulling the I_{LIM} pin low, or to completely shut down the regulator. Threshold for the former is approximately 2.35V, and for complete shutdown, approximately 0.3V. Total supply current in shutdown is about 150μA. A 10μA pull-up current forces the shutdown pin high when left open. A capacitor can be used to generate delayed startup. A resistor divider will program "undervoltage lockout" if the divider voltage is set at 2.35V when the input is at the desired trip point.

The switch used in the LT1074 is a Darlington NPN (single NPN for LT1076) driven by a saturated PNP. Special patented circuitry is used to drive the PNP on and off very quickly even from the saturation state. This particular switch arrangement has no "isolation tubs" connected to the switch output, which can therefore swing to 40V below ground.

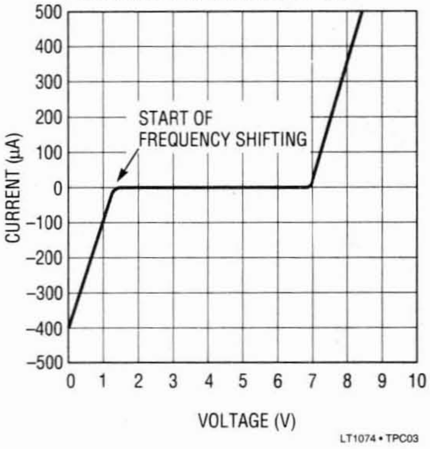
TYPICAL PERFORMANCE CHARACTERISTICS



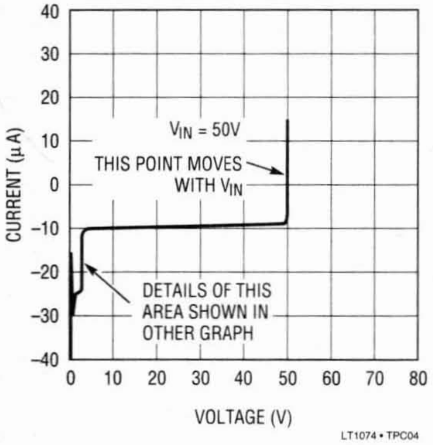
V_C Pin Characteristics



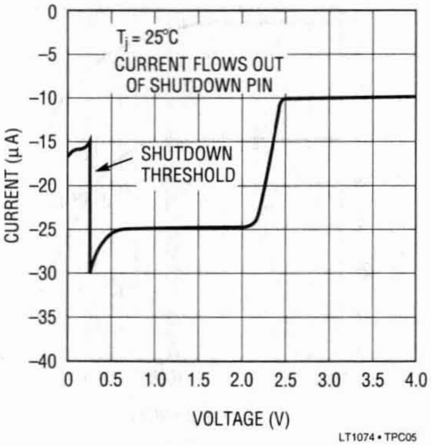
V_C Pin Characteristics



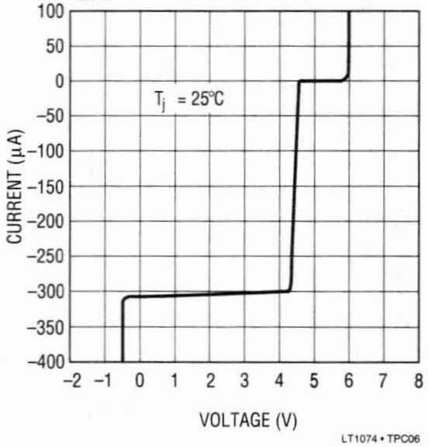
Feedback Pin Characteristics



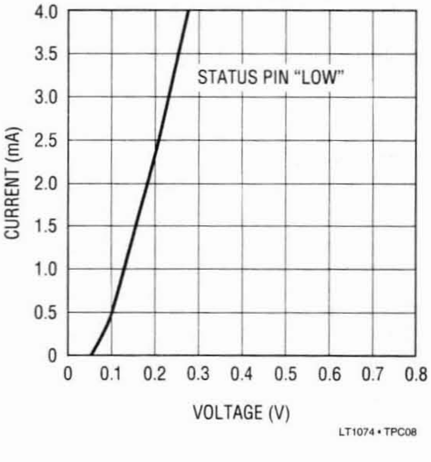
Shutdown Pin Characteristics



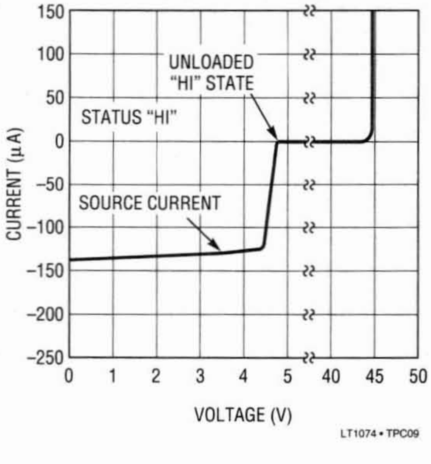
Shutdown Pin Characteristics



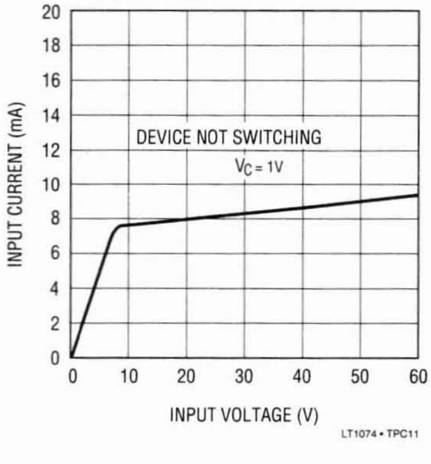
I_{LIM} Pin Characteristics



Status Pin Characteristics



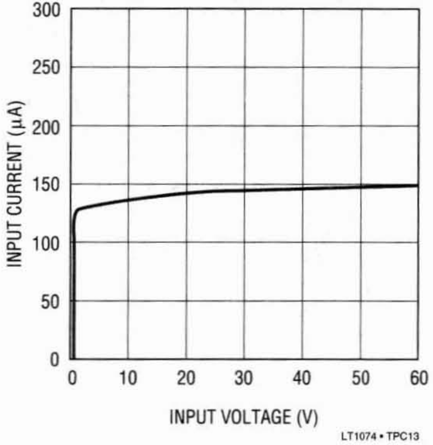
Status Pin Characteristics



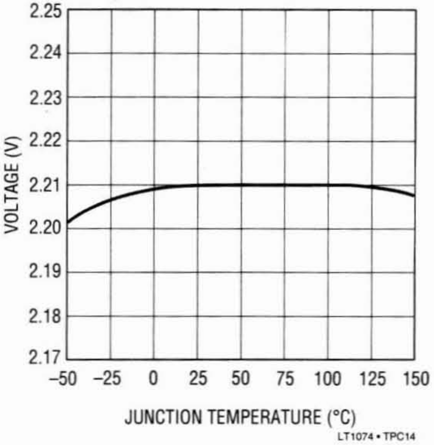
Supply Current

TYPICAL PERFORMANCE CHARACTERISTICS

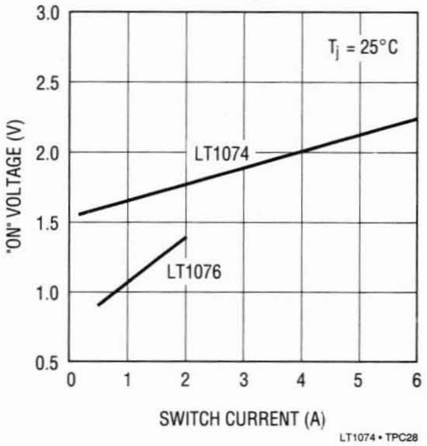
Supply Current (Shutdown)



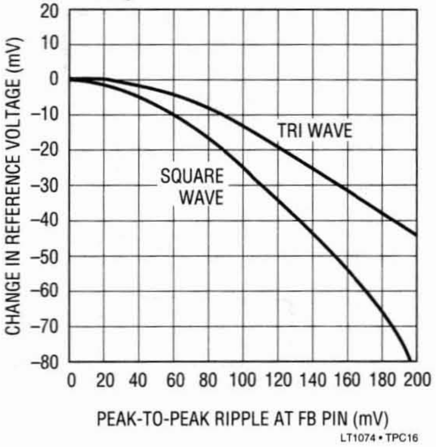
Reference Voltage vs Temperature



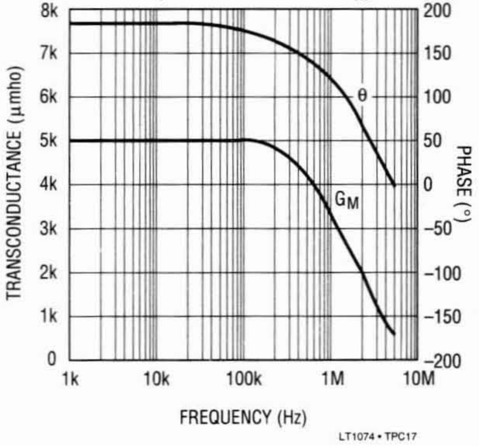
Switch "On" Voltage



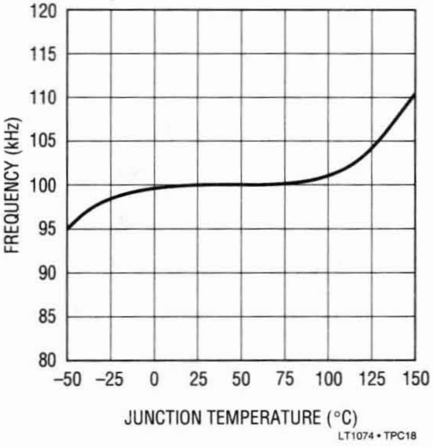
Reference Shift with Ripple Voltage



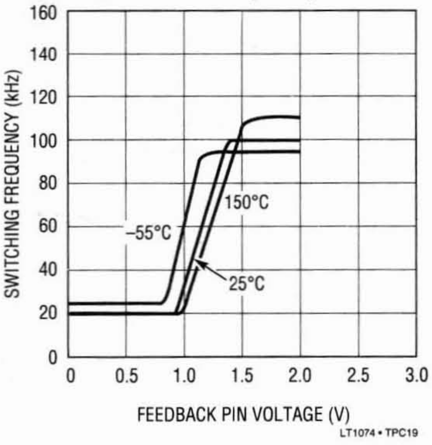
Error Amplifier Phase and G_M



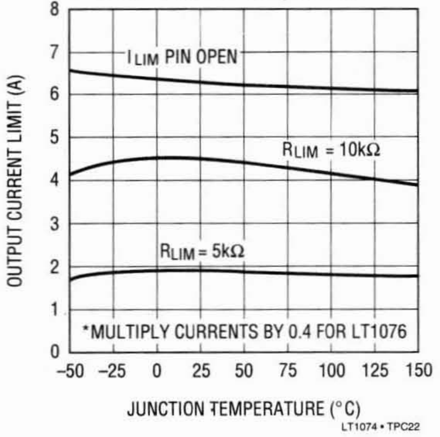
Switching Frequency vs Temperature



Feedback Pin Frequency Shift



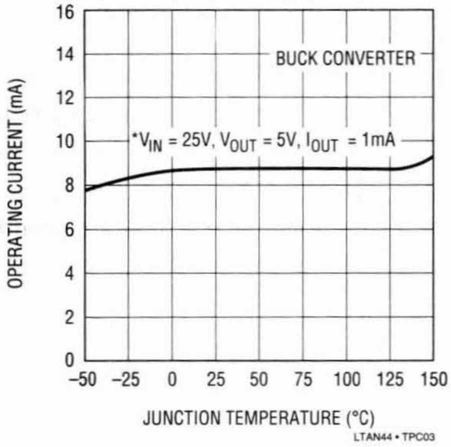
Current Limit vs Temperature*



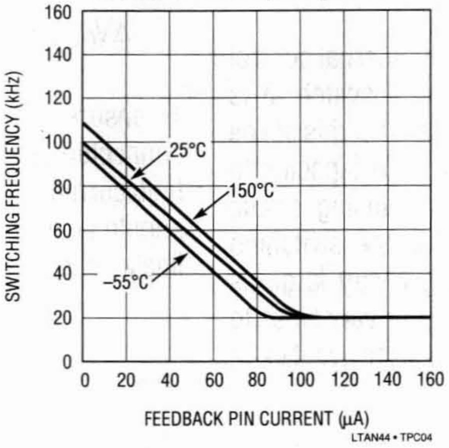
*MULTIPLY CURRENTS BY 0.4 FOR LT1076

TYPICAL PERFORMANCE CHARACTERISTICS

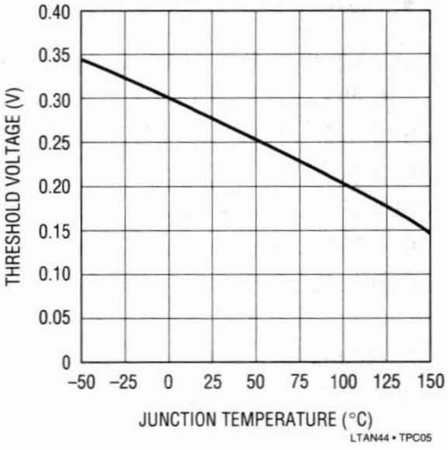
Operating Input Supply Current*



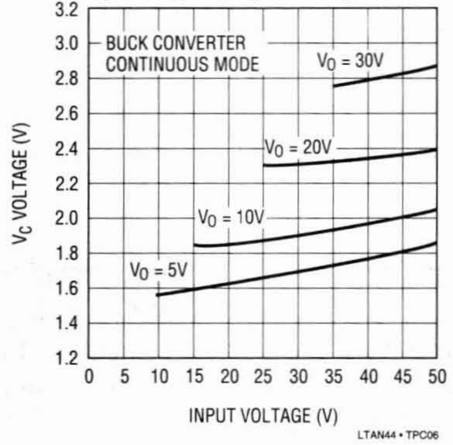
Feedback Pin Frequency Shift



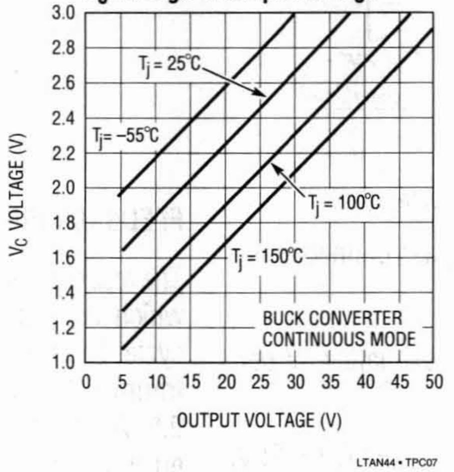
Shutdown Threshold



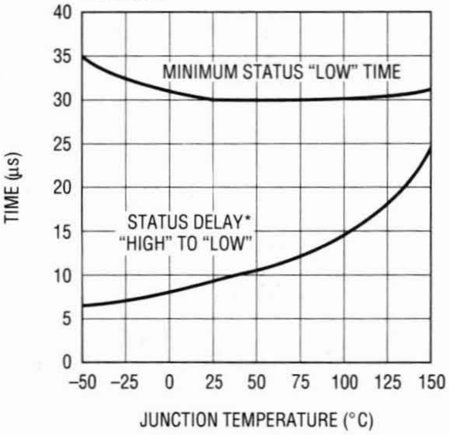
V_C Voltage vs Input Voltage



V_C Voltage vs Output Voltage



Status Delay and Minimum Timeout



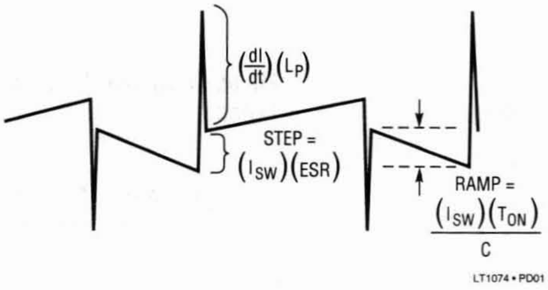
* STATUS WILL NOT GO LOW IF OUTPUT IS OUTSIDE WINDOW FOR LESS THAN DELAY TIME

LTAN44 • TPC08

PIN DESCRIPTIONS

V_{IN} PIN

The V_{IN} pin is both the supply voltage for internal control circuitry and one end of the high current switch. It is important, *especially at low input voltages*, that this pin be bypassed with a low ESR, and low inductance capacitor to prevent transient steps or spikes from causing erratic operation. At full switch current of 5A, the switching transients at the regulator input can get very large as shown in Figure 1. Place the input capacitor very close to the regulator and connect it with wide traces to avoid extra inductance. Use radial lead capacitors.



$\left(\frac{dI}{dt}\right)(L_P)$
STEP = $(I_{SW})(ESR)$
RAMP = $\frac{(I_{SW})(T_{ON})}{C}$
LT1074 • PD01

Figure 1. Input Capacitor Ripple

L_P = Total inductance in input bypass connections and capacitor.

"Spike" height $\left(\frac{dI}{dt} \bullet L_P\right)$ is approximately 2V *per inch* of lead length.

Step = 0.25V for ESR = 0.05Ω and I_{SW} = 5A is 0.25V.
Ramp = 125mV for C = 200µF, T_{ON} = 5µs, and I_{SW} = 5A is 125mV.

Input current on the V_{IN} Pin in shutdown mode is the sum of actual supply current (≈140µA, with a maximum of 300µA) and switch leakage current. Consult factory for special testing if shutdown mode input current is critical.

GROUND PIN

It might seem unusual to describe a ground pin, but in the case of regulators, the ground pin must be connected properly to ensure good load regulation. The internal reference voltage is referenced to the ground pin; so any error in ground pin voltage will be multiplied at the output;

$$\Delta V_{OUT} = \frac{(\Delta V_{GND})(V_{OUT})}{2.21}$$

To ensure good load regulation, the ground pin must be connected directly to the proper output node, so that no high currents flow in this path. The output divider resistor should also be connected to this low current connection line as shown in Figure 2.

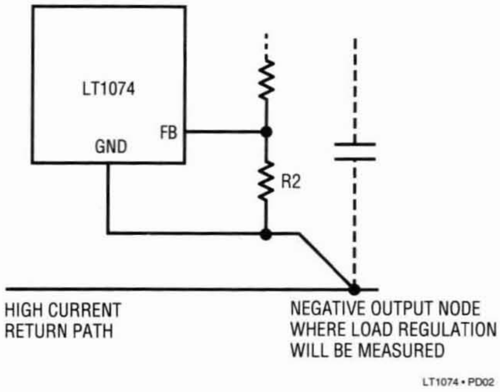


Figure 2. Proper Ground Pin Connection

FEEDBACK PIN

The feedback pin is the inverting input of an error amplifier which controls the regulator output by adjusting duty cycle. The non-inverting input is internally connected to a trimmed 2.21V reference. Input bias current is typically 0.5µA when the error amplifier is balanced (I_{OUT} = 0). The error amplifier has asymmetrical G_M for large input signals to reduce startup overshoot. This makes the amplifier more sensitive to large ripple voltages at the feedback pin. 100mVp-p ripple at the feedback pin will create a 14mV offset in the amplifier, equivalent to a 0.7% output voltage shift. To avoid output errors, output ripple (p-p) should be less than 4% of DC output voltage at the point where the output divider is connected.

See the "Error Amplifier" section for more details.

Frequency Shifting at the Feedback Pin

The error amplifier feedback pin (FB) is used to downshift the oscillator frequency when the regulator output voltage is low. This is done to guarantee that output short circuit

PIN DESCRIPTIONS

current is well controlled even when switch duty cycle must be extremely low. Theoretical switch "on" time for a buck converter in continuous mode is;

$$t_{ON} = \frac{V_{OUT} + V_D}{V_{IN} \bullet f}$$

V_D = Catch diode forward voltage (≈ 0.5V)
f = Switching frequency

At f = 100kHz, t_{ON} must drop to 0.2µs when V_{IN} = 25V and the output is shorted (V_{OUT} = 0V). In current limit, the LT1074 can reduce t_{ON} to a minimum value of ≈ 0.6µs, much too long to control current correctly for V_{OUT} = 0. To correct this problem, switching frequency is lowered from 100kHz to 20kHz as the FB pin drops from 1.3V to 0.5V. This is accomplished by the circuitry shown in Figure 3.

Q1 is off when the output is regulating (V_{FB} = 2.21V). As the output is pulled down by an overload, V_{FB} will eventually reach 1.3V, turning on Q1. As the output continues to drop, Q1 current increases proportionately and lowers the frequency of the oscillator. Frequency shifting starts when the output is ≈ 60% of normal value, and is down to its minimum value of ≅ 20kHz when the output is ≅ 20% of normal value. The rate at which frequency is shifted is determined by both the internal 3k resistor R3 and the external divider resistors. For this reason, R2 should not be increased to more than 4kΩ, if the LT1074 will be subjected to the simultaneous conditions of high input voltage and output short circuit.

SHUTDOWN PIN

The shutdown pin is used for undervoltage lockout, micropower shutdown, soft start, delayed start, or as a general purpose on/off control of the regulator output. It controls switching action by pulling the I_{LIM} pin low, which forces the switch to a continuous "off" state. Full micropower shutdown is initiated when the shutdown pin drops below 0.3V.

The V/I characteristics of the shutdown pin are shown in Figure 4. For voltages between 2.5V and ≈V_{IN}, a current of 10µA flows *out* of the shutdown pin. This current increases to ≈25µA as the shutdown pin moves through the 2.35V threshold. The current increases further to ≈ 30µA at the 0.3V threshold, then drops to ≈15µA as the shutdown voltage falls below 0.3V. The 10µA current source is included to pull the shutdown pin to its high or default state when left open. It also provides a convenient pullup for delayed start applications with a capacitor on the shutdown pin.

When activated, the typical collector current of Q1 in Figure 5, is ≈ 2mA. A soft start capacitor on the I_{LIM} pin will delay regulator shutdown in response to C1, by ≈(5V)(C_{LIM})/2mA. Soft start after full micropower shutdown is ensured by coupling C2 to Q1.

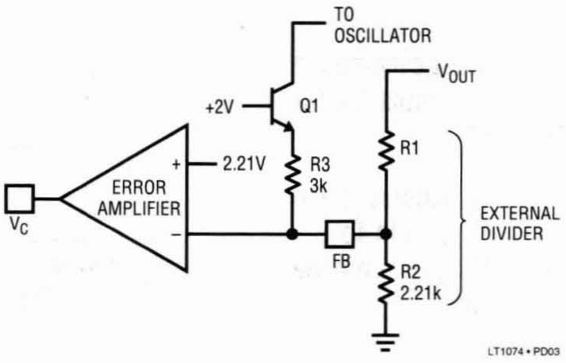


Figure 3. Frequency Shifting

PIN DESCRIPTIONS

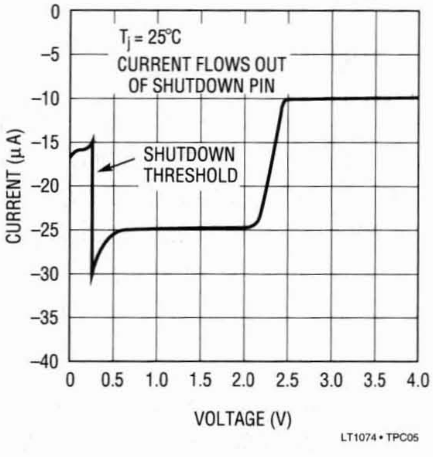


Figure 4. Shutdown Pin Characteristics

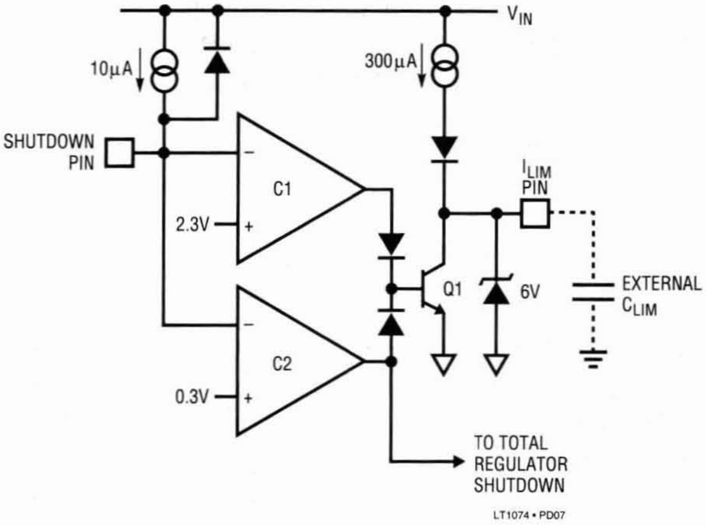

V_{IN}
10μA
300μA
SHUTDOWN PIN
C1
2.3V
C2
0.3V
I_{LIM} PIN
Q1
6V
EXTERNAL C_{LIM}
TO TOTAL REGULATOR SHUTDOWN
LT1074 • PD07

Figure 5. Shutdown Circuitry

Undervoltage Lockout

Undervoltage lockout point is set by R1 and R2 in Figure 6. To avoid errors due to the 10μA shutdown pin current, R2 is usually set at 5k, and R1 is found from:

$$R1 = R2\frac{(V_{TP} - V_{SH})}{V_{SH}}$$

V_{TP} = Desired undervoltage lockout voltage.
V_{SH} = Threshold for lockout on the shutdown pin = 2.45V.

If quiescent supply current is critical, R2 may be increased up to 15kΩ, but the denominator in the formula for R2 should replace V_{SH} with V_{SH} – (10μA)(R2).

Hysteresis in undervoltage lockout may be accomplished by connecting a resistor (R3) from the I_{LIM} pin to the shutdown pin as shown in Figure 7. D1 prevents the shutdown divider from altering current limit.

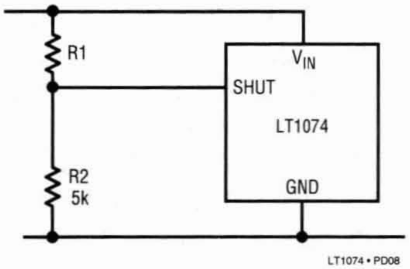
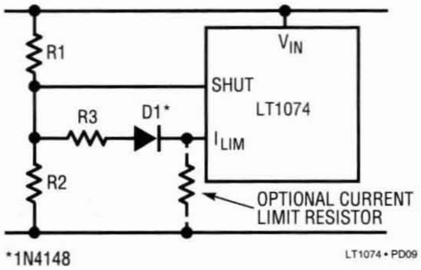

R1
V_{IN}
SHUT
LT1074
R2
5k
GND
LT1074 • PD08

Figure 6. Undervoltage Lockout


R1
V_{IN}
SHUT
LT1074
R3
D1*
I_{LIM}
R2
OPTIONAL CURRENT LIMIT RESISTOR
LT1074 • PD09

*1N4148

Figure 7. Adding Hysteresis

PIN DESCRIPTIONS

$$\text{Trip Point} = V_{TP} = 2.35V\left(1+\frac{R1}{R2}\right)$$

If R3 is added, the lower trip point (V_{IN} descending) will be the same. The upper trip point (V_{UTP}) will be;

$$V_{UTP} = V_{SH}\left(1+\frac{R1}{R2}+\frac{R1}{R3}\right) - 0.8V\left(\frac{R1}{R3}\right)$$

If R1 and R2 are chosen, R3 is given by

$$R3 = \frac{(V_{SH} - 0.8V)(R1)}{V_{UTP} - V_{SH}\left(1+\frac{R1}{R2}\right)}$$

Example: An undervoltage lockout is required such that the output will not start until $V_{IN} = 20V$, but will continue to operate until V_{IN} drops to 15V. Let R2 = 2.32k.

$$R1 = (2.32k)\frac{(15V - 2.35V)}{2.35V} = 12.5k$$

$$R3 = \frac{(2.35 - 0.8)(12.5)}{20 - 2.35\left(1+\frac{12.5}{2.32}\right)} = 3.9k$$

STATUS PIN (AVAILABLE ONLY ON LT1176 PARTS)

The status pin is the output of a voltage monitor "looking" at the feedback pin. It is low for a feedback voltage which is more than 5% above or below nominal. "Nominal" in this case means the internal reference voltage, so that the ±5% window tracks the reference voltage. A time delay of ≈ 10µs prevents short spikes from tripping the status low. Once it does go low, a second timer forces it to stay low for a minimum of ≈ 30µs.

The status pin is modeled in Figure 8 with a 130µA pullup to a 4.5V clamp level. The sinking drive is a saturated NPN with ≈100Ω resistance and a maximum sink current of approximately 5mA. An external pullup resistor can be added to increase output swing up to a maximum of 20V.

When the status pin is used to indicate "output OK," it becomes important to test for conditions which might create unwanted status states. These include output overshoot, large signal transient conditions, and excessive output ripple. "False" tripping of the status pin can usually be controlled by a pulse stretcher network as shown in Figure 8. A single capacitor (C1) will suffice to delay an output "OK" (status high) signal to avoid false "true" signals during start-up, etc. Delay time for status high will be approximately (2.3×10^4) (C1), or 23ms/µF. Status low delay will be much shorter, ≈ 600µs/µF.

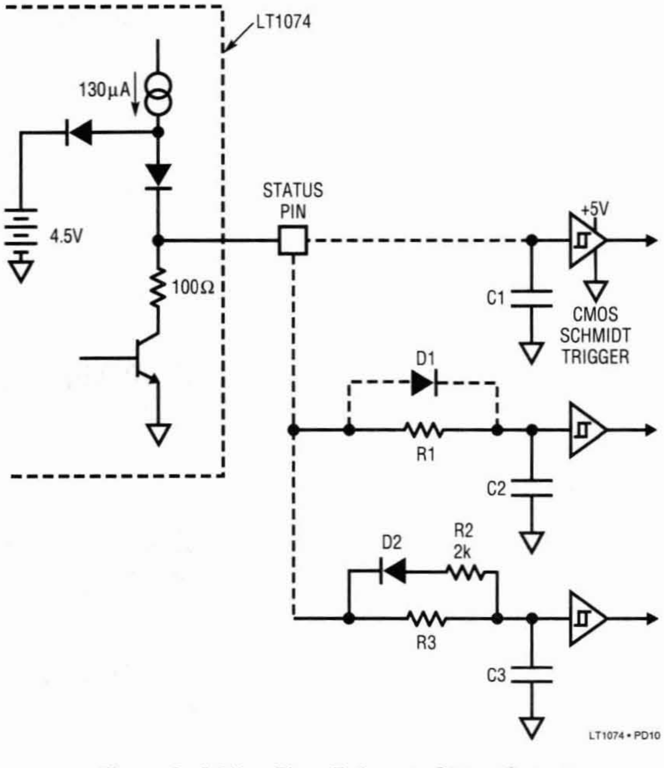


Figure 8. Adding Time Delays to Status Output

PIN DESCRIPTIONS

If false tripping of status "low" could be a problem, R1 can be added. Delay of status high remains the same if R1 ≤ 10kΩ. Status low delay is extended by R1 to approximately R1 • C2 seconds. Select C2 for high delay and R1 for low delay.

Example: Delay status high for 10ms, and status low for 3ms.

$$C2 = \frac{10\text{ms}}{23\text{ms}/\mu\text{F}} = 0.47\mu\text{F}\ (\text{Use } 0.47\mu\text{F})$$

$$R1 = \frac{3\text{ms}}{C2} = \frac{3\text{ms}}{0.47\mu\text{F}} = 6.4\text{k}\Omega$$

In this example D1 is not needed because R1 is small enough to not limit the charging of C2.

If very fast "low" tripping combined with long "high" delays is desired, use the D2, R2, R3, C3 configuration. C3 is chosen first to set "low" delay

$$C3 \approx \frac{t_{LOW}}{2\text{k}\Omega}$$

R3 is then selected for "high" delay

$$R3 \approx \frac{t_{HIGH}}{C3}$$

For t_{LOW} = 100µs and t_{HIGH} = 10ms, C3 = 0.05µF and R3 = 200kΩ.

I_{LIM} PIN

The I_{LIM} pin is used to reduce current limit below the preset value of 6.5A. The equivalent circuit for this pin is shown in Figure 9.

When I_{LIM} is left open, the voltage at Q1 base clamps at 5V through D2. Internal current limit is determined by the current through Q1. If an external resistor is connected between I_{LIM} and ground, the voltage at Q1 base can be reduced for lower current limit. The resistor will have a voltage across it equal to (320µA) (R), limited to ≈ 5V when clamped by D2. Resistance required for a given current limit is

$$R_{LIM} = I_{LIM}\ (2\text{k}\Omega) + 1\text{k}\Omega\ (\text{LT1074})$$

$$R_{LIM} = I_{LIM}\ (5.5\text{k}\Omega) + 1\text{k}\Omega\ (\text{LT1076})$$

As an example, a 3A current limit would require 3A (2k) + 1k = 7kΩ for the LT1074. The accuracy of these formulas is ±25% for $2A \le I_{LIM} \le 5A$ (LT1074) and $0.7A \le I_{LIM} \le 1.8A$ (LT1076), so I_{LIM} should be set at least 25% above the *peak* switch current required.

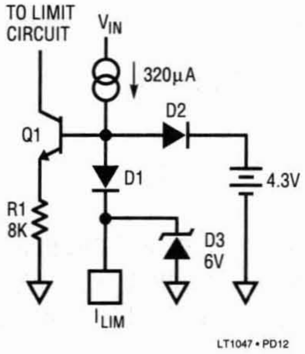


Figure 9. I_{LIM} Pin Circuit

Foldback current limiting can be easily implemented by adding a resistor from the output to the I_{LIM} pin as shown in Figure 10. This allows full desired current limit (with or without R_{LIM}) when the output is regulating, but reduces current limit under short circuit conditions. A typical value for R_{FB} is 5kΩ, but this may be adjusted up or down to set the amount of foldback. D2 prevents the output voltage from forcing current back into the I_{LIM} pin. To calculate a

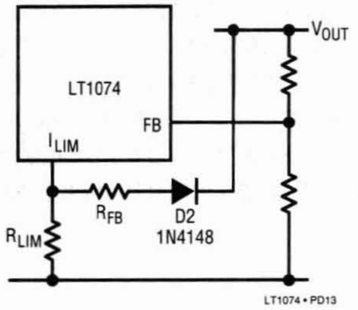


Figure 10. Foldback Current Limit

PIN DESCRIPTIONS

value for R_{FB}, first calculate R_{LIM}, then R_{FB};

$$R_{FB} = \frac{(I_{SC} - 0.44^*)(R_L)}{0.5^*(R_L - 1k\Omega) - I_{SC}} \; (R_L \text{ in } k\Omega)$$

*Change 0.44 to 0.16, and 0.5 to 0.18 for LT1076.

Example: $I_{LIM} = 4A$, $I_{SC} = 1.5A$, $R_{LIM} = (4)(2k) + 1k = 9k$

$$R_{FB} = \frac{(1.5 - 0.44)(9k\Omega)}{0.5(9k - 1k) - 1.5} = 3.8k\Omega$$

ERROR AMPLIFIER

The error amplifier in Figure 11 is a single stage design with added inverters to allow the output to swing above and below the common mode input voltage. One side of the amplifier is tied to a trimmed internal reference voltage of 2.21V. The other input is brought out as the FB (feedback) pin. This amplifier has a G_M (voltage "in" to current "out") transfer function of ≈5000μmho. Voltage gain is determined by multiplying G_M times the total equivalent output loading, consisting of the output resistance of Q4 and Q6 in parallel with the series RC external frequency compensation network. At DC, the external RC is ignored, and with a parallel output impedance for Q4 and Q6 of 400kΩ, voltage gain is ≈ 2000. At frequencies above a few hertz, voltage gain is determined by the external compensation, R_C and C_C.

$$A_V = \frac{G_m}{2\pi \bullet f \bullet C_C} \text{ at midfrequencies}$$

$$A_V = G_m \bullet R_C \text{ at highfrequencies}$$

Phase shift from the FB pin to the V_C pin is 90° at midfrequencies where the external C_C is controlling gain, then drops back to 0° (actually 180° since FB is an inverting input) when the reactance of C_C is small compared to R_C. The low frequency "pole" where the reactance of C_C is equal to the output impedance of Q4 and Q6 (r_O), is

$$f_{POLE} = \frac{1}{2\pi \bullet r_O \bullet C} \quad r_O \approx 400k\Omega$$

Although f_{POLE} varies as much as 3:1 due to r_O variations, mid-frequency gain is dependent only on G_M, which is specified much tighter on the data sheet. The higher frequency "zero" is determined solely by R_C and C_C.

$$f_{ZERO} = \frac{1}{2\pi \bullet R_C \bullet C_C}$$

The error amplifier has *asymmetrical* peak output current. Q3 and Q4 current mirrors are unity gain, but the Q6 mirror has a gain of 1.8 at output null and a gain of 8 when the FB pin is high (Q1 current = 0). This results in a maximum positive output current of 140μA and a maximum negative (sink) output current of ≅ 1.1mA. The asymmetry is deliberate — it results in much less regulator output overshoot during rapid startup or following the release of an output overload. Amplifier offset is kept low by area scaling Q1 and Q2 at 1.8:1.

Amplifier swing is limited by the internal 5.8V supply for positive outputs and by D1 and D2 when the output goes low. Low clamp voltage is approximately one diode drop (≈ 0.7V – 2mV/°C).

Note that both the FB pin and the V_C pin have other internal connections. Refer to the frequency shifting and sychronizing discussions.

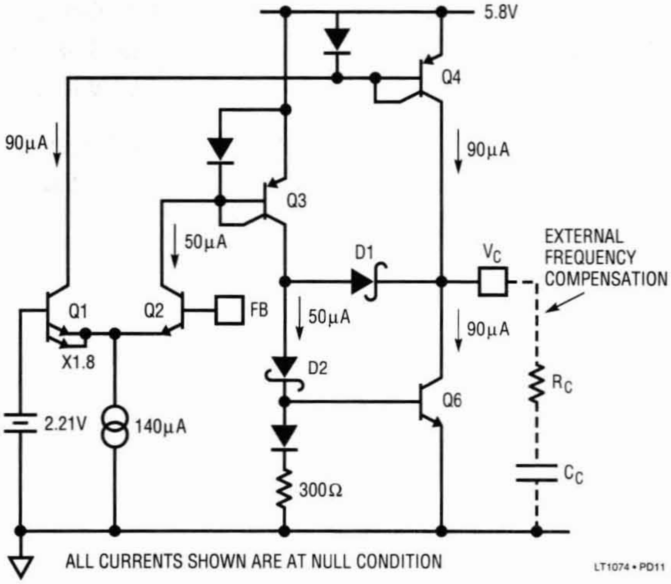


Figure 11. Error Amplifier

DEFINITION OF TERMS

V_{IN}: DC input voltage.

V_{IN}': DC input voltage minus switch voltage loss. V_{IN}' is 1.5 V to 2.3V less than V_{IN}, depending on switch current.

V_{OUT}: DC output voltage.

V_{OUT}': DC output voltage plus catch diode forward voltage. V_{OUT}' is typically 0.4V to 0.6V more than V_{OUT}.

f: Switching frequency.

I_M: Maximum specified switch current I_M = 5.5A for the LT1074 and 2A for the LT1076.

I_{SW}: Switch current during switch on time. The current typically jumps to a starting value, then ramps higher. I_{SW} is the *average* value during this period unless otherwise stated. It is *not* averaged over the whole switching period, which includes switch off time.

I_{OUT}: DC output current.

I_{LIM}: DC output current limit.

I_{DP}: Catch diode forward current. This is the peak current for discontinuous operation and the average value of the current *pulse* during switch off time for continuous mode.

I_{DA}: Catch diode forward current averaged over one complete switching cycle. I_{DA} is used to calculate diode heating.

ΔI: Peak-to-peak ripple current in the inductor, also equal to peak current in the discontinuous mode. ΔI is used to calculate output ripple voltage and inductor core losses.

Vp-p: Peak-to-peak output voltage ripple. This does not include "spikes" created by fast rising currents and capacitor parasitic inductance.

t_{SW}: This is not really an actual rise or fall time. Instead, it represents the *effective* overlap time of voltage and current in the switch. t_{SW} is used to calculate switch power dissipation.

L: Inductance, usually measured with low AC flux density, and zero DC current. Note that large AC flux density can increase L by up to 30%, and large DC currents can decrease L dramatically (core saturation).

B_{AC}: *Peak* AC flux density in the inductor core, equal to one-half peak-to-peak AC flux density. Peak value is used because nearly all core loss curves are plotted with peak flux density.

N: Tapped-inductor or transformer turns ratio. Note the exact definition of N for each application.

μ: Effective permeability of core material used in the inductor. μ is typically 25-150. Ferrite material is much higher, but is usually gapped to reduce the effective value to this range.

V_e: Effective core material volume (cm^3).

L_e: Effective core magnetic path length (cm).

A_e: Effective core cross sectional area (cm^2).

A_W: Effective core or bobbin winding area.

L_t: Average length of one turn on winding.

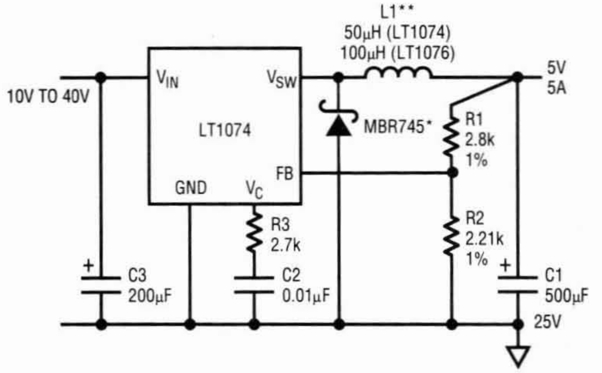
P_{CU}: Power dissipation caused by winding resistance. It does not include skin effect.

P_C: Power loss in the magnetic core. P_C depends only on *ripple current* in the inductor not DC current.

E: Overall regulator efficiency. It is simply output power divided by input power.

POSITIVE STEP-DOWN (BUCK) CONVERTER

The circuit in Figure 12 is used to convert a larger positive input voltage to a lower positive output. Typical waveforms are shown in Figure 13, with $V_{IN} = 20V$, $V_{OUT} = 5V$, $L = 50\mu H$, for both continuous mode (inductor current never drops to zero) with $I_{OUT} = 3A$ and discontinuous mode, where inductor current drops to zero during a portion of the switching cycle ($I_{OUT} = 0.17A$). Continuous mode maximizes output power but requires larger inductors. *Maximum* output current in true discontinuous mode is only one-half of switch current rating. Note that when load current is reduced in a continuous mode design, eventually the circuit will enter discontinuous mode. The LT1074 operates equally well in either mode and there is no significant change in performance when load current reduction causes a shift to discontinuous mode.



*USE MBR340 FOR LT1076
**COILTRONICS #50-2-52 (LT1074)
#100-1-52 (LT1076)

PULSE ENGINEERING, INC.
#PE-92114 (LT1074)
#PE-92102 (LT1076)
HURRICANE #HL-AK147QQ (LT1074)
#HL-AG210LL (LT1076)

LTAN44 • TA15

Figure 12. Basic Positive Buck Converter

Duty cycle of a buck converter in continuous mode is

$$DC = \frac{V_{OUT} + V_f}{V_{IN} - V_{SW}} = \frac{V_{OUT}'}{V_{IN}'} \qquad (01)$$

V_f = Forward voltage of catch diode
V_{SW} = Voltage loss across "on" switch

Note that duty cycle does not vary with load current except to the extent that V_f and V_{SW} change slightly.

A buck converter will change from continuous to discontinuous mode (and duty cycle will begin to drop) at a load current equal to

$$I_{OUT(CRIT)} = \frac{(V_{OUT}')(V_{IN}' - V_{OUT}')}{2 \bullet V_{IN}' \bullet f \bullet L} \qquad (02)$$

With the possible exception of load transient response, there is no reason to increase L to ensure continuous mode operation at light load.

Using the values from Figure 12, with $V_{IN} = 25V$, $V_f = 0.5V$, $V_{SW} = 2V$

$$DC = \frac{5 + 0.5}{25 - 2} = 24\% \qquad (03)$$

$$I_{OUT(CRIT)} = \frac{(5.5)(23 - 5.5)}{2(23)\left(10^5\right)\left(50 \times 10^{-6}\right)} = 0.42A$$

The "ringing" which occurs at some point in the switch "off" cycle in discontinuous mode is simply the resonance created by the catch diode capacitance plus switch capacitance in parallel with the inductor. This ringing does no harm and any attempt to dampen it simply wastes efficiency. Ringing frequency is given by;

$$f_{RING} = \frac{1}{2\pi\sqrt{L \bullet (C_{SW} + C_{DIODE})}} \qquad (04)$$

$C_{SW} \approx 80pF$
$C_{DIODE} = 200pF - 1000pF$

No off state ringing occurs in continuous mode because the diode is always conducting during switch off time and effectively shorts the resonance.

A detailed look at the leading edge of the switch waveform may reveal a second "ringing" tendency, usually at frequencies around 20MHz-50MHz. This is the result of the inductance in the loop which includes the input capacitor, the LT1074 leads, and the diode leads, combined with the capacitance of the catch diode. A total lead length of 4 inches will create ≈0.1μH. This coupled with 500pF of diode capacitance will create a damped 25MHz oscillation superimposed on the fast rising switch voltage waveform. Again, no harm is created by this ringing and no attempt should be made to dampen it other than minimizing lead length. Certain board layouts combined with very short interconnects and high diode capacitance may create a tuned circuit which resonates with the switch output to

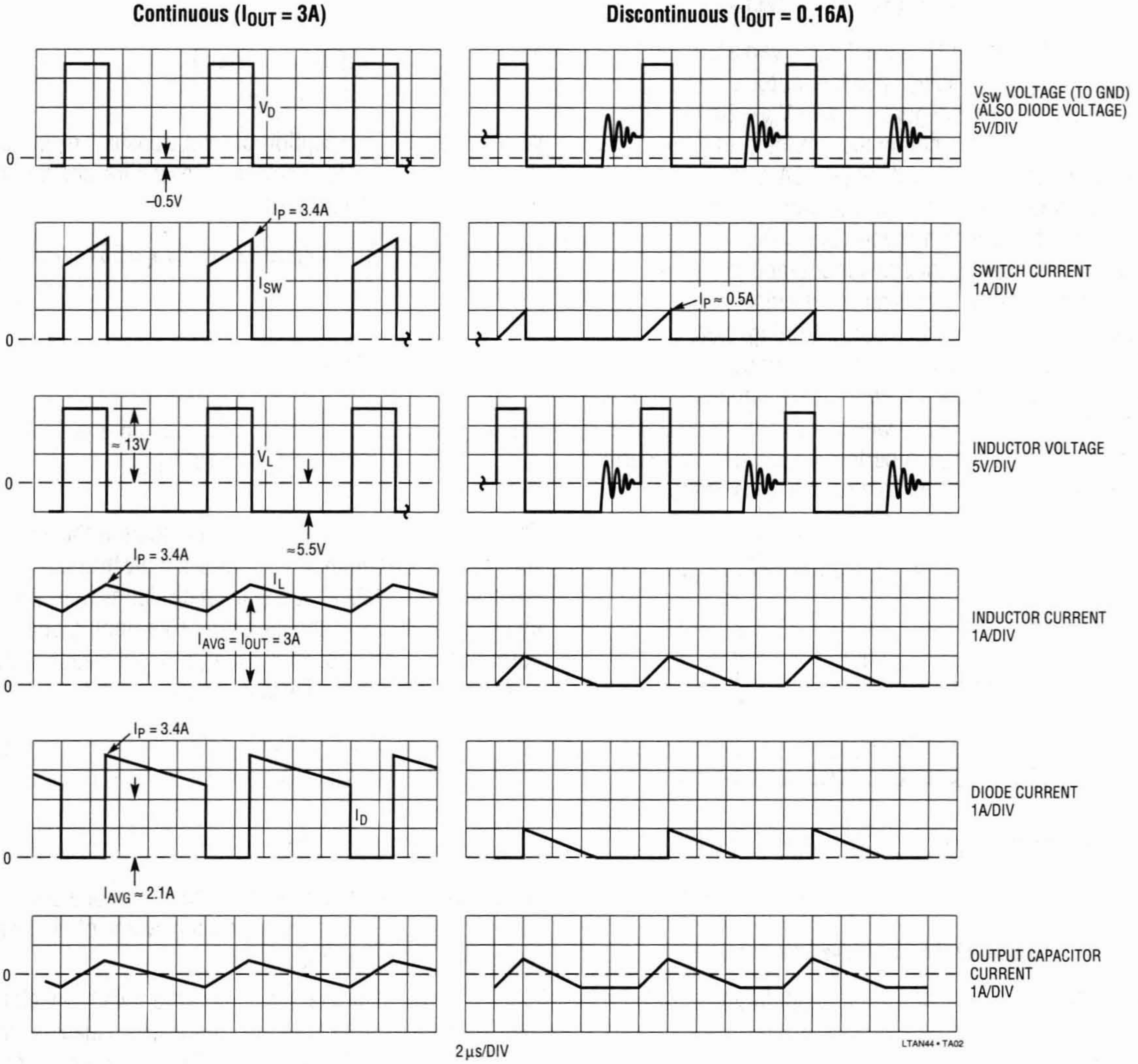


Figure 13. Buck Converter Waveforms with V_{IN} = 20V, L = 50µH

cause a low amplitude oscillation at the switch output during "on" time. This can be eliminated with a ferrite bead slipped over either diode lead during board assembly.

It is interesting to note that standard silicon fast recovery diodes create almost no ringing because of their lower capacitance and because they are effectively damped by their slower turn-off characteristics. This slower turn-off and the larger forward voltage represent additional power loss, so Schottky diodes are normally recommended.

Maximum output current of a buck converter is given by;

Continuous Mode (05)

$$I_{OUT(MAX)} = I_M - \frac{V_{OUT}\left(V_{IN} - V_{OUT}\right)}{2f \bullet V_{IN} \bullet L}$$

I_M = Maximum switch current (5.5A for LT1074)
V_{IN} = DC input voltage (maximum)
V_{OUT} = Output voltage
f = Switching frequency

For the example shown, with L = 50µH, and V_{IN} = 25V,

$$I_{OUT(MAX)} = 5.5 - \frac{5(25-5)}{2\left(10^5\right)(25)\left(50\times10^{-6}\right)} = 5.1\text{A} \quad (06)$$

Note that increasing inductor size to 100µH would only increase maximum output current by 4%, but decreasing it to 20µH would drop maximum current to 4.5A. Low inductance can be used for lower output currents, but core loss will increase.

Inductor

The inductor used in a buck converter acts as both an energy storage element and a smoothing filter. There is a basic tradeoff between good filtering versus size and cost. Typical inductor values used with the LT1074 range from 5µH to 200µH, with the small values used for lower power, minimum size applications and the larger values used to maximize output power or minimize output ripple voltage. The inductor must be rated for currents at least equal to output current and there are restrictions on ripple current (expressed as volt • microsecond product at various frequencies) to avoid core heating. For details on selecting an inductor and calculating losses, see the "Inductor Selection" section.

Output Catch Diode

D1 is used to generate a current path for L1 current when the LT1074 switch turns off. The current through D1 in continuous mode is equal to output current with a duty cycle of $(V_{IN} - V_{OUT})/V_{IN}$. For low input voltages, D1 may operate at duty cycles of 50% or less, but one must be very careful of utilizing this fact to minimize diode heat sinking. First, an unexpected high input voltage will cause duty cycle to increase. More important however, is a shorted output condition. When $V_{OUT} = 0$, diode duty cycle is ≈1 for any input voltage. Also, in current limit, diode current is not load current, but is determined by LT1074 switch current limit. If continuous output shorts must be tolerated, D1 must be adequately rated and heat sunk. 7 and 11-pin versions of the LT1074 allow current limit to be reduced to limit diode dissipation. 5-pin versions can be accurately current limited using the technique shown in Figure 20.

Under normal conditions, D1 dissipation is given by;

$$P_{DI} = I_{OUT}\frac{\left(V_{IN} - V_{OUT}\right)}{V_{IN}} \bullet V_f \quad (07)$$

V_f is the forward voltage of D1 at I_{OUT} current. Schottky diode forward voltage is typically 0.6V at the diode's full rated current, so it is normal design practice to use a diode rated at 1.5 to 2 times output current to maintain efficiency and allow margin for short circuit conditions. This derating allows V_f to drop to approximately 0.5V

Example: $V_{IN(MAX)}$ = 25V, I_{OUT} = 3A, V_{OUT} = 5V, assume V_f = 0.5V;

Full Load (08)

$$P_{DI} = \frac{(3)(25-5)(0.5\text{V})}{25} = 1.2\text{W}$$

Shorted Output

$$P_{DI} = (\approx 6\text{A})(\text{DC} = 1)(0.6\text{V}) = 3.6\text{W}$$

The high diode dissipation under shorted output conditions may necessitate current limit adjustment if adequate heat sinking cannot be provided.

Diode switching losses have been neglected because the reverse recovery time is assumed to be short enough to ignore. If a standard silicon diode is used, switching losses cannot be ignored. They can be approximated by;

$$Pt_{rr} \approx \left(V_{IN}\right)(f)\left(t_{rr}\right)\left(I_{OUT}\right) \quad (09)$$

t_{rr} = Diode reverse recovery time

Example: Same circuit with t_{rr} = 100ns

$$Pt_{rr} = (25)\left(10^5\right)\left(10^{-7}\right)(3) = 0.75\text{W} \quad (10)$$

Diodes with abrupt turn-off characteristics will transfer most of this power to the LT1074 switch. Soft recovery diodes will dissipate much of the power within the diode itself.

LT1074 Power Dissipation

The LT1074 draws about 7.5mA quiescent current, independent of input voltage or load. It draws an additional 5mA during switch "on" time. The switch itself dissipates a power approximately proportional to load current. This power is due to pure conduction losses (switch "on" voltage times switch current) and dynamic switching losses due to finite switch current rise and fall times. Total LT1074 power dissipation can by calculated from

$$P = V_{IN}\left[7mA + 5mA \bullet DC + 2I_{OUT} \bullet t_{SW} \bullet f\right] + \qquad (11)$$

$$DC\left[I_{OUT}\,(1.8V)^{*} + 0.1\Omega^{*}\left(I_{OUT}\right)^{2}\right]$$

$$DC = \text{Duty Cycle} \approx \frac{V_{OUT} + 0.5V}{V_{IN} - 2V}$$

t_{SW} = Effective overlap time of switch voltage and current

$\approx$ 50ns + (3ns/A) (I_{OUT}) (LT1074)
$\approx$ 60ns + (10ns/A) (I_{OUT}) (LT1076)

Example: V_{IN} = 25V, V_{OUT} = 5V, f = 100kHz, I_{OUT} = 3A

$$DC = \frac{5 + 0.5}{25 - 2} = 0.196 \qquad (12)$$

$$t_{SW} = 50ns + (3ns/A)(3A) = 59ns$$

$$P = \qquad (13)$$

$$25\begin{bmatrix}7mA + 5mA(0.196) + \\ (2)(3)(59ns)\left(10^{5}\right)\end{bmatrix} + 0.196\left[3(1.8) + 0.1(3)^{2}\right]$$

$$= \underbrace{0.21W}_{\substack{\text{Supply}\\ \text{Current}\\ \text{Loss}}} + \underbrace{0.89W}_{\substack{\text{Dynamic}\\ \text{Switching}\\ \text{Loss}}} + \underbrace{1.24W}_{\substack{\text{Switch}\\ \text{Conduction}\\ \text{Loss}}} = 2.34W$$

*LT1076 = 1V, 0.3Ω

Input Capacitor (Buck Converter)

A local input bypass capacitor is normally required for buck converters because the input current is a square wave with fast rise and fall times. This capacitor is chosen by ripple current rating—the capacitor must be large enough to avoid overheating created by its ESR and the AC RMS value of converter input current. For continuous mode;

$$I_{AC,RMS} = I_{OUT}\sqrt{\frac{V_{OUT}\left(V_{IN} - V_{OUT}\right)}{\left(V_{IN}\right)^{2}}} \qquad (14)$$

Worst case is at $V_{IN} = 2V_{OUT}$.

Power loss in the input capacitor is not insignificant in high efficiency applications. It is simply RMS capacitor current squared times ESR.

$$P_{C3} = \left(I_{AC,RMS}\right)^{2}(ESR) \qquad (15)$$

Example: V_{IN} = 20V-30V, I_{OUT} = 3A, V_{OUT} = 5V.

Worst case is at $V_{IN} = 2 \bullet V_{OUT} = 10V$, so use the closest V_{IN} value of 20V;

$$I_{AC,RMS} = 3A\sqrt{\frac{5(20 - 5)}{(20)^{2}}} = 1.3A\ RMS \qquad (16)$$

The input capacitor must be rated at a working voltage of 30V minimum and 1.3A ripple current. Ripple current ratings vary with maximum ambient temperature, so check data sheets carefully.

It is important to locate the input capacitor very close to the LT1074 and to use short leads (radial) when the DC input voltage is less than 12V. Spikes as high as 2V/inch of lead length will appear at the regulator input. If these spikes drop below ≈7V, the regulator will exhibit anomalous behavior. See "V_{IN} Pin" in the Pin Descriptions section.

You may be wondering why no mention has been made of capacitor value. That's because it doesn't really matter. Larger electrolytic capacitors are purely resistive (or inductive) at frequencies above 10kHz, so their bypassing impedance is resistive, and ESR is the controlling factor. For input capacitors used with the LT1074, a unit which meets ripple current ratings will provide adequate "bypassing" regardless of its capacitance value. Units with higher voltage rating will have lower capacitance for the same ripple current rating, but as a general rule, the *volume* required to meet a given ripple current/ESR is fixed over a wide range of capacitance/voltage rating. If the capacitor chosen for this application has 0.1Ω ESR, it will have a power loss of $(1.3A)^2\,(0.1\Omega) = 0.17W$.

Output Capacitor

In a buck converter, output ripple voltage is determined by both the inductor value and the output capacitor;

Continuous Mode (17)

$$Vp-p = \frac{(ESR)(V_{OUT})\left(1-\frac{V_{OUT}}{V_{IN}}\right)}{(L1)(f)}$$

Discontinuous Mode

$$Vp-p = ESR\sqrt{\frac{(2I_{OUT})(V_{OUT})(V_{IN}-V_{OUT})}{L \bullet f \bullet V_{IN}}}$$

Note that only the ESR of the output capacitor is used in the formula. It is assumed that the capacitor is purely resistive at frequencies above 10kHz. If an inductor value has been chosen, the formula can be rearranged to solve for ESR to aid in selecting a capacitor.

Continuous Mode (18)

$$ESR\,(MAX) = \frac{(Vp-p)(L1)(f)}{V_{OUT}\left(1-\frac{V_{OUT}}{V_{IN}}\right)}$$

Discontinuous Mode

$$ESR\,(MAX) = Vp-p\sqrt{\frac{L \bullet f \bullet V_{IN}}{2I_{OUT}(V_{OUT})(V_{IN}-V_{OUT})}}$$

Worst case output ripple is at highest input voltage. Ripple is independent of load for continuous mode and proportional to the square root of load current for discontinuous mode.

Example: Continuous mode with $V_{IN(MAX)} = 25V$, $V_{OUT} = 5V$, $I_{OUT} = 3A$, $L1 = 50\mu H$, $f = 100kHz$. Required maximum peak-to-peak output ripple is 25mV.

$$ESR = \frac{(0.025)\left(50\times10^{-6}\right)\left(10^{5}\right)}{(5)\left(1-\frac{5}{25}\right)} = 0.03\Omega \qquad (19)$$

A 10V capacitor with this ESR would have to be several thousand microfarads, and therefore fairly large. Tradeoffs which could be made include;

A. Paralleling several capacitors if component height is more critical than board area.

B. Increasing inductance. This can be done at no increase in size if a more expensive core (molypermalloy, etc.) is used.

C. Adding an output filter. This is often the best solution because the additional components are fairly low cost and their additional space is minimized by being able to "size down" the main L and C. See the "Output Filter" section.

Although ripple current is not usually a problem with buck converter output capacitors because the current is prefiltered by the inductor, a quick check should be done before a final capacitor is chosen—especially if the capacitor has been "downsized" to take advantage of an additional output filter. RMS ripple current into the output capacitor is

Continuous Mode (20)

$$I_{RMS} = \frac{0.29(V_{OUT})\left(1-\frac{V_{OUT}}{V_{IN}}\right)}{L1 \bullet f}$$

From the previous example:

$$I_{RMS} = \frac{0.29(5)\left(1-\frac{5}{25}\right)}{\left(50\times10^{-6}\right)\left(10^{5}\right)} = 0.23A\ RMS \qquad (21)$$

This ripple current is low enough to not be a problem, but that could change if the inductor was reduced by two or three to one and the output capacitor was minimized by adding an output filter.

The calculations for discontinuous mode RMS ripple current were considered too complicated for this discussion, but a conservative value would be 1.5 to 2 times output current.

To minimize output ripple, the output terminals of the regulator should be connected directly to the capacitor leads so that the diode (D1) and inductor currents do not circulate in output leads.

Efficiency

All the losses except those created by the inductor and the output filter are covered in this buck regulator section. The example used was a 5V, 3A output with 25V input. Calculated losses were: switch, 1.24W; diode, 1.2W; switching times, 0.89W; supply current, 0.21W; and input capacitor, 0.17W. Output capacitor losses were negligible . The sum of all these losses is 3.71W. Inductor loss is covered in a special section of this Application Note. Assume for this application that inductor copper loss is 0.3W and core loss is 0.15W. Total regulator loss is 4.16W. Efficiency is

$$E=\frac{I_{OUT}\bullet V_{OUT}}{I_{OUT}\bullet V_{OUT}+\Sigma P_L}=\frac{(3A)(5V)}{(3A)(5V)+4.16}=78\% \quad (22)$$

When considering improvements or tradeoffs of particular loss terms, keep in mind that a change in any one term will be attenuated by efficiency *squared.* For instance, if switch loss were reduced by 0.3W, this is 2% of the 15W output power, but only a $2(0.8)^2 = 1.28\%$ improvement in efficiency.

Output Divider

R1 and R2 set DC output voltage. R2 is normally set at 2.21kΩ (a standard 1% value) to match the LT1074 reference voltage of 2.21V, giving a divider current of 1mA. R1 is then calculated from

$$R1=\frac{R2\left(V_{OUT}-V_{REF}\right)}{V_{REF}} \quad (23)$$

If R2 = 2.21kΩ, R1 = $(V_{OUT} - V_{REF})$ kΩ

R2 may be scaled in either direction to suit other needs, but an upper limit of 4kΩ is suggested to ensure that the frequency shifting action created by the FB pin voltage is maintained under shorted output conditions.

Output Overshoot

Switching regulators often exhibit startup overshoot because the 2-pole LC network requires a fairly low unity gain frequency for the feedback loop. The LT1074 has asymmetrical error amplifier slew rate to help reduce overshoot, but it can still be a problem with certain combinations of L1C1 and C2R3. Overshoot should be checked on all designs by allowing the output to slew from zero in a no-load condition with maximum input voltage. This can be done by stepping the input or by pulling the V_C pin low through a diode connected to a 0V-10V square wave.

Worst case overshoot can occur on recovery from an output short because the V_C pin must slew from its high clamp state down to ≈1.3V. This condition is best checked with the brute force method of shorting and releasing the output.

If excessive output overshoot is found, the procedure for reducing it to a tolerable level is to first try increasing the compensation resistor. The error amplifier output must slew negative rapidly to control overshoot and its slew rate is limited by the compensation capacitor. The compensation resistor, however, allows the amplifier output to "step" downward very rapidly before slewing limitations begin. The size of this step is ≈(1.1mA)(R_C). If R_C can be increased to 3kΩ, the V_C pin can respond very quickly to control output overshoot.

If loop stability cannot be maintained with R_C = 3kΩ, there are several other solutions. Increasing the size of the output capacitor will reduce short-circuit-recovery overshoot by limiting output rise time. Reducing current limit will also help for the same reason. Reducing the compensation capacitor below 0.05μF helps because the V_C pin can then slew an appreciable amount during the allowable overshoot time.

The "final solution" to output overshoot is to clamp the V_C pin so that it does not have to slew as far to shut off the output. The V_C pin voltage in normal operation is known fairly precisely because it is made independent of everything except output voltage by the internal multiplier;

$$V_C \text{ Voltage} \approx 2\phi + \frac{V_{OUT}}{24} \tag{24}$$

$\phi = V_{BE}$ of internal transistor = 0.65V – 2mV/°C

To allow for transient conditions and circuit tolerances, a slightly different expression is used to calculate clamp level for the V_C pin

$$V_{C(CLAMP)} = 2\phi + \frac{V_{OUT}}{20} + \frac{V_{IN(MAX)}}{50} + 0.2V \tag{25}$$

For a 5V output with $V_{IN(MAX)}$ = 30V,

$$V_{C(CLAMP)} = 2(0.65) + \frac{5}{20} + \frac{30}{50} + 0.2 = 2.35V \tag{26}$$

There are several ways to clamp the V_C pin as shown in Figure 14. The simplest way is to just add a clamp Zener (D3). The problem is finding a low voltage Zener which does not leak badly below the knee. Maximum Zener leakage over temperature should be 40μA @ $V_C = 2\phi + V_{OUT}/20V$. One solution is to use an LM385-2.5V micropower reference diode where the calculated clamp level does not exceed 2.5V.

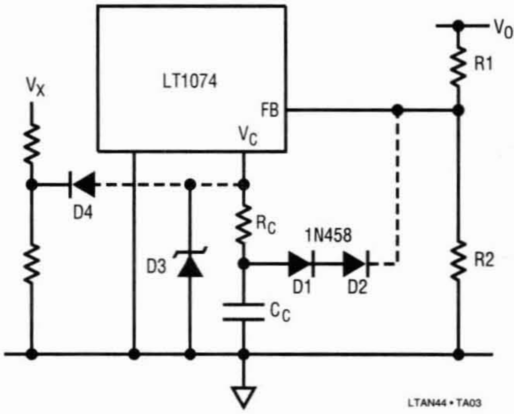


Figure 14. Clamping the V_C Pin

A second clamp scheme is to use a voltage divider and diode (D4). V_X must be some quasi-regulated source which does not collapse with regulator output voltage. A third technique can be used for outputs up to 20V. It clamps the V_C pin to the feedback pin with two diodes, D1 and D2. These are small signal nongold doped-diodes with a forward voltage that matches ϕ. The reason for this is start-up. V_C is essentially clamped to ground through the output divider when V_{OUT} = 0. It must be allowed to rise sufficiently to ensure start-up. The feedback pin will sit at about 0.5V with V_{OUT} = 0, because of the combined current from the feedback pin and V_C pin. The V_C voltage will be $2\phi + 0.5V + (0.14mA)(R_C)$. With $R_C = 1k\Omega$, $V_C = 1.94$. This is plenty to ensure start-up.

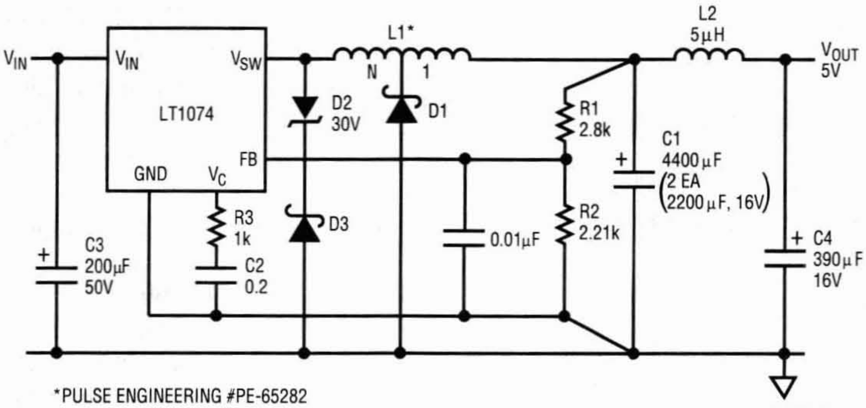
Overshoot Fixes that Don't Work

I know that these things don't work because I tried them. The first is soft start, created by allowing the output current or the V_C voltage to ramp up slowly. The first problem is that a slowly rising output allows more time for the V_C pin to ramp up well beyond its nominal control point so that it has to slew farther down to stop overshoot. If the V_C pin itself is ramped slowly, this can control input start-up overshoot, but it becomes very difficult to guarantee reset of the soft start for all conditions of input sequencing. In any case, these techniques do not address the problem of overshoot following overload of the output, because they do not get "reset" by the output.

Another common practice is to parallel the upper resistor in the output divider with a capacitor. This again works fine under limited conditions, but it is easily defeated by overload conditions which pull the output slightly below its regulated point long enough for the V_C pin to hit the positive limit (≈6V). The added capacitor remains charged and the V_C pin must slew almost 5V to control overshoot when the overload is released. The resulting overshoot is impressive—and often deadly.

TAPPED-INDUCTOR BUCK CONVERTER

Output current of a buck converter is normally limited to maximum switch current, but this restriction can be altered by tapping the inductor as shown in Figure 15. The ratio of "input" turns to "output" turns is "N" as shown in the schematic. The effect of the tap is to lengthen switch "on" time and therefore draw more power from the input without raising switch current. During switch "on" time, current delivered to the output through L1 is equal to switch current—5.5A maximum for the LT1074. When the switch turns off, inductor current flows only in the output section of L1, labeled "1," through D1 to the output. Energy conservation in the inductor requires that current increase by the ratio (N + 1):1. If N = 3, then maximum current delivered to the output during switch off



*PULSE ENGINEERING #PE-65282
D1 MOTOROLA MBR1635
D2 MOTOROLA P6KE30A
D3 1N5819

Figure 15. Tapped-Inductor Buck Converter

time is (3 + 1)(5.5A) = 22A. Average load current is increased to the weighted average of the 5A and 22A currents. Maximum output current is given by;

$$I_{OUT(MAX)} = \qquad (27)$$

$$0.95\left[I_{SW} - \frac{(V_{IN}' - V_{OUT}')(1+N)}{2Lf\left(N + \frac{V_{IN}'}{V_{OUT}'}\right)}\right]\left[\frac{N+1}{1+\frac{N \bullet V_{OUT}'}{V_{IN}'}}\right]$$

L = Total Inductance

The last term, $(N+1)/(1+N \bullet V_{OUT}/V_{IN})$ is the basic switch current multiplier term. At high input voltages it approaches N + 1, and theoretical output current approaches 18A for N = 3. For lower input voltages the multiplier term approaches unity and no benefit is gained by tapping the inductor. Therefore, when calculating maximum load current capability, always use the worst case low input voltage. The 0.95 multiplier is thrown-in to account for second order effects of leakage inductance, etc.

Example: $V_{IN(MIN)} = 20V$, N = 3, L = 100μH, $V_{OUT} = 5V$, Diode $V_f = 0.55V$, f = 100kHz. Let I_{SW} = Maximum for LT1074 = 5.5A, $V_{OUT}' = 5V + 0.55V = 5.55V$, $V_{IN}' = 20V - 2V = 18V$

$$I_{OUT(MAX)} = \qquad (28)$$

$$0.95\left[5.5 - \frac{(18-5.55)(1+3)}{2\left(10^{-4}\right)\left(10^{5}\right)\left(3+\frac{18}{5.5}\right)}\right]\left[\frac{3+1}{1+\frac{3(5.55)}{18}}\right]$$

$$= 0.95[5.5 - 0.4][2.08] = 10.08A$$

Duty cycle of the tapped-inductor converter is equal to;

$$DC = \frac{1+N}{N + \frac{V_{IN}'}{V_{OUT}'}} \qquad (29)$$

Average and peak diode currents are

$$I_{D(AVG)} = \frac{I_{OUT}\,(V_{IN}' - V_{OUT}')}{V_{IN}'} \qquad (30)$$

(Use Maximum V_{IN}')

$$I_{D(PEAK)} = \frac{I_{OUT}\,(N\,V_{OUT}' + V_{IN}')}{V_{IN}'}$$

(Use Minimum V_{IN}')

Average switch current *during switch on time is*

$$I_{SW(AVG)} = \frac{I_{OUT}\left(N \bullet V_{OUT}' + V_{IN}'\right)}{V_{IN}'(1+N)} \qquad (31)$$

(Use Minimum V_{IN}')

Diode peak reverse voltage is

$$V_{DI(PEAK)} = \frac{V_{IN} + N \bullet V_{OUT}}{1+N} \qquad (32)$$

(Use Maximum V_{IN})

Switch reverse voltage is

$$V_{SW} = V_{IN} + V_Z + V_{SPIKE} \qquad (33)$$

(Use Maximum V_{IN})

V_Z = Reverse breakdown of D2 (30V)

V_{SPIKE} = Narrow (<100ns) spike created by rapid switch turnoff and the stray wiring inductance of C3, D2, D3, and the LT1074 V_{IN} and switch pins. This voltage spike is approximately $I_{SW}/2$ *volts per inch* of total lead length.

Using parameters from the maximum output current example, with $V_{IN(MAX)}$ = 30V, I_{OUT} = 8A

$$DC\ @\ V_{IN} = 20V = \frac{1+3}{3+\dfrac{18}{5.55}} = 64\% \qquad (34)$$

$$I_{D(AVG)} = \frac{(8)(28-5.55)}{28} = 6.7A$$

$$I_{D(PEAK)}\ @\ V_{IN} = 20V = \frac{(8)(3 \bullet 5.55 + 18)}{18} = 15.4A$$

$$I_{SW(AVG)}\ @\ V_{IN} = 20V = \frac{(8)(3 \bullet 5.55 + 18)}{18(1+3)} = 3.85A$$

Note that this is the average switch current during "on" time. It must be multiplied by duty cycle and switch voltage drop to obtain switch power loss. Total loss also includes switch fall time (rise time losses are minimal due to leakage inductance in L1).

$$P_{SWITCH} = (I_{SW})(DC)\left[1.8V + (0.1)(I_{SW})\right] + (V_{IN}' + V_Z)(I_{SW})(f)(t_{SW}) \qquad (35)$$

$$t_{SW} = 50ns + 3ns \bullet I_{SW}$$

$$= (3.85)(0.64)\left[1.8 + (0.1)(3.85)\right] + (20+30)(3.85)\left(10^5\right)(62ns)$$

$$= 5.3W + 1.19W = 6.5W$$

$$V_{DI(PEAK)} = \frac{30+3.5}{1+3} = 11.25V \qquad (36)$$

$$V_{SW} = 30 + 30 + \frac{3.85}{2}(2'')^* = 64V$$

* This assumes 2" of lead length

Snubber

The tapped-inductor converter requires a snubber (D2 and D3) to clip off negative switching spikes created by the leakage inductance of L1. This inductance (L_L) is the value measured between the tap and the switch (N) terminal with the tap shorted to the output terminal. Theoretically, the measured inductance will be zero because the shorted turns reflect "0" ohms back to any other terminals. In practice, even with bifilar winding techniques, there is ≥1% leakage inductance compared to total inductance. This is ≈1.2µH for the PE-65282. L_L is modeled as a separate inductance in series with the "N" section input, which does not couple to the rest of the inductor. This gives rise to a negative spike at the switch pin at switch turnoff. D2 and D3 clip this spike to prevent switch damage, but D2 dissipates a significant amount of power. This power is equal to the energy stored in L_L at switch turnoff, ($E = (I_{SW})^2 \bullet L_L/2$) multiplied by switching frequency and a multiplier term which is dependent on the *difference* between D2 voltage and the normal reverse voltage swing at the inductor input.

$$P_{D2} = \frac{(I_{SW})^2 \bullet L_L}{2}(f)\left(\frac{V_Z}{V_Z - V_{OUT}' \bullet N}\right) \qquad (37)$$

For this example;

$$P_{D2} = \qquad (38)$$

$$\frac{(3.85)^2\left(1.2\times 10^{-6}\right)\left(10^5\right)}{2}\left(\frac{30}{30-5.55\bullet 3}\right) = 2W$$

Output Ripple Voltage

Output ripple on a tapped-inductor converter is higher than a simple buck converter because a square wave of current is superimposed on the normal triangular current fed to the output. Peak-to-peak ripple current delivered to the output is:

$$Ip-p = \qquad (39)$$

$$\frac{I_{OUT}\left(N\bullet V_{OUT}+V_{IN}\right)(N)}{V_{IN}(1+N)} + \frac{(1+N)\left(V_{IN}-V_{OUT}\right)}{f\bullet L\left(N+\frac{V_{IN}}{V_{OUT}}\right)}$$

$$\left(\text{Use Minimum } V_{IN}\right)$$

A conservative approximation of RMS ripple current is one-half of peak-to-peak current.

Output ripple voltage is simply the ESR of the output capacitor multiplied times Ip-p. In this example, with ESR = 0.03Ω

$$Ip-p = \qquad (40)$$

$$\frac{(8)(3\bullet 5+20)(3)}{20(1+3)} + \frac{(1+3)(20-5)}{\left(10^5\right)\left(10^{-4}\right)\left(3+\frac{20}{5}\right)} = 11.4A$$

$$I_{RMS} = 5.7A$$

$$Vp-p = (0.03)(11.4) = 340mV$$

This high value of ripple current and voltage requires some thought about the output capacitor. To avoid an excessively large capacitor, several smaller units are paralleled to achieve a combined 5.7A ripple current rating. The ripple voltage is still a problem for many applications. However, to reduce ripple voltage to 50mV would require an ESR of less than 0.005W—an impractical value. Instead, an output filter is added which attenuates ripple by more than 20:1.

Input Capacitor

The input bypass capacitor is selected by ripple current rating. It is assumed that all the converter input ripple current is supplied by the input capacitor. RMS input ripple current is approximately

$$I_{IN(RMS)} \approx \frac{\left(I_{OUT}\right)\left(V_{OUT}'\right)}{\left(V_{IN}'\right)(1+N)}\sqrt{(1+N)\left(\frac{V_{IN}'}{V_{OUT}'}-1\right)} \qquad (41)$$

$$\left(\text{Use Minimum } V_{IN}\right)$$

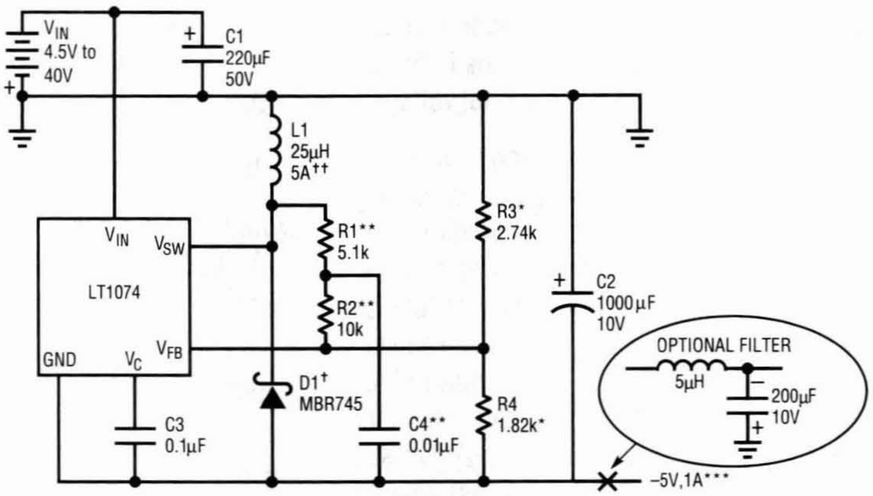
$$= \frac{(8)(5.5)}{(18)(1+3)}\sqrt{(1+3)\left(\frac{18}{5.5}-1\right)} = 1.84A\ RMS$$

The input capacitor value in microfarads is not particularly important since it is purely resistive at 100kHz; but it must be rated at the required ripple current and maximum input voltage. Radial lead types should be used to minimize lead inductance.

POSITIVE TO NEGATIVE CONVERTER

The LT1074 can be used to convert positive voltages to negative if the *sum* of input and output voltage is greater than the 8V minimum supply voltage specification, and the minimum positive supply is 4.75V. Figure 16 shows the LT1074 used to generate negative 5V. The ground pin of the device is connected to the negative output. This allows the feedback divider, R3 and R4, to be connected in the normal fashion. If the ground pin were tied to ground, some sort of level shift and inversion would be required to generate the proper feedback signal.

Positive to negative converters have a "right half plane zero" in the transfer function which makes them particularly hard to frequency stabilize, especially with low input voltage. R1, R2, and C4 have been added to the basic design solely to guarantee loop stability at low input voltage. They may be omitted for $V_{IN} > 10V$, or $V_{IN}/V_{OUT} > 2$. R1 plus R2 is in parallel with R3 for DC output voltage calculations. Use the following guidelines for these resistors:



* = 1% FILM RESISTORS
D1 = MOTOROLA-MBR745
C1 = NICHICON-UPL1C221MRH6
C2 = NICHICON-UPL1A102MRH6
L1 = COILTRONICS-CTX25-5-52

† LOWER REVERSE VOLTAGE RATING MAY BE USED FOR LOWER INPUT VOLTAGES. LOWER CURRENT RATING IS ALLOWED FOR LOWER OUTPUT CURRENT.

†† LOWER CURRENT RATING MAY BE USED FOR LOWER OUTPUT CURRENT.

** R1, R2, AND C4 ARE USED FOR LOOP FREQUENCY COMPENSATION, BUT R1 AND R2 MUST BE INCLUDED IN THE CALCULATION FOR OUTPUT VOLTAGE DIVIDER VALUES. FOR HIGHER OUTPUT VOLTAGES, INCREASE R1, R2 AND R3 PROPORTIONATELY;
$R3 = V_{OUT} - 2.37$ (KΩ)
$R1 = (R3)(1.86)$
$R2 = (R3)(3.65)$

*** MAXIMUM OUTPUT CURRENT OF 1A IS DETERMINED BY MINIMUM INPUT VOLTAGE OF 4.5V. HIGHER MINIMUM INPUT VOLTAGE WILL ALLOW MUCH HIGHER OUTPUT CURRENTS.

LTAN44 • TA05

Figure 16. Positive to Negative Converter

$$\begin{aligned} R4 &= 1.82k \\ R3 &= |V_{OUT}| - 2.37 \qquad (\text{In } k\Omega) \\ R1 &= R3\,(1.86) \\ R2 &= R3\,(3.65) \end{aligned}$$

If R1 and R2 are omitted:

$$\begin{aligned} R4 &= 2.21k \\ R3 &= |V_{OUT}| - 2.21 \qquad (\text{In } k\Omega) \end{aligned}$$

A +12V to –5V converter would have R4 = 2.21k and R3 = 2.74k.

Recommended compensation components would be C3 = 0.005µF in parallel with a series RC of 0.1µF and 1kΩ.

The converter works by charging L1 through the input voltage when the LT1074 switch is "on." During switch "off" time, the inductor current is diverted through D1 to the negative output. For continuous mode operation, duty cycle of the switch is

$$DC = \frac{V_{OUT}'}{V_{IN}' + V_{OUT}} \tag{42}$$

(Use absolute value for V_{OUT})

Peak switch current for continuous mode is

$$I_{SW(PEAK)} = \frac{I_{OUT}\left(V_{IN}' + V_{OUT}'\right)}{V_{IN}'} + \frac{\left(V_{IN}'\right)\left(V_{OUT}'\right)}{2f \bullet L\left(V_{IN}' + V_{OUT}'\right)} \tag{43}$$

To calculate maximum output current for a given maximum switch current (I_M) this can be rearranged as;

$$I_{OUT(MAX)} = \frac{V_{IN}' - (I_M)(R_L)}{V_{IN}' + V_{OUT}'}\left[I_M - \frac{\left(V_{IN}'\right)\left(V_{OUT}'\right)}{2f \bullet L\left(V_{IN}' + V_{OUT}'\right)}\right] \tag{44}$$

(Use Minimum V_{IN}')

Note that an extra term ($I_M \bullet R_L$) has been added. This is to account for the series resistance (R_L) of the inductor, which may become a significant loss at low input voltages.

Maximum output current is dependent upon input *and* output voltage, unlike the buck converter which will supply essentially a constant output current. The circuit shown will supply over 4A at V_{IN} = 30V, but only 1.3A at V_{IN} = 5V. The $I_{OUT(MAX)}$ equation does not include second order loss terms such as capacitor ripple current, switch rise and fall time, core loss, and output filter. These factors may reduce maximum output current by up to 10% at low input and/ or output voltages. Figure 17 shows $I_{OUT(MAX)}$ versus input voltage for various output voltages. It assumes a 25µH inductor for V_{OUT} = –5V, 50µH for V_{OUT} = –12V, and 100µH for V_{OUT} = –25V.

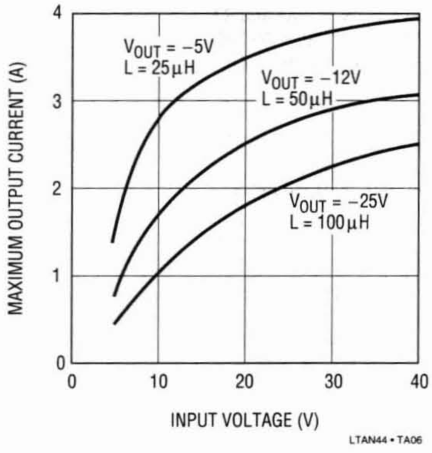


Figure 17. Maximum Output Current of Positive to Negative Converter

If absolute minimum circuit size is required and load currents are not too high, discontinuous mode can be used. Minimum inductance required for a specified load is;

Discontinuous Mode (45)

$$L_{MIN} = \frac{2I_{OUT}(V_{OUT}')}{(I_M)^2 \bullet f}$$

There is a maximum load current that can be supplied in discontinuous mode. Above this current, the formula for L_{MIN} is invalid. Maximum load current in discontinuous mode is;

Discontinuous Mode (46)

$$I_{OUT(MAX)} = \left(\frac{V_{IN}'}{V_{IN}' + V_{OUT}'}\right)\left(\frac{I_M}{2}\right)$$

(Use Minimum V_{IN})

Example: V_{OUT} = 5V, I_M = 5A, f = 100kHz, Load Current = 0.5A. Diode Forward Voltage = 0.5V, giving V_{OUT}' = 5.5V. V_{IN} = 4.7V to 5.3V. Assume $V_{IN}'_{(MIN)}$ = 4.7V – 2.3V = 2.4V.

$$I_{OUT(MAX)} = \left(\frac{2.4}{2.4 + 5.5}\right)\left(\frac{5}{2}\right) = 0.76A \quad (47)$$

The required load current of 0.5A is less than the maximum of 0.76A, so discontinuous can be used.

$$L_{MIN} = \frac{2(0.5)(5.5)}{(5)^2(10^5)} = 2.2\mu H \quad (48)$$

To ensure full load current with production variations of frequency and inductance, 3µH should be used.

The formula for minimum inductance assumes a high peak current in the inductor (≈5A). If the minimum inductance is used, the inductor must be specified to handle the high peak current without saturating. The high ripple current will also cause relatively high core loss and output ripple voltage, so some judgment must be used in minimizing the inductor size. See the "Inductor Selection" section for more details.

To calculate peak inductor and switch current in discontinuous mode, use

$$I_{PEAK} = \sqrt{\frac{2 \bullet I_{OUT} \bullet V_{OUT}'}{L \bullet f}} \quad (49)$$

Input Capacitor

C3 is used to absorb the large square wave switching currents drawn by positive to negative converters. It must have low ESR to handle the RMS ripple current and to avoid input voltage "dips" during switch on time, especially with 5V inputs. Capacitance value is not particularly important if ripple current and operating voltage requirements are met. RMS ripple current in the capacitor is

Continuous Mode (50)

$$I_{RMS} = I_{OUT}\sqrt{\frac{V_{OUT}'}{V_{IN}'}}$$

(Use Minimum V_{IN})

Discontinuous Mode* (51)

$$I_{RMS} = \frac{(I_{OUT})(V_{OUT}')}{V_{IN}'}\sqrt{\frac{1.35\left(1-\frac{m}{2}\right)^3}{m} + 0.17m^2 + 1 - m}$$

$$m = \frac{1}{V_{IN}'}\sqrt{2L\,f\,I_{OUT}\,V_{OUT}'}$$

*This formula is a test for calculator students

Examples: A continuous mode design with $V_{IN} = 12V$, $V_{OUT} = -5V$, $I_{OUT} = 1A$, $V_{OUT}' = 5.5V$, and $V_{IN}' = 10V$.

$$I_{RMS} = (1)\sqrt{\frac{5.5}{10}} = 0.74\text{A RMS} \qquad (52)$$

Now change to a discontinuous design with the same conditions and L = 5µH, f = 100kHz.

$$m = \frac{1}{10}\sqrt{(2)\left(10\times10^{-6}\right)(105)(1)(5.5)} = 0.33 \qquad (53)$$

$$I_{RMS} = \frac{(1)(5.5)}{10}\sqrt{\frac{1.35(1-0.165)^3}{0.33} + 0.17(0.33)^2 + 1 - 0.33}$$

$$= 0.96\text{A RMS}$$

Notice that discontinuous mode saves on inductor size, but may require a a larger input capacitor to handle the ripple current increase. The 30% increases in ripple current generates 70% more heating in the capacitor ESR.

Output Capacitor

The inductor on a positive to negative converter does not operate as a filter. It simply acts as an energy storage device so that energy can be transferred from input to output. Therefore, all filtering is done by the output capacitor, and it must have adequate ripple current rating and low ESR. Output ripple voltage for continuous mode will contain three distinct components; a "spike" on switch transitions which is equal to the rate of rise/fall of switch current multiplied by the effective series inductance (ESL) of the output capacitor, a square wave proportional to load current and capacitor ESR, and a triangular component dependent on inductor value and ESR. The spikes are very narrow, typically less than 100ns, and often "disappear" in the parasitic filter created by the inductance of PC board traces between the converter and load combined with the load bypass capacitors. One must be extremely careful when looking at these spikes with an oscilloscope. The magnetic fields created by currents transitions in converter wiring will generate "spikes" on the screen even when they do not exist at the converter output. See the "Oscilloscope Techniques" section for details.

The peak-to-peak sum of square wave and triangular output ripple voltage is

Vp – p = (54)

$$\text{ESR}\left[\frac{I_{OUT}(V_{IN}' + V_{OUT}')}{V_{IN}'} + \frac{(V_{OUT}')(V_{IN}')}{2(V_{OUT} + V_{IN})(f)(L)}\right]$$

(Use Minimum V_{IN}')

Example: $V_{IN} = 5V$, $V_{OUT} = -5V$, $L = 25\mu H$, $I_{OUT(MAX)} = 1A$, f = 100kHz. Assume $V_{IN}' = 2.8V$, $V_{OUT}' = 5.5V$, and ESR = 0.05Ω.

Vp – p = (55)

$$0.05\left[\frac{(1)(2.8+5.5)}{2.8} + \frac{(5.5)(2.8)}{2(5.5+2.8)\left(10^5\right)\left(25\times10^{-6}\right)}\right]$$

$$= 172\text{mV}$$

For some applications this rather high ripple voltage may be acceptable, but more commonly it will be necessary to reduce ripple voltage to 50mV or less. This may be impractical to achieve simply by reducing ESR, so an output filter (L2, C4) is shown, The filter components are relatively small and low cost, both of which are additionally offset by possible reduction in the size of the main output capacitor C1. See the "Output Filters" section for details.

C1 must be chosen for ripple current as well as ESR. Ripple current into the output capacitor is given by;

Continuous Mode (56)

$$I_{RMS} = I_{OUT}\sqrt{\frac{V_{OUT}'}{V_{IN}'}}$$

Discontinuous Mode (57)

$$I_{RMS} =$$

$$I_{OUT}\sqrt{\frac{0.67\left(I_P - I_{OUT}\right)^3}{I_{OUT}\left(I_P\right)^2} + \frac{0.67\left(I_{OUT}\right)^2}{\left(I_P\right)^2} + 1 - \frac{2I_{OUT}}{I_P}}$$

Where I_P = Peak Inductor Current

$$= \sqrt{\frac{2I_{OUT}\left(V_{OUT}'\right)}{L \bullet f}}$$

For the Continuous Mode example

$$I_{RMS} = (1A)\sqrt{\frac{5.5}{2.8}} = 1.4A\ RMS \qquad (58)$$

With Discontinuous Mode using a 3μA inductor, with $I_{OUT} = 0.5A$

$$I_P = \sqrt{\frac{(2)(0.5)(5.5)}{\left(3 \times 10^{-6}\right)\left(10^5\right)}} = 4.28A \qquad (59)$$

$$I_{RMS} =$$

$$(0.5)\sqrt{\frac{(0.67)(4.28 - 0.5)^3}{(0.5)(4.28)^2} + \frac{(0.67)(0.5)^2}{(4.28)^2} + 1 - \frac{2(0.5)}{4.28}}$$

$$= 1.09A\ RMS$$

Notice that output capacitor ripple current is over twice the DC output current in this discontinuous example. The smaller inductor size obtained by discontinuous mode may be somewhat offset by the larger capacitors required on input and output to meet ripple current conditions.

Efficiency

Efficiency for this positive to negative converter can be quite high for larger input and output voltages (>90%), but can be much lower for low input voltages. Losses are summarized below for a continuous mode design. Discontinuous losses are much more difficult to express analytically, but will typically be 1.2 to 1.3 times higher than in continuous mode.

Conduction loss in switch = P_{SW} (DC)

$$P_{SW}(DC) = \qquad (60)$$

$$\frac{\left(I_{OUT}\right)\left(V_{OUT}'\right)}{V_{IN}'}\left[1.8V + \frac{(0.1)\left(I_{OUT}\right)\left(V_{OUT}' + V_{IN}'\right)}{V_{IN}'}\right]$$

Transient switch loss = P_{SW} (AC)

$$P_{SW}(AC) = \frac{I_{OUT}\left(V_{OUT}' + V_{IN}'\right)^2 2\left(t_{SW}\right)(f)}{V_{IN}'} \qquad (61)$$

Where t_{SW} = 50ns + 3ns $(V_{OUT}' + V_{IN}')/V_{IN}'$. The LT1074 quiescent current generates a loss called P_{SUPPLY}

$$P_{SUPPLY} = \left(V_{IN}' + V_{OUT}'\right)\left[\frac{7mA + 5mA\left(V_{OUT}'\right)}{\left(V_{OUT}' + V_{IN}'\right)}\right] \qquad (62)$$

Catch diode loss = $P_{DI} = (I_{OUT})(V_f)$

Where V_f = Forward Voltage of D1 at a current equal to;

$I_{OUT}(V_{OUT}' + V_{IN}')/V_{IN}'$

Capacitor losses can be found by calculating RMS ripple current and multiplying by capacitor ESR. Inductor losses are the sum of copper (wire) loss and core loss

$$P_{L1} = R_L\left[\frac{\left(I_{OUT}\right)\left(V_{OUT}' + V_{IN}'\right)}{V_{IN}'}\right]^2 + P_{CORE} \qquad (63)$$

R_L = Inductor Copper Resistance

P_{CORE} can be calculated if the inductor core material is known. See the "Inductor Selection" section.

Example: V_{IN} = 12V, V_{OUT} = –12V, I_{OUT} = 1.5A, f = 100kHz. Let L1= 50μH, with R_L = 0.04Ω. Assume ESR of input and output capacitor is 0.05Ω. V_{IN}' = 12V – 2V = 10V, V_{OUT}' = 12V + 0.5V = 12.5V.

$$P_{SW}\,(DC) = \tag{64}$$

$$\frac{(1.5)(12.5)}{10}\left[1.8+\frac{(0.1)(1.5)(12.5+10)}{10}\right]=4W$$

$$P_{SW}\,(AC) =$$

$$\frac{(1.5)(12.5+10.5)^2}{10}\left[2\,(50ns+3ns)\,\frac{(12.5+10)}{10}\right]\left(10^5\right)$$

$$=0.86W$$

$$P_{SUPPLY}=(12+12)\left[7mA+\frac{5mA(12.5)}{12.5+10}\right]=0.23W$$

$$P_{DI}=(1.5)(0.5)=0.75W$$

$$I_{RMS(INPUT\,CAP)}=1.5\sqrt{\frac{12.5}{10}}=1.68A\ RMS$$

$$P_{C3}=(1.68)^2\,(0.05)=0.14W$$

$$I_{RMS(OUTPUT\,CAP)}=$$

$$I_{OUT}\sqrt{\frac{(12.5)^2+(12.5)(10)}{(10)(12.5+10)}}=1.68A\ RMS$$

$$P_{C1}=(1.68)^2\,(0.05)=0.14W$$

$$P_{L1}=0.04\left[\frac{(1.5)(12.5+10)}{10}\right]^2=0.46W$$

$$\text{Assume } P_{CORE}=0.2W$$

$$\text{Efficiency}=\frac{I_{OUT}\,V_{OUT}}{I_{OUT}\,V_{OUT}+\Sigma P_{LOSS}}$$

$$\Sigma P_{LOSS}=4+0.86+0.23+0.75+0.14+0.14+0.46+0.2=6.78W$$

$$\text{Efficiency}=\frac{(1.5)(12)}{(1.5)(12)+6.78}=73\%$$

NEGATIVE BOOST CONVERTER

Note: *All equations in this section use the absolute value of V_{IN} and V_{OUT}.*

The LT1074 can be configured as a negative boost converter (Figure 18) by tying the ground pin to the negative output. This allows the regulator to operate from input voltages as low as 4.75V if the regulated output is at least 8V. R1 and R2 set the output voltage as in a conventional connection, with R1 selected from

$$R1=\frac{V_{OUT}\bullet R2}{V_{REF}}-R2 \tag{65}$$

Boost converters have a "right half plane zero" in the forward part of the signal path and for this reason, L1 is kept to a low value to maximize the "zero" frequency. With larger values for L1, it becomes difficult to stabilize the regulator, especially at low input voltages. If V_{IN} >10V, L1 can be increased to 50μH.

There are two important characteristics of boost converters to keep in mind. First, the input voltage cannot exceed the output voltage, or D1 will simply pull the output unregulated high. Second, the output cannot be pulled below the input, or D1 will drag down the input supply. For this reason, boost converters are not normally considered short circuit protected unless some form of fusing is provided. Even with fuses, there is the possibility of damage to D1 if the input supply can deliver very large surge currents.

Boost converters require switch currents which can be much greater than output load current. Peak switch current is given by

$$I_{SW(PEAK)}=\frac{I_{OUT}\bullet V_{OUT}'}{V_{IN}'}+\frac{V_{IN}'\left(V_{OUT}'-V_{IN}'\right)}{2L\bullet f\bullet V_{OUT}'} \tag{66}$$

For the circuit in Figure 18, with V_{IN} = 5V, (V_{IN}' ≈3V), V_{OUT}' ≈15.5V, with an output load of 0.5A;

$$I_{SW\,(PEAK)}= \tag{67}$$

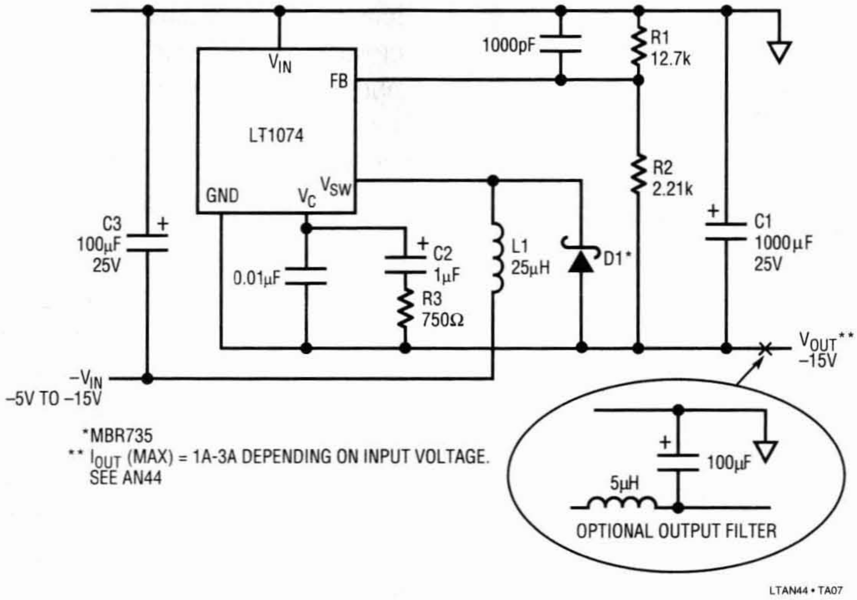
$$\frac{(0.5A)(15.5)}{3}+\frac{3\,(15.5-3)}{2\,(25\mu H)\left(10^5\right)(15.5)}=3.07A$$

This formula can be rearranged to yield maximum load current for a given maximum switch current (I_M)

$$I_{OUT(MAX)}=\frac{I_M\bullet V_{IN}'}{V_{OUT}'}-\left(\frac{V_{IN}'}{V_{OUT}'}\right)^2\frac{V_{OUT}'-V_{IN}'}{2L\bullet f} \tag{68}$$

For I_M = 5.5A, this equation yields 0.82A with V_{IN} = 4.5V, 1.8A with V_{IN} = 8V, and 3.1A for V_{IN} = 12V.

The explanation for switch current which is much higher than output current is that current is delivered to the output only during switch "off" time. With low input voltages, the switch is "on" a high percentage of the total switching cycle and current is delivered to the output only a small percent of the time. Switch duty cycle is given by



*MBR735
** I_{OUT} (MAX) = 1A-3A DEPENDING ON INPUT VOLTAGE. SEE AN44

Figure 18. Negative Boost Converter

$$DC = \frac{V_{OUT}' - V_{IN}'}{V_{OUT}'} \tag{69}$$

For $V_{IN} = 5V$, $V_{OUT} = 15V$, $V_{IN}' \approx 3V$, $V_{OUT}' = 15.5V$ and;

$$DC = \frac{15.5 - 3}{15.5} = 81\% \tag{70}$$

Peak inductor current is equal to peak switch current. Average inductor current in continuous mode is equal to

$$I_{L(AVG)} = \frac{I_{OUT} \bullet V_{OUT}'}{V_{IN}'} \tag{71}$$

A 0.5A load requires 2.6A inductor current for $V_{IN} = 5V$.

Along with high switch currents, keep in mind that boost converters draw DC input currents *higher* than the output load current. Average input current to the converter is

$$I_{IN}(DC) \approx \frac{(I_{OUT})(V_{OUT}')}{V_{IN}'} \tag{72}$$

With $I_{OUT} = 0.5A$, and $V_{IN} = 5V$ ($V_{IN}' \approx 3V$)

$$I_{IN}(DC) = \frac{(0.5)(15.5)}{3} = 2.6A \tag{73}$$

This formula does not take into account secondary loss terms such as the inductor, output capacitor, etc., so it is somewhat optimistic. Actual input current may be closer to 3A. *Be sure the input supply is capable of providing the required boost converter input current.*

Output Diode

The *average* current through D1 is equal to output current, but the peak pulse current is equal to peak switch current, which can be many times output current. D1 should be conservatively rated at 2 to 3 times output current.

Output Capacitor

The output capacitor of a boost converter has high RMS ripple current so this is often the deciding factor in the selection of C1. RMS ripple current is approximately

$$I_{RMS(C1)} \approx I_{OUT} \sqrt{\frac{V_{OUT}' - V_{IN}'}{V_{IN}'}} \tag{74}$$

For $I_{OUT} = 0.5A$, $V_{IN} = 5V$

$$I_{RMS} \approx 0.5 \sqrt{\frac{15.5 - 3}{3}} = 1A\ RMS \tag{75}$$

C1 must have a ripple current rating of 1A RMS. Its actual capacitance value is not critical. ESR of the capacitor will determine output ripple voltage.

Output Ripple

Boost converters tend to have high output ripple because of the high pulse currents delivered to the output capacitor.

$$V_{p-p} = ESR\left[\frac{I_{OUT} \bullet V_{OUT}'}{V_{IN}'} + \frac{V_{IN}'\left(V_{OUT}' - V_{IN}'\right)}{2L \bullet f \bullet V_{OUT}'}\right] \quad (76)$$

This formula assumes continuous mode operation, and it ignores the inductance of C1. In actual operation, C1 inductance will allow output "spikes" which should be removed with an output filter. The filter can be as simple as several inches of output wire or trace and a small solid tantalum capacitor if only the spikes need to be removed. A filter inductor is required if significant reduction of the fundamental is needed. See the "Output Filter" section.

For the circuit in Figure 18, with $I_{OUT} = 0.5A$, $V_{IN} = 5V$; and an output capacitor ESR of 0.05Ω

$$V_{p-p} = \quad (77)$$

$$0.05\left[\frac{(0.5)(15.5)}{3} + \frac{3(15.5-3)}{2\left(25\times10^{-6}\right)\left(10^{5}\right)(15.5)}\right] = 153\text{mV}$$

Input Capacitor

Boost converters are more benign with respect to input current pulsing than buck or inverting converters. The input current is a DC level with a triangular ripple superimposed. RMS value of input current ripple is

$$I_{RMS(C3)} \approx \frac{V_{IN}'\left(V_{OUT}' - V_{IN}'\right)}{3L \bullet f \bullet V_{OUT}'} \quad (78)$$

Notice that ripple current is independent of load current assuming that load current is high enough to keep the converter in continuous mode. For the converter in Figure 18, with $V_{IN} = 5V$

$$I_{RMS} = \frac{3(15.5-3)}{3\left(25\times10^{-6}\right)\left(10^{5}\right)(15.5)} = 0.32\text{A RMS} \quad (79)$$

C3 may be chosen on a ripple current basis to minimize size. Larger values will allow less conducted EMI back into the input supply.

INDUCTOR SELECTION

There are five main criteria in selecting an inductor for switching regulators. First, and most important, is the actual inductance value. If inductance is too low, output power will be restricted. Too much inductance results in large physical size and poor transient response. Second, the inductor must be capable of handling both RMS and peak currents which may be significantly higher than load current. Peak currents are limited by core saturation, with resultant loss of inductance. RMS currents are limited by heating effects in the winding. Also important is peak-to-peak current which determines heating effects in the core itself. Third, the physical size or weight of the inductor may be important in many applications. Fourth, power losses in the inductor can significantly affect regulator efficiency, especially at higher switching frequencies. Last, the price of inductors is very dependent on particular construction techniques and core materials, which impact overall size, efficiency, mountability, EMI, and form factor. There may be a significant cost penalty, for instance, if more expensive core materials are needed in "minimum size" applications.

The issues of price and size become particularly complicated at higher frequencies. High frequencies are used to reduce component size, and indeed, the inductance values required scale inversely with frequency. The problem with a scaled-down high frequency inductor is that total core loss increases slightly with frequency for constant ripple current, and this power is now dissipated in a smaller core, so temperature rise *and* efficiency can limit size reductions. Also, the smaller core has less room for wire, so wire losses may increase. The only solution to this problem is to find a better core material. Common low cost inductors use powdered iron cores, which are very low cost. These cores exhibit modest losses at 40kHz with a typical flux density of 300 gauss. At 100kHz, core losses can become unacceptably high at these flux densities. Reducing flux density requires a larger core, canceling part of the advantage gained in reducing inductance at the higher frequency.

Molypermalloy, "high flux," "Kool Mμ" (Magnetics, Inc.), and ferrite cores have considerably lower core loss, and can be used at 100kHz and above with higher flux density, but these cores are expensive. The basic lesson here is that attention to inductor selection is very important to minimize costs and achieve desired goals of size and efficiency.

A special equation has been developed in the following section which shows that for a given core material, total core loss is dependent almost totally on *frequency* and *inductance value*, not physical size or shape. The formula is arranged to solve for the inductance required to achieve a given core loss. It shows that, in a typical 100kHz buck converter, inductance has to be increased by a factor of three over the minimum required, if a low cost powdered iron core is used.

"Standard" switching regulator inductors are toroids. Although this shape is hardest to wind, it offers excellent utilization of the core, and more importantly, has low EMI fringing fields. Rod or drum shaped inductors have very high fringing fields and are not recommended except possibly for secondary output filters. Inductors made with "E-E" or "E-C" split cores are easy to wind on the separate bobbin, but tend to be much taller than toroids and more expensive. "Pot" cores reverse the position of winding and core—the core surrounds the winding. These cores offer the best EMI shielding, but tend to be bulky and more expensive. Also, temperature rise is higher because of the enclosed winding. Special low profile split cores (TDK "EPC," etc.) are now offered in a wide range of sizes. Although not as efficient as EC cores in terms of watts/volume, these cores are attractive for restricted height applications.

The best way to select an inductor is to first calculate the limitations on its minimum value. These limitations are imposed by a maximum allowed switch current, maximum allowable efficiency loss, and the necessity to operate in continuous versus discontinuous mode. (See discussion elsewhere of the consequences related to these two modes.) After the minimum value has been established, calculations are done to establish the operating conditions of the inductor; i.e., RMS current, peak-to-peak ripple current, and peak current. With this information, next select an "off the shelf" inductor which meets all the calculated requirements, or is reasonably close, Then ascertain the physical size and price of the selected inductor. If it fits in the allowed "budget" of space, height, and cost, you can then give some consideration to increasing the inductance to gain better efficiency, lower output ripple, lower input ripple, more output power, or some combination of these. If the selected inductor is physically too large, there are several possibilities; select a different core shape, a different core material, (which will require recalculating the minimum inductance based on efficiency loss), a higher operating frequency, or consider a custom wound inductor which is optimized for the application. Keep in mind when attempting to shoehorn an inductor into the smallest possible space that output overload conditions may cause currents to increase to the point of inductor failure. The major failure mode to consider is winding insulation failure due to high winding temperature. IC failure caused by loss of inductance due to core saturation or core temperature is not usually a problem because the LT1074 has pulse-by-pulse current limiting which is effective even with drastically lowered inductance.

The following equations solve for minimum inductance based on the assumption of limited peak switch current (I_M).

Minimum Inductance to Achieve a Required Output Power

Buck Mode Discontinuous, $I_{OUT} \le \frac{I_M}{2}$, Use Maximum V_{IN} (80)

$$L_{MIN} = \frac{2 \bullet I_{OUT} \bullet V_{OUT}\left(V_{IN}' - V_{OUT}\right)}{f\left(I_M\right)^2\left(V_{IN}'\right)}$$

Buck Mode Continuous, $I_{OUT} \le I_M$, Use Maximum V_{IN} (81)

$$L_{MIN} = \frac{V_{OUT}\left(V_{IN}' - V_{OUT}\right)}{2 \bullet f \bullet V_{IN}'\left(I_M - I_{OUT}\right)}$$

Inverting Mode Discontinuous, $I_{OUT} \le \frac{I_M \bullet V_{IN}'}{2\left(V_{IN}' + V_{OUT}'\right)}$ (82)

$$L_{MIN} = \frac{2 \bullet I_{OUT} \bullet V_{OUT}'}{\left(I_M\right)^2 \bullet f}$$

Inverting Mode Continuous, $I_{OUT} \le \frac{I_M \bullet V_{IN}'}{\left(V_{IN}' + V_{OUT}'\right)}$ (83)

$$L_{MIN} = \frac{\left(V_{IN}'\right)^2 \bullet V_{OUT}'}{2 \bullet f\left(V_{OUT}' + V_{IN}'\right)^2\left(\frac{I_M \bullet V_{IN}'}{V_{IN}' + V_{OUT}'} - I_{OUT}\right)}$$

Boost Mode Discontinuous, $I_{OUT} \le \frac{I_M \bullet V_{IN}'}{2 \bullet V_{OUT}'}$ (84)

$$L_{MIN} = \frac{2 \bullet I_{OUT}\left(V_{OUT}' - V_{IN}'\right)}{\left(I_M\right)^2 \bullet f}$$

$$\text{Boost Mode Continuous, } I_{OUT} \le \frac{I_M \bullet V_{IN}'}{V_{OUT}'} \qquad (85)$$

$$L_{MIN} = \frac{(V_{IN}')^2 (V_{OUT}' - V_{IN}')}{2 \bullet f (V_{OUT}')^2 \left(\frac{I_M \bullet V_{IN}'}{V_{OUT}'} - I_{OUT} \right)}$$

$$\text{Tapped Inductor Continuous, } I_{OUT} \le \frac{I_M (N+1)(V_{IN}')}{V_{IN}' + N V_{OUT}'} \qquad (86)$$

$$L_{MIN} = \frac{V_{IN} \bullet V_{OUT} (V_{IN} - V_{OUT})(N+1)^2}{I_M \bullet 2f \bullet V_{IN}(N+1)(V_{IN} + N V_{OUT}) - I_{OUT}(V_{IN} + N V_{OUT})^2 (2f)}$$

Minimum Inductance Required to Achieve a Desired Core Loss

Power loss in inductor core material is not intuitive at all. It is, to a first approximation, independent of the *size* of the core for a given inductance and operating frequency. Second, power loss *drops* as inductance increases, for constant frequency. Last, raising frequency with a given inductor will *decrease* core loss, even though manufacturer's curves show that core loss increases with frequency. These curves assume constant flux density, which is not true for a fixed inductance.

The general formula for core loss can be expressed as;

$$P_C = C \bullet B_{AC}^p \bullet f^d \bullet V_C \qquad (87)$$

C, d, p = Constants (see Table 1)
B_{AC} = Peak AC Flux Density (1/2 peak-to-peak) (gauss)
f = Frequency
V_C = Core Volume (cm^3)

The exponent "p" falls in the range of 1.8-2.4 for powdered iron cores, ≈2.1 for molypermalloy, and 2.3-2.8 for ferrites. "d" is ≈1 for powdered iron and ≈1.3 for ferrite. A closed form expression can be generated which relates core loss to the basic requirements of a switching regulator; inductance, frequency, and input/output voltages. The general form is

$$\text{Continuous Mode } P_C = \frac{a \bullet b^p}{f^{p-d} \bullet L^{p/2}} \qquad (88)$$

$$\text{Discontinuous Mode } P_C = a \bullet f^{d-1} \bullet e \qquad (89)$$

a, d, p = Core Material Constants (see Table 1)
b, e = Constants Determined by Input and Output Voltages and Currents
L = Inductance

These formulas show that core material, inductance, and frequency are the only degrees of freedom to alter core loss in the continuous mode case. For discontinuous mode, even inductance disappears as a variable, leaving frequency and core material. Further, the constant "d" is close to unity for many core materials, yielding a discontinuous mode core loss independent of all user variables except core material!

The following specific formulas will allow calculation of the inductance to achieve a given core loss in continuous mode and will indicate actual core loss for the discontinuous mode.

When using these formulas, assume initially that the term $V_e^{p-2/p}$ can be ignored. It is close to unity for a relatively wide range of core volumes because the exponent (p–2)/2 is less than 0.1 for commonly used powdered iron and molypermalloy cores. After an inductor is chosen and V_e is known, the term $V_e^{p-2/p}$ can be calculated to double check its effect on the value for L_{MIN}, usually less than 20%.

Continuous Mode (90)

$$L_{MIN}^* = \frac{a \bullet \mu_e \bullet V_L^2}{(P_C)^{2/p} \bullet f^{\left(2 - \frac{2d}{p}\right)} \bullet V_e^{\left(\frac{p-2}{p}\right)}}$$

Buck Mode Discontinuous (91)

$$P_C = \frac{a \bullet \mu_e (0.4\pi) f^{d-1}}{10^{-8}} (V_L \bullet I_{OUT})$$

*A strict derivation

a, d, p = Core loss constants. Use Table 1.
μ_e = Effective core permeability. For ungapped cores, use Table 1. For gapped cores, use manufacturer's specification, or calculate.
V_L = An equivalent "voltage," dependent on input voltage, output voltage, and topology. Use Table 2.
P_C = Total core loss in watts.
L = Inductance.
V_e = Effective core volume in cm^3.

Table 1. Core Constants

		C	a	d	p	μ	Loss at 100kHz, 500 Gauss (mW/cm3)
Micrometals							
Powdered Iron	# 8	4.30E-10	8.20E-05	1.13	2.41	35	617
	# 18	6.40E-10	1.20E-04	1.18	2.27	55	670
	# 26	7.00E-10	1.30E-04	1.36	2.03	75	1300
	# 52	9.10E-10	4.90E-04	1.26	2.11	75	890
Magnetics							
Kool Mμ	60	2.50E-11	3.20E-06	1.5	2	60	200
	75	2.50E-11	3.20E-06	1.5	2	75	200
	90	2.50E-11	3.20E-06	1.5	2	90	200
	125	2.50E-11	3.20E-06	1.5	2	125	200
Molypermalloy	– 60	7.00E-12	2.90E-05	1.41	2.24	60	87
	– 125	1.80E-11	1.60E-04	1.33	2.31	125	136
	– 200	3.20E-12	2.80E-05	1.58	2.29	200	390
	– 300	3.70E-12	2.10E-05	1.58	2.26	300	368
	– 550	4.30E-12	8.50E-05	1.59	2.36	550	890
High Flux	– 14	1.10E-10	6.50E-03	1.26	2.52	14	1330
	– 26	5.40E-11	4.90E-03	1.25	2.55	26	740
	– 60	2.60E-11	3.10E-03	1.23	2.56	60	290
	– 125	1.10E-11	2.10E-03	1.33	2.59	125	460
	– 160	3.70E-12	6.70E-04	1.41	2.56	160	1280
Ferrite	F	1.80E-14	1.20E-05	1.62	2.57	3000	20
	K	2.20E-18	5.90E-06	2	3.1	1500	5
	P	2.90E-17	4.20E-07	2.06	2.7	2500	11
	R	1.10E-16	4.80E-07	1.98	2.63	2300	11
Philips							
Ferrite	3C80	6.40E-12	7.30E-05	1.3	2.32	2000	37
	3C81	6.80E-14	1.50E-05	1.6	2.5	2700	38
	3C85	2.20E-14	8.70E-08	1.8	2.2	2000	18
	3F3	1.30E-16	9.80E-08	2	2.5	1800	7
TDK							
Ferrite	PC30	2.20E-14	1.70E-06	1.7	2.4	2500	21
	PC40	4.50E-14	1.10E-05	1.55	2.5	2300	14
Fair-Rite	77	1.70E-12	1.80E-05	1.5	2.3	1500	86

Table 2. Equivalent Inductor Voltage

TOPOLOGY	V_L
Buck Continuous	$V_{OUT}(V_{IN} - V_{OUT})/2V_{IN}$
Buck Discontinuous	
Inverting Continuous	$V_{IN}' \cdot V_{OUT}'/[2(V_{IN}' + V_{OUT}')]$
Inverting Discontinuous	
Boost Continuous	$V_{IN}'(V_{OUT}' - V_{IN}')/2V_{OUT}'$
Boost Discontinuous	
Tapped-inductor	$(V_{IN} - V_{OUT})(V_{OUT})(1 + N)/2(V_{IN} + NV_{OUT})$

Example: Buck converter with $V_{IN} = 20V\text{-}30V$, $V_{OUT} = 5V$, $I_{OUT} = 3A$, f = 100kHz, maximum inductor loss = 0.8W.

3A is more than $I_M/2$, so continuous mode must be used. Maximum input voltage is used to calculate L_{MIN} from equation 81

$$L_{MIN} = \frac{5(30-5)}{2\left(10^5\right)(30)(5-3)} = 10.4\mu H \qquad (92)$$

Now calculate minimum inductance to achieve desired core loss. Assume 1/2 total inductor loss in winding and 1/2 loss in the core ($P_C = 0.4W$). Try Micrometals #26 core material. V_L (from Table 2) = 5(30 – 5)/(2 • 30) = 2.08

$$L_{MIN} = \frac{\left(1.3 \times 10^{-4}\right)\left(75\right)\left(2.08\right)^2}{\left(0.4\right)^{0.985} \bullet \left(10^5\right)^{2-1.34}} = 52\mu H \qquad (93)$$

The inductance must be five times the minimum to achieve desired core loss. Let's assume that 52µH is too large for our space requirements and try a better core material, #52, which is only slightly more expensive.

$$L_{MIN} = \frac{\left(4.9 \times 10^{-4}\right)\left(75\right)\left(2.08\right)^2}{\left(0.4\right)^{\frac{2}{2.11}} \bullet \left(10^5\right)^{\frac{2-2(1.26)}{2.11}}} = 35\mu H \qquad (94)$$

To see if an off-the-shelf inductor is suitable, calculate inductor currents and V • t product using Table 3.

$$I_{RMS} = I_{OUT} = 3A \qquad (95)$$

$$I_P = 3 + \frac{5\left(30-5\right)}{2\left(35 \times 10^{-6}\right)\left(10^5\right)\left(30\right)} = 3.6A$$

$$V \bullet t = \frac{5\left(30-5\right)}{\left(10^5\right)\left(30\right)} = 42V \bullet \mu s$$

Table 3. Inductor Operating Conditions

	I_{AVG}	I_{PEAK}	Ip-p	V•µs
Buck Converter (Continuous)	I_O	$I_O + \frac{V_O(V_I - V_O)}{2 \bullet L \bullet f \bullet V_I}$	$\frac{V_O(V_I - V_O)}{L \bullet f \bullet V_I}$	$\frac{V_O(V_I - V_O) \bullet 10^6}{f \bullet V_I}$
Positive to Negative (Continuous)	$\frac{I_O(V_I + V_O)}{V_I}$	$\frac{I_O(V_O + V_I)}{V_I} + \frac{V_I \bullet V_O}{2 \bullet L \bullet f(V_I + V_O)}$	$\frac{V_I \bullet V_O}{L \bullet f(V_I + V_O)}$	$\frac{V_I \bullet V_O \bullet 10^6}{f(V_I + V_O)}$
Negative Boost (Continuous)	$\frac{I_O \bullet V_O}{V_I}$	$\frac{I_O \bullet V_O}{V_I} + \frac{V_I(V_O - V_I)}{2L \bullet f \bullet V_O}$	$\frac{V_I(V_O - V_I)}{L \bullet f \bullet V_O}$	$\frac{V_I(V_O - V_I) \bullet 10^6}{f \bullet V_O}$
Tapped-Inductor*	$\frac{I_O(N \bullet V_O + V_I)}{V_I(1+N)}, \frac{I_O(N \bullet V_O + V_I)}{V_I}*$	$\frac{I_O(N \bullet V_O + V_I)}{V_I(1+N)} + \frac{(V_I - V_O)(1+N)(V_O)}{2L \bullet f(N \bullet V_O + V_I)}*$	$\frac{(V_I - V_O)(1+N)(V_O)}{L \bullet f(N \bullet V_O + V_I)}*$	$\frac{10^6(V_I - V_O)(1+N)(V_O)}{f(N \bullet V_O + V_I)}$
Buck Converter (Discontinuous)	$1/4\sqrt{\frac{(I_O)^3 \bullet V_O(V_I - V_O)}{f \bullet L \bullet V_I}}$	$\sqrt{\frac{2I_O \bullet V_O(V_I - V_O)}{L \bullet f \bullet V_I}}$		$10^6\sqrt{\frac{2 \bullet L \bullet I_O \bullet V_O(V_I - V_O)}{f \bullet V_I}}$
Positive to Negative (Discontinuous)	$1/4\sqrt{\frac{I_O^3(V_I + V_O)^2}{V_I \bullet f \bullet L}}$	$\sqrt{\frac{2I_O \bullet V_O}{f \bullet L}}$		$10^6\sqrt{\frac{2I_O \bullet V_O \bullet L}{f}}$
Negative Boost (Discontinuous)	$1/4\sqrt{\frac{I_O^3 \bullet V_O^2(V_O + V_I)}{V_I^2 \bullet L \bullet f}}$	$\sqrt{\frac{2I_O(V_O - V_I)}{L \bullet f}}$		$10^6\sqrt{\frac{2I_O \bullet L(V_O - V_I)}{L \bullet f}}$

* Values given for tapped-inductor I_{AVG} are average current through entire inductor during switch "on" time (first term), and average current through output section during switch "off" time (second term). To calculate heating, these currents must be multiplied by the appropriate winding resistance and factored by duty cycle.

I_{PEAK} is used to ensure the core does not saturate and should be used with the entire inductance.

Peak-to-peak current is used with the entire inductance to calculate core heating losses. It is the equivalent value if the inductor is not tapped.

This inductor must be at least 35μH, rated at 3A and ≥ 42V • μs @ 100kHz. It must not saturate at a peak current of 3.6A.

Example: Inverting mode with V_{IN} = 4.7-5.3V, V_{OUT} = –5V, I_{OUT} = 1A, f = 100kHz, maximum inductor loss = 0.3W. Let V_{IN}' = 2.7V, V_{OUT}' = 5.5V. Maximum output current for discontinuous mode (equation 82) is 0.82A, so use continuous mode.

$$L_{MIN} = \tag{96}$$

$$\frac{(2.7)^2(5.5)}{2\times10^5(5.5+2.7)^2\left(\frac{5\bullet2.7}{5.5+2.7}-1\right)} = 4.6\mu H$$

Now calculate minimum inductance from core loss. Assume core loss is 1/2 of total inductor loss, (P_C = 0.15W).

$$V_L(\text{From Table 2}) = \frac{(2.7)(5.5)}{2(2.7+5.5)} = 0.905 \tag{97}$$

Assuming Micrometals type #26 material,

$$L_{MIN} = \frac{\left(1.3\times10^{-4}\right)(75)(0.905)^2}{(0.15)^{\frac{2}{2.03}}\bullet\left(10^5\right)^{2-\frac{2.72}{2.03}}} = 26\mu H \tag{98}$$

This value is over five times the minimum of 4.6μH Perhaps a higher core loss is acceptable. Here's how to do a quick check. If we assume total efficiency is ≈60% (+ to – conversion with a 5V input is inefficient due to switch loss), then input power is equal to output power divided by 0.6 = 8.33W. If we double core loss from 0.15W to 0.3W, efficiency will be 5W/(8.33 + 0.15) = 59%. This is only a 1% drop in efficiency. A core loss of 0.3W allows inductance to drop to 12μH, assuming that the 12μH inductor will tolerate the core loss plus winding loss without overheating. Inductor currents are

$$I_{RMS}(\text{From Table 3}) = \frac{(1A)(2.7+5.5)}{2.7} = 3A \tag{99}$$

$$I_P =$$

$$\frac{(1A)(2.7+5.5)}{2.7} + \frac{(2.7)(5.5)}{2\left(12\times10^{-6}\right)\left(10^5\right)(2.7+5.5)} = 3.8A$$

$$V\bullet t = \frac{(2.7)(5.5)}{\left(10^5\right)(2.7+5.5)} = 18\ V\bullet\mu s\ @\ 100kHz$$

MICROPOWER SHUTDOWN

The LT1074 will go into a micropower shutdown mode, with I_{SUPPLY} ≈ 150μA, when the shutdown pin is held below 0.3V. This can be accomplished with an open collector TTL gate, a CMOS gate, or a discrete NPN or NMOS device, as shown in Figure 19.

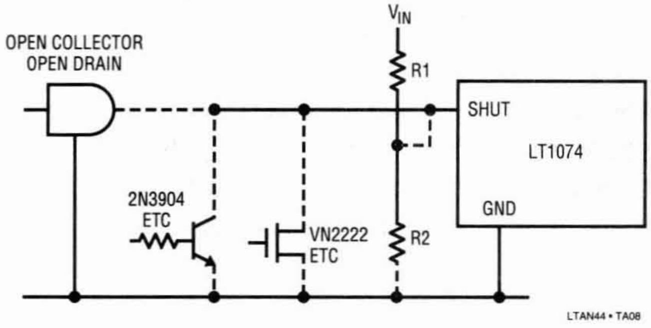


Figure 19. Shutdown

The basic requirement is that the pull down device can sink 50μA of current at a worst case threshold of 0.1V. This requirement is easily met with any open collector TTL gate (not Schottky clamped), a CMOS gate, or discrete device.

The sink requirements are more stringent if R1 and R2 are added for under voltage lockout. Sink capability must be 50μA + V_{IN}/R1 at the worst case threshold of 0.1V. The suggested value for R2 is 5kΩ to minimize the effect of shutdown pin bias current. This sets the current through R1 and R2 at ≈ 500μA at the undervoltage lockout point. At an input voltage of twice the lockout point, R1 current will be slightly over 1mA, so the pull down device must sink this current down to 0.1V. A VN2222 or equivalent is suggested for these conditions.

Start-Up Time Delay

Adding a capacitor to the shutdown pin will generate a delayed start-up. The internal current averages to about 25μA during the delay period, so delay time will be =(2.45V)/(C • 25μA), ±50%. If more accurate time out is required, R1 can be added to swamp out the effects of the internal current, but a larger capacitor is needed, and time out is dependent on input voltage.

Some thought must be given to reset of the timing capacitor. If a resistor to ground is used, it must be large enough to not drastically affect timing, so reset time is typically ten times longer than time delay. A diode to V_{IN}

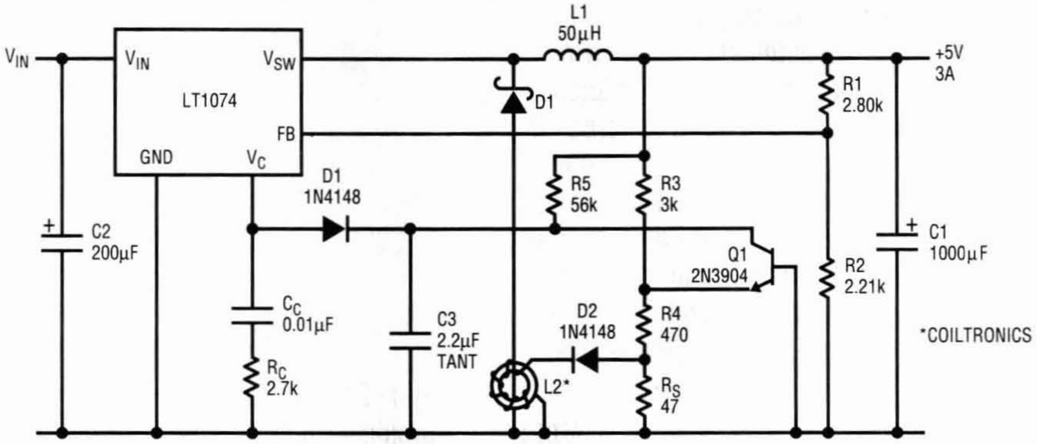


Figure 20. Low Loss External Current Limit

resets quickly, but if V_{IN} does not drop to near zero, time delay will be shortened when power is recycled immediately.

5-PIN CURRENT LIMIT

Sometimes it may be desirable to current limit the 5-pin version of the LT1074. This is particularly helpful where maximum load current is significantly less than the 6.5A internal current limit, and the inductor and/or catch diode are minimum size to save space. Short circuit conditions put maximum stress on these components.

The circuit in Figure 20 uses a small toroidal inductor slipped over one lead of the catch diode to sense diode current. Diode current during switch "off" time is almost directly proportional to output current, and L2 can generate an accurate limit signal without affecting regulator efficiency. Total power lost in the limit circuitry is less than 0.1W.

L2 has 100 turns. It therefore delivers 1/100 times diode current to R_S when D1 conducts. The voltage across R_S required to current limit the LT1074 is equal to the voltage across R4 plus the forward biased emitter base voltage Q1 (≈600mV @25°C). The voltage across R4 is set at 1.1V by R3, which is connected to the output. Current limit is set by selecting R_S;

$$R_S = \frac{R_4 I_X + V_{BE}}{\frac{I_{LIM}}{100} - I_X} \tag{100}$$

$$I_X = \frac{V_{OUT} + V_{BE}}{R_3} + 0.4\text{mA}$$

V_{BE} = Forward biased emitter base voltage of Q1 @ I_C = 500µA (≈600mV).

N = Turns on L2.

I_{LIM} = Desired output current limit. I_{LIM} should be set ≈1.25 times maximum load current to allow for variations in V_{BE} and component tolerances.

The circuit in Figure 20 is intended to supply 3A maximum load current, so I_{LIM} was set at 3.75A. Nominal V_{IN} is 25V, giving

$$I_X = \frac{5 + 0.6}{3000} + 0.4 \times 10^{-3} = 2.27 \times 10^{-3} \tag{101}$$

$$R_S = \frac{(470)\left(2.27 \times 10^{-3}\right) + 0.6}{3.75/100 - 2.27 \times 10^{-3}} = 47\Omega$$

This circuit has "foldback" current limit, meaning that short circuit current is lower than the current limit at full output voltage. This is the result of using the output voltage to generate part of the current limit trip level. Short circuit current will be approximately 45% of peak current limit, minimizing temperature rise in D1.

R5, C3, and D3 allow separate frequency compensation of the current limit loop. D3 is reversed biased during normal operation. For higher output voltages, scale R3 and R5 to provide approximately the same currents.

SOFT START

Soft start is a means for ramping switch currents during the turn on of a switching regulator. The reasons for doing this include surge protection for the input supply, protection of switching elements, and prevention of output overshoot. Linear Technology switching regulators have built-in switch protection that eliminates concern over device failure, but some input supplies may not tolerate the inrush current of a switching regulator. The problem occurs with current limited input supplies or those with relatively high source resistance. These supplies can "latch" in a low voltage state where the current drawn by the switching regulator in much higher than the normal input current. This is shown by the general formula for switching regulator input current and input resistance;

$$I_{IN} = \frac{(V_{OUT})(I_{OUT})}{(V_{IN})(E)} = \frac{P_{OUT}}{(V_{IN})(E)} \qquad (102)$$

$$R_{IN} = \frac{-(V_{IN})^2(E)}{(V_{OUT})(I_{OUT})} = \frac{-(V_{IN})^2(E)}{P_{OUT}} \text{(note negative sign)}$$

E = Efficiency (≈0.7-0.9)

These formulas show that input current is proportional to the reciprocal of input voltage, so that if input voltage drops by 3:1, input current increases by 3:1. An input supply which rises slowly will "see" a much heavier current load during its low voltage state. This can activate current limit in the input supply and "latch" it permanently in a low voltage condition. By instituting a soft start in the switching regulator which is *slower* than the input supply rise time, regulator input current is held low until the input supply has a chance to reach full voltage.

The formula for regulator input resistance shows that it is negative and decreases as the square of input voltage. The maximum allowed positive source resistance to avoid latch-up is given by;

$$R_{SOURCE(MAX)} = \frac{(V_{IN})^2(E)}{4(V_{OUT})(I_{OUT})} \qquad (103)$$

The formula shows that a +12V to –12V converter with 80% efficiency and 1A load must have a source resistance less than 2.4Ω. This may sound like much ado about nothing, because an input supply designed to deliver 1A would not normally have such a high source resistance, but a sudden output load surge or a dip in the source voltage might trigger a permanent overload condition Low V_{IN} and high output load require lower source resistance.

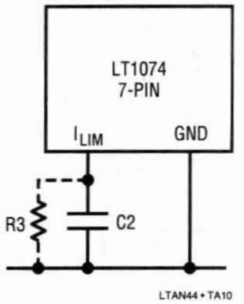


Figure 21. Soft Start Using I_{LIM} Pin

In Figure 21, C2 generates a soft start of switching current by forcing the I_{LIM} pin to ramp up slowly. Current out of the I_{LIM} pin is ≈300μA, so the time for the LT1074 to reach full switch current (V_{LIM} ≈ 5V) is ≈(1.6×10^4)(C). To ensure low switch current until V_{IN} has reached full value, an approximate value for C2 is

$$C2 \approx (10^{-4})(T) \qquad (104)$$

T = Time for input voltage to rise to within 10% of final value.

C2 must be reset to zero volts whenever the input voltage goes low. An internal reset is provided when the shutdown pin is used to generate undervoltage lockout. The "undervoltage" state resets C2. If lockout is not used, R3 should be added to reset C2. For full current limit, R3 should be 30kΩ. If reduced current limit is desired, R3's value is set by desired current limit. See the "Current Limit" section.

If the only reason for adding soft start is to prevent input supply latchup, a better alternative may be undervoltage lockout (UVLO). This prevents the regulator from drawing input current until the input voltage reaches a preset voltage. The advantage of UVLO is that it is a true DC function and cannot be defeated by a slow rising input, short reset times, momentary output shorts, etc.

OUTPUT FILTERS

When converter output ripple voltage must be less than ≈2% of output voltage, it is usually better to add an output filter (Figure 22) than to simply "brute force" the ripple by using very large output capacitors. The output filter consists of a small inductor (≈2μH-10μH) and a second output capacitor, usually 50μF-200μF. The inductor must be rated at full load current. Its core material is not important (core loss is negligible) except that core material will determine the size and shape of the inductor. Series resistance should be low enough to avoid unwanted efficiency loss. This can be estimated from;

$$R_L = \frac{(\Delta E)(V_{OUT})}{(I_{OUT})(E)^2} \tag{105}$$

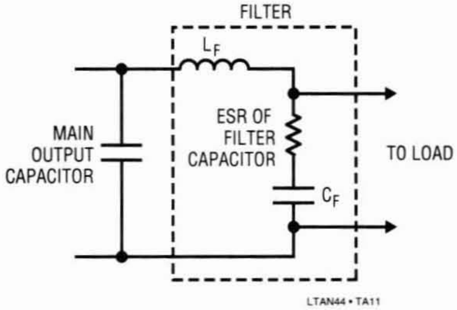


Figure 22. Output Filter

"E" is overall efficiency and ΔE is the loss in efficiency allocated to the filter. Both are expressed as a ratio, i.e., 2% ΔE = 0.02, and 80% E = 0.8.

To obtain the required component values for the filter, one must assume a value for inductance or capacitor ESR, then calculate the remaining value. Actual capacitance in microfarads is of secondary importance because it is assumed that the capacitor will be basically resistive at ripple frequencies. One consideration on filter capacitor value is the load transient response of the converter. A small output filter capacitor (high ESR) will allow the output to "bounce" excessively if large amplitude load transients occur. When these load transients are expected, the size of the output filter capacitor must be increased to meet transient requirements rather than just ripple limits. In this situation, the main output capacitor can be reduced to simply meet ripple current requirements. The complete design should be checked for transient response with full expected load change.

If the capacitor is selected first, the inductor value can be found from ripple attenuation requirements.

Buck converter with triangular ripple into filter

$$L_f = \frac{(ESR)(ATTN)}{8f} \tag{106}$$

All other converters with essentially rectangular ripple into filter

$$L_f = \frac{(ESR)(ATTN)(DC)(1-DC)}{f} \tag{107}$$

ESR = Filter capacitor series resistance.

ATTN = Ripple attenuation required, as a ratio of peak-to-peak ripple IN to peak-to-peak ripple OUT.

DC = Duty cycle of converter. (If unknown, use worst case of 0.5).

Example: A 100kHz buck converter with 150mVp-p ripple which must be reduced to 20mV. ATTN = 150/20 = 7.5. Assume a filter capacitor with ESR = 0.3Ω

$$L = \frac{(0.3)(7.5)}{8\left(10^5\right)} = 2.8\mu H \tag{108}$$

Example: A 100kHz positive to negative converter with output ripple of 250mVp-p which must be reduced to 30mV. Assume duty cycle has been calculated at 30% = 0.3, and ESR of filter capacitor is 0.2Ω

$$L = \frac{(0.2)(250/30)(0.3)(1-0.3)}{10^5} = 3.5\mu H \tag{109}$$

If the inductor is known, the equations can be rearranged to solve for capacitor ESR.

Buck Converter; (110)

$$ESR = \frac{8f(L)}{ATTN}$$

Square Wave Ripple In;

$$ESR = \frac{f \bullet L}{(ATTN)(DC)(1-DC)}$$

The output filter will affect load regulation if it is "outside" the regulator feedback loop. Series resistance of the filter inductor will add directly to the closed loop output resistance of the converter. This closed loop resistance is typically in the range of 0.002Ω-0.01Ω, so a filter inductor resistance of 0.02Ω may represent a significant loss in load regulation. One solution is to move the filter "inside" the feedback loop by moving the sense points to the output of the filter. This should be avoided if possible because the added phase shift of the filter can cause difficulties in stabilizing the converter. Buck converters will tolerate an output filter inside the feedback loop by simply reducing the loop unity gain frequency. Positive to negative converters and boost converters have a "right half plane zero" which makes them very sensitive to additional phase shift. To avoid stability problems, one should first determine if the load regulation degradation caused by a filter is really a problem. Most digital and analog "chips" in use today tolerate modest changes in supply voltage with little or no effect on performance.

When the sense resistor is tied to the output of the filter, a "fix" for stability problems is to connect a capacitor from the input of the filter to a tap on the feedback divider as shown in Figure 23. This acts as a "feedforward" path around the filter. The minimum size of C_X will be determined by the filter response, but should be in the range of 0.1µF-1µF.

C_X could theoretically be connected directly to the FB pin, but this should be done only if the peak-to-peak ripple on the main output capacitor is less than 75mVp-p.

A word about "measured" filter output ripple. The true ripple voltage should contain only the fundamental of the switching frequency because higher harmonics and "spikes" are very heavily attenuated. If the ripple as measured on an oscilloscope is abnormally high or contains high frequencies, the measurement technique is probably at fault. See the "Oscilloscope Techniques" section.

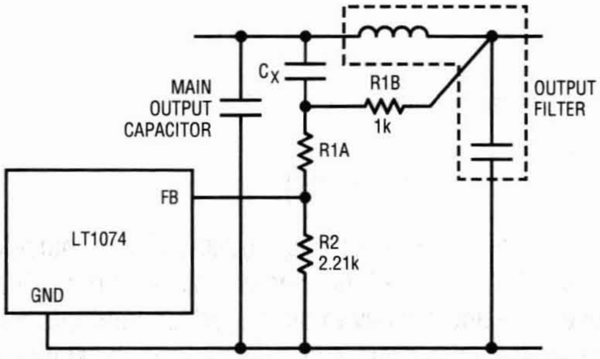


Figure 23. Feedforward when Output Filter is Inside Feedback Loop

INPUT FILTERS

Most switching regulators draw power from the input supply with rectangular or triangular current pulses. (The exception is a boost converter where the inductor acts as a filter for input current). These current pulses are absorbed primarily by the input bypass capacitor which is located right at the regulator input. Significant ripple current can still flow in the input lines, however, if the impedance of the source, including the inductance of supply lines, is low. This ripple current may cause unwanted ripple voltage on the input supply or may cause EMI in the form of magnetic radiation from supply lines. In these cases, an input filter may be required. The filter consists of an inductor in series with the input supply combined with the input capacitor of the converter, as shown in Figure 24.

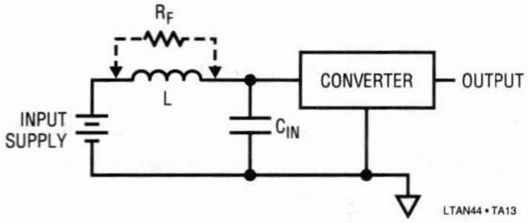


Figure 24. Input Filter

To calculate a value for L requires knowledge of what ripple current is allowed in the supply line. This is normally an unknown parameter, so much hand waving may go on in search of a value. Assuming that a value *has* been arrived at, L is found from;

$$L=\frac{ESR(DC)(1-DC)}{f\left(\frac{I_{SUP}}{I_{CON}}-\frac{ESR}{Rf}\right)} \qquad (111)$$

ESR = Effective series resistance of input capacitor.

DC = Converter duty cycle. If unknown, use 0.5 as worst case.

I_{CON} = Peak-to-peak ripple current drawn by the converter, assuming continuous mode. For buck converters, $I_{CON} \approx I_{OUT}$. Positive to negative converters have $I_{CON} = I_{OUT}(V_{OUT}' + V_{IN}')/V_{IN}'$. Tapped-inductor $I_{CON} = I_{OUT}(N \bullet V_{OUT}' + V_{IN}')/[V_{IN}'(1+N)]$.

I_{SUP} = Peak-to-peak ripple allowed in supply lines.

R_f = "Damping" resistor which may be required to prevent instabilities in the converter.

Example: A 100kHz buck converter with $V_{OUT} = 5V$, $I_{OUT} = 4A$, $V_{IN} = 20V$, (DC = 0.25). Input capacitor ESR is 0.05Ω. It is desired to reduce supply line ripple current to 100mA(p-p). Assume R_f is not needed (= ∞).

$$L = \frac{(0.05)(0.25)(1-0.25)}{10^5\left(\frac{0.1}{4}-0\right)} = 3.75\mu H \qquad (112)$$

For further details on input filters, including the possible need for a damping resistor (R_f), see the "Input Filters" section in Application Note 19.

The current rating of the input inductor must be a minimum of;

$$I_L = \frac{(V_{OUT})(I_{OUT})}{(V_{IN})(E)} \text{ Amps} \qquad (113)$$

$(\text{Use Minimum } V_{IN})$

For this example;

$$I_L = \frac{(5)(4)}{(20)(E \approx 0.8)} = 1.25A$$

Efficiency or overload considerations may dictate an inductor with higher current rating to minimize copper losses. Core losses will usually be negligible.

OSCILLOSCOPE TECHNIQUES

Switching regulators are a perfect test bed for poor oscilloscope techniques. A "scope" can lie in many ways and they all show up in a switching regulator because of the combination of fast and slow signals, coupled with both large and very small amplitudes. The following Rogue's Gallery will hopefully help the reader avoid many hours of frustration (and eliminate some embarrassing phone calls to the author).

Ground Loops

Good safety practice requires most instruments to have their "ground" system tied to a "third" (green) wire in the power cord. This unfortunately results in current flow through oscilloscope probe ground leads (shield) when other instruments source or sink current to the device under test. Figure 25 details this effect.

A generator is driving a 5V signal into 50Ω on the breadboard, resulting in a 100mA current. The return path for this current divides between the ground from the signal generator (typically the shield on a BNC cable) and the secondary ground "loop" created by the oscilloscope probe ground clip (shield), and the two "third wire" connections on the signal generator and oscilloscope. In

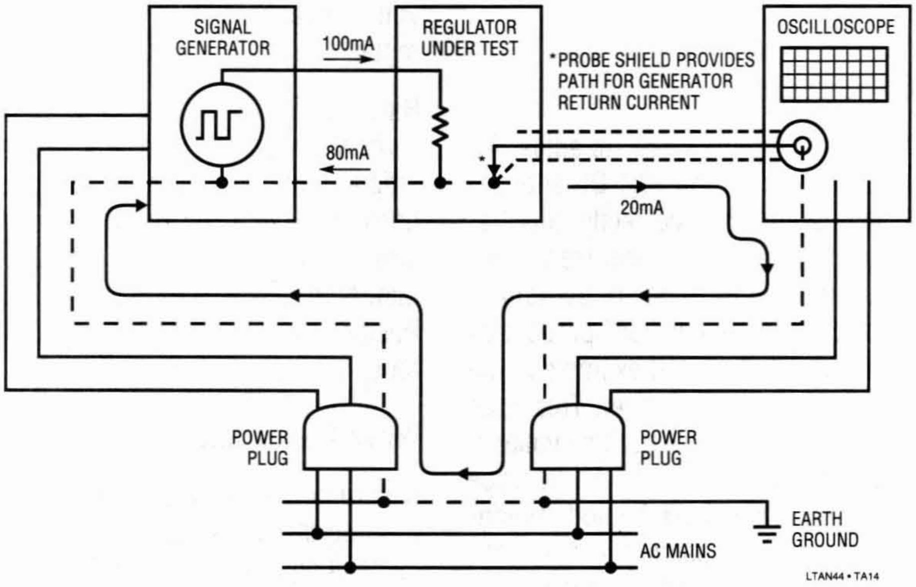


Figure 25. Ground Loop Errors

this case, it was assumed that 20mA flows in the parasitic ground loop. If the oscilloscope ground lead has a resistance of 0.2Ω, the screen will show a 4mV "bogus" signal. The problem gets much worse for higher currents, and fast signal edges where the inductance of the scope probe shield is important.

DC ground loops can be eliminated by disconnecting the third wire on the oscilloscope (its called a cheater plug, and my lawyers will *not* let me recommend it!) or by the use of an isolation transformer in the oscilloscope power connection.

Another source of circulating current in the probe shield wire is a second connection between a signal source and the scope. A typical example is a trigger signal connection between the generator trigger output and the scope external trigger input. This is most often a BNC cable *with its own grounded shield connection.* This forms a second path for signal ground return current, with the scope probe shield completing the path. My solution is to use a BNC cable which has had its shield intentionally broken. The trigger signal may be less than perfect, but the scope will not care. Mark the cable to prevent normal use!

Rule #1: *Before making any low level measurements, touch the scope probe "tip" to the probe ground clip with the clip connected to the desired breadboard ground.* The "scope" should indicate flatline. Any signal displayed is a ground loop lie.

Miscompensated Scope Probe

10X scope probes must be "compensated" to adjust AC attenuation so it precisely matches the 10:1 DC attenuation of the probe. If this is not done correctly, low frequency signals will be distorted and high frequency signals will have the wrong amplitude. In switching regulator applications, a "miscompensated" probe may show "impossible" waveforms. A typical example is the switching node of an LT1074 buck converter. This node swings positive to a level 1.5V-2V *below* the input voltage, and negative to one diode drop below ground. A 10X probe with too little AC attenuation could show the node swinging *above* the supply, and so far negative that the diode forward voltage appears to be many volts instead of the expected 0.5V. Remember that at these frequencies (100kHz), the wave *shape* looks right because the probe acts purely capacitive, so the wrong amplitude may not be immediately obvious.

Rule #2: Check 10X scope probe compensation *before* being embarrassed by a savvy tech.

Ground "Clip" Pickup

Oscilloscope probes are most often used with a short ground "lead" with an alligator clip on the end. This ground wire is a remarkably good antenna. It picks up local magnetic fields and displays them in full color on the oscilloscope screen. Switching regulators generate lots of magnetic fields. Switch wires, diodes, capacitor and inductor leads, even "DC" supply lines can radiate significant magnetic fields because of the high currents and fast rise/fall times encountered. The test for ground clip problems is to touch the probe tip to the alligator clip, with the clip connected to the regulator ground point. Any trace seen on the screen is caused either by circulating currents in a ground loop, or by antenna action of the ground clip.

The fix for ground clip "pickup" is to throw the clip wire away and replace it with a special soldered-in probe terminator which can be obtained from the probe manufacturer. The plastic probe tip cover is pulled off to reveal the naked coaxial metal tube shield which extends to the small needle tip. This tube slips into the terminator to complete the ground connection. This technique will allow you to measure millivolts of output ripple on a switching regulator even in the presence of high magnetic fields.

Rule #3: *Don't make any low level measurements on a switching regulator using a standard ground clip lead.* If an official terminator is not available, solder a solid bare hookup wire to the desired ground point and wrap it around the exposed probe coaxial tube with absolute minimum distance between the ground point and the tube. Position the ground point so that the probe needle tip can touch the desired test point.

Wires Are Not Shorts

A common error in probing switching regulators is to assume that the voltage anywhere on a wire path is the same. A typical example is the ripple voltage measured at the output of a switching regulator. If the regulator delivers square waves of current to the output capacitor, a positive to negative converter for instance, the current rise/fall time will be approximately 10^8A/sec. This dI/dt will generate ≈*2V per inch* "spikes" in the lead inductance of the output capacitor. The output (load) traces of the regulator should connect directly to the through-hole points where the radial-lead output capacitor leads are soldered in. The oscilloscope probe tip terminator (no ground clips, please) must be tied in directly at the base of the capacitor also.

The 2V/in. number can cause significant measurement errors even at high level points. When the input voltage to a switching regulator is measured across the input bypass capacitor, the spikes seen may be only a few tenths of a volt. If that capacitor is several inches away from the LT1074 though, the spikes "seen" by the regulator may be many volts. This can cause problems, especially at a low input voltage. Probing the "wrong" point on the input wire might mask these spikes.

Rule #4: If you want to know what the voltage is *on a high AC current signal path, define exactly which component voltage you are measuring* and connect the probe terminator directly across that component. As an example, if your circuit has a snubber to protect against switch overvoltage, connect the probe terminator *directly* to the IC switch terminals. Inductance in the leads connecting the switch to the snubber may cause the switch voltage to be many volts higher than the snubber voltage.

EMI SUPPRESSION

Electromagnetic interference (EMI) is a fact of life with switching regulators. Consideration of its effects should occur early in the design so that the electrical, physical, and monetary implications of any required filtering or shielding are understood and accounted for. EMI takes two basic forms; "conducted," which travels down input and output wiring, and "radiated," which takes the form of electric and magnetic fields.

Conducted EMI occurs on input lines because switching regulators draw current from their input supply in pulses, either square wave, or triangular, or a combination of these. This pulsating current can create bothersome ripple voltage on the input supply and it can radiate from input lines to surrounding lines or circuitry.

Conducted EMI on the output of a switching regulator is usually limited to the voltage ripple on the output nodes. Ripple frequencies from buck regulators consist almost entirely of the fundamental switching frequency, whereas boost and inverting regulator outputs contain much higher frequency harmonics if no additional filtering is used.

Electric fields are generated by the fast rise and fall times of the switch node in the regulator. EMI from this source is usually of secondary concern and can be minimized by keeping all connections to this node as short as possible and by keeping this node "internal" to the switching regulator circuitry so that surrounding components act as shields.

The primary source of electric field problems *within* the regulator itself is coupling between the switching node and the feedback pin. The switching node has a typical slew rate of 0.8×10^9V/sec., and the impedance at the feedback pin is typically 1.2kΩ. Just 1PF coupling between these pins will generate 1V spikes at the feedback pin, creating erratic switching waveforms. Avoid long traces on the feedback pin by locating the feedback resistors immediately adjacent to the pin. When coupling to switching node cannot be avoided, a 1000pF capacitor from the LT1074 ground pin to the feedback pin will prevent most pickup problems.

Magnetic fields are more troublesome because they are generated by a variety of components, including the input and output capacitors, catch diode, snubber networks, the inductor, the LT1074 itself, and many of the wires connecting these components. While these fields do not usually cause regulator problems, they can create problems for surrounding circuitry, especially with low level signals such as disc drives, data acquisition, communication, or video processing. The following guidelines will be helpful in minimizing magnetic field problems.

1. Use inductors or transformers with good EMI characteristics such as toroids or pot cores. The worst offenders from an EMI standpoint are "rod" inductors. Think of them as cannon barrels firing magnetic flux lines in every direction. Their only application in switchers should be in the output filter where ripple current is very low.

2. Route all traces carrying high ripple current over a ground plane to minimize radiated fields. This includes the catch diode leads, input and output capacitor leads, snubber leads, inductor leads, LT1074 input and switch pin leads, and input power leads. Keep these leads short and the components close to the ground plane.

3. Keep sensitive low level circuitry as far away as possible, and use field-cancelling tricks such as twisted-pair differential lines.

4. In critical applications, add a "spike killer" bead on the catch diode to suppress high harmonics. These beads will prevent very high dI/dt signals, but will also make the diode appear to turn "on" slowly. This can create higher transient switch voltages at switch turn-off, so switch waveforms should be checked carefully.

5. Add an input filter if radiation from input lines could be a problem. Just a few µH in the input line will allow the regulator input capacitor to swallow nearly all the ripple current created at the regulator input.

TROUBLESHOOTING HINTS

Low Efficiency

The major contributors here are switch and diode loss. These are readily calculable. If efficiency is abnormally low after factoring in these effects, zero in on the inductor. Core or copper loss may be the problem. Remember that inductor current may be much higher than output current in some topologies. A very handy substitution tool is a 500µH inductor wound with heavy wire on a large molypermalloy core. 100µH and 200µH taps are helpful. This inductor can be substituted for suspect units when inductor losses are suspected. If you read this App Note, you will know that a large core is used not to reduce core loss, but to allow enough room for large wire that eliminates copper loss.

If inductor losses are not the problem, check all the nickel and dime effects such as quiescent current and capacitor loss to see if the sum is no longer negligible.

Alternating Switch Timing

Switch "on" time may alternate from cycle to cycle if excess switching frequency ripple appears on the V_C pin. This can occur naturally because of high ESR in the output capacitor or because of pickup on the FB pin or the V_C pin. A simple check is to put a 3000pF capacitor from V_C pin to the ground pin close to the IC. If the erratic switching improves or is cured, excess V_C pin ripple is the problem. Isolate it by connecting the capacitor from FB to ground pin. If this also makes the problem disappear, V_C pin pickup is eliminated, and FB pickup is the likely culprit. The feedback resistors should be located close to the IC so that connections to the FB pin are short and routed away from switching nodes. A 500pF capacitor from FB to ground pin will usually be sufficient if pickup cannot be eliminated. Occasionally, excess output ripple is the problem. This can be checked by paralleling the output capacitor with a second unit. A 1000pF-3000pF capacitor on V_C can often be used to stop erratic switching caused by high output ripple, but be sure the ripple current rating of the output capacitor is adequate!

Input Supply Won't Come Up

Switching regulators have negative input resistance at DC. Therefore, they draw high current at low V_{IN}. This can latch input supplies low. See "Soft Start" section for details.

Switching Frequency is Low in Current Limit

This is normal. See "Frequency Shifting at the Feedback Pin" in the Pin Description section.

IC Blows Up!

Like the LT1070 before it, the only thing that can destroy the LT1074 or LT1076 is excess switch voltage. (I am ignoring obvious stuff like voltage reversal or wiring errors).

Start-up surges can sometimes cause momentary large switch voltages, so check voltages carefully with an oscilloscope. Read the section on oscilloscope techniques.

IC Runs Hot

A common mistake is to assume that heat sinks are no longer needed with a switching design. This is often true for small load currents, but as load current climbs above 1A, switch loss may increase to the point where a heat sink is needed. A TO-220 package has a thermal resistance of 50°C/W with no heat sink. A 5V, 3A output (15W) with 10% switch loss, will dissipate over 1.5W in the IC. This means a 75°C temperature rise, or 100°C case temperature at room ambient. This is normally referred to as hot! A small heat sink solves the problem. Simply soldering the TO-220 tab to an enlarged copper pad on the PC board will reduce thermal resistance to ≈25°C/W.

High Output Ripple or Noise Spikes

First read "Oscilloscope Techniques" section to avoid possible embarrassment, then check ESR of the output capacitor. Remember that fast (<100ns) spikes will be greatly attenuated by parasitic supply line inductance and load capacitance even if supply lines are only a few inches long.

Poor Load or Line Regulation

Check in this order:

1. Secondary output filter DC resistance if it is outside the loop.
2. Ground loop error in oscilloscope.
3. Improper connection of output divider resistors to current carrying lines.
4. Excess output ripple. The LT1074 can peak detect ripple voltages on the FB pin if they exceed 50mVp-p.

See "Reference Shift with Ripple Voltage" graph in Typical Performance Characteristics section.

500kHz-5MHz Oscillations, Especially at Light Load

This is discontinuous mode ringing and is quite normal and harmless. See buck converter waveform description for more details.

Application Note 45

June 1991

Measurement and Control Circuit Collection

Diapers and Designs on the Night Shift

Jim Williams

Introduction

During my wife's pregnancy I wondered what it would *really* be like when the baby was finally born. Before that time, there just wasn't much mothering and fathering to do. As a consolation, we busied ourselves watching the baby's heartbeat (Figure 1) on a thrown-together fetal heart monitor (see References).

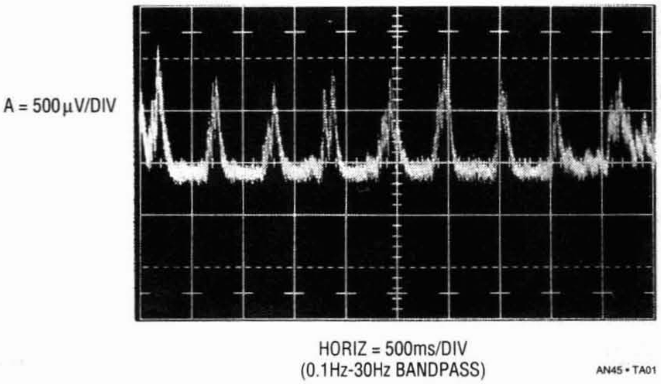


Figure 1. Michael's Fetal Heartbeat 4 1/2 Months into Pregnancy

When Michael was born things got noticeably busier in a hurry. My wife and I split up the evening duties. I got the night shift, 2 am to 7 am. After a few weeks, Michael and I got the hang of it and things began to go (relatively) smoothly. The two of us had mastered feedings, naps, crying jags, bottles, diapers and such and we began looking around for something to do. I decided to introduce Michael to the glories of late night circuit hacking. I first learned about wee hours circuit design at MIT in the 1970s. There was a subculture there that loaded up on pizza, soft drinks, and junk food, took it all into the lab, and closed the door until long after daylight. I was an enthusiastic convert.

Michael and I changed the rules just a bit. We loaded up on formula, diapers, and bottles and went into the lab.

The circuits in this collection represent our efforts, which stopped when he (more or less) began sleeping through the night. Most of the breadboarding occurred between feedings, with design reviews and discussions during feedings. As such, the circuits are annotated with the number of feedings required for their completion; e.g. a "3-bottle circuit" took three feedings. The circuit's degree of difficulty, and Michael's degree of cooperation, combined to determine the bottle rating, which is duly recorded in each figure.

Low Noise and Drift Chopped Bipolar Amplifier

Figure 2's circuit combines the low noise of an LT1028 with a chopper based carrier modulation scheme to achieve an extraordinarily low noise, low drift DC amplifier. DC drift and noise performance exceed any currently available monolithic amplifier. Offset is inside 1µV, with drift less than 0.05µV/°C. Noise in a 10Hz bandwidth is less than 40nV, far below monolithic chopper stabilized amplifiers.

Bias current, set by the bipolar LT1028 input, is about 25nA. These specifications suit demanding transducer signal conditioning situations such as high resolution scales and magnetic search coils.

The 74C04 inverters form a simple two-phase square wave clock running at about 350Hz. The oscillator provides complementary drive to S1 and S2, causing A1 to see a chopped version of the input voltage. A1 amplifies this AC signal. A1's square wave output is synchronously demodulated by S3 and S4. Because these switches are synchronously driven with the input chopper, proper amplitude and polarity information is presented to A2, the DC output amplifier. This stage integrates the square wave into a DC voltage, providing the output. The output is divided down (R2 and R1) and fed back to the input chopper where it serves as a zero signal reference. Gain, in this case 1000, is set by the R1-R2 ratio. Because A1 is AC coupled, its DC offset and drift do not affect overall circuit offset, resulting in the extremely low offset and drift noted.

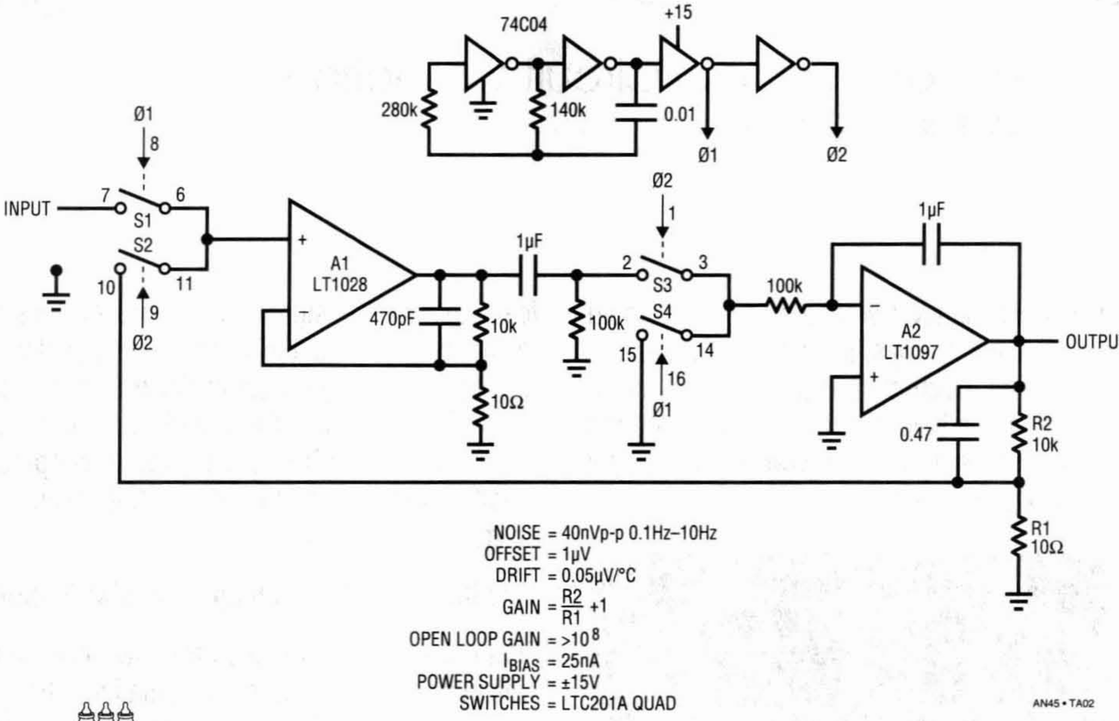

74C04
+15
280k
140k
0.01
Ø1
Ø2
Ø1
8
INPUT
7
6
S1
S2
10
11
9
Ø2
A1
LT1028
470pF
10k
10Ω
1µF
100k
Ø2
1
2
3
S3
S4
15
14
16
Ø1
100k
1µF
A2
LT1097
OUTPUT
0.47
R2
10k
R1
10Ω
NOISE = 40nVp-p 0.1Hz–10Hz
OFFSET = 1µV
DRIFT = 0.05µV/°C
GAIN = $\frac{R2}{R1}$ +1
OPEN LOOP GAIN = >10^8
I_{BIAS} = 25nA
POWER SUPPLY = ±15V
SWITCHES = LTC201A QUAD
AN45 • TA02

Figure 2. The Chopped Bipolar Amplifier. Noise is Inside 40nV with 0.05µV/°C Drift

Figure 3, a noise plot of the amplifier in a 0.1Hz-10Hz bandwidth, shows less than 40nV of peak-to-peak noise. A1 and the 60Ω resistance of S1-S2 contribute about equally to form this noise. When using this amplifier it is important to realize that A1's bias current flowing through the input source impedance causes additional noise. In general, to maintain low noise performance, source resistance should be kept below 500Ω. Fortunately, transducers such as strain gauge bridges, RTDs, and magnetic detectors are well below this figure.

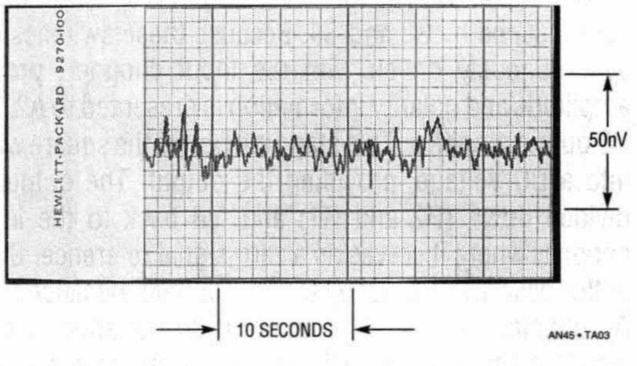


Figure 3. Noise in a 0.1Hz-10Hz Bandwidth is Less Than 40nV with 0.05µV/°C Drift

Low Noise and Drift Chopped FET Amplifier

Figure 4's circuit combines the low drift of a chopper stabilized amplifier with a pair of low noise FETs. The result is an amplifier with 0.05µV/°C drift, offset within 5µV, 50pA bias current, and 200nV noise in a 0.1Hz-10Hz bandwidth. The noise performance is especially noteworthy; it is almost eight times better than monolithic chopper stabilized amplifiers.

FET pair Q1 differentially feeds A2 to form a simple low noise op amp. Feedback, provided by R1 and R2, sets closed loop gain (in this case 1000) in the usual fashion. Although Q1 has extraordinarily low noise characteristics, its 15mV offset and 25µV/°C drift are poor. A1, a chopper stabilized amplifier, corrects these deficiencies. It does this by measuring the difference between the amplifier's inputs and adjusting Q1A's channel current to minimize the difference. Q1's skewed drain values ensure that A1 will be able to capture the offset. A1 supplies whatever current is required into Q1A's channel to force offset within 5µV. Additionally, A1's low bias current does not appreciably add to the overall 50pA amplifier bias current. As shown, the amplifier is set up for a non-inverting gain of 1000, although other gains and inverting operation are

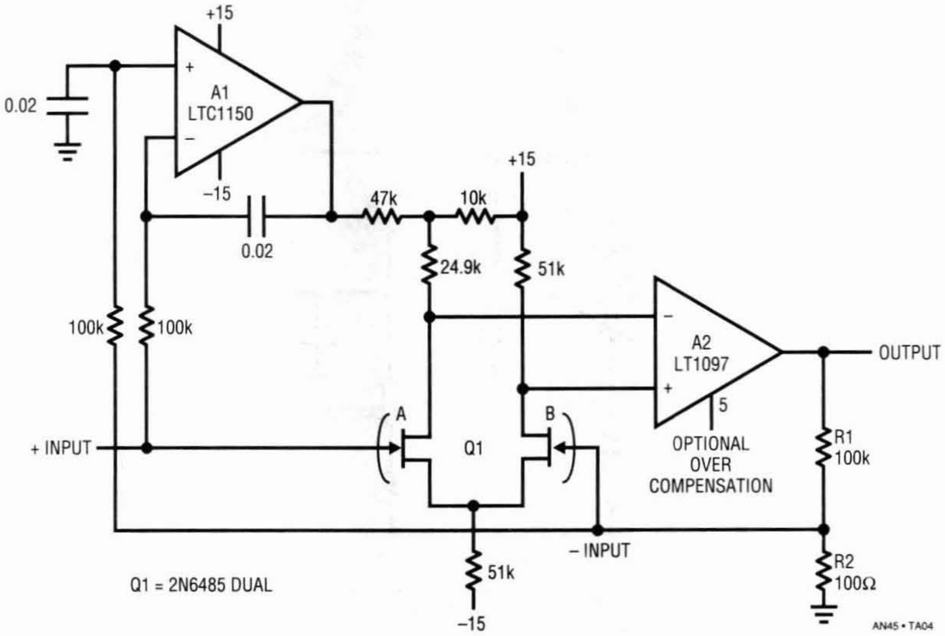


Figure 4. Chopper Stabilized FET Pair Combines Low Bias, Offset and Drift with 200nV Noise

possible. Figure 5 is a plot of noise measured in a 0.1Hz-10Hz bandwidth. The performance obtained is almost an order of magnitude better than any monolithic chopper stabilized amplifier, while retaining low offset and drift.

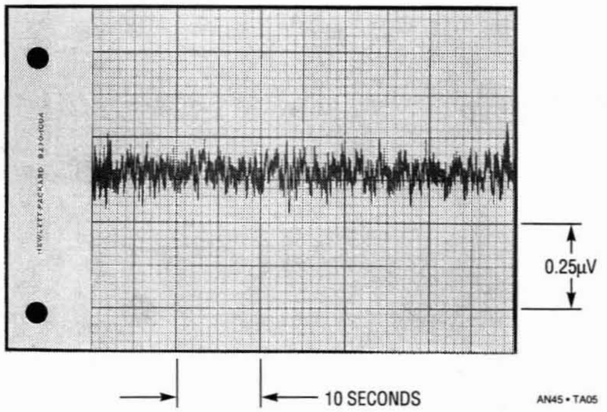


Figure 5. Noise Performance for Figure 4. A1's Low Offset and Drift are Retained, but Noise is Almost Ten Times Better

A2's optional overcompensation can be used (capacitor to ground) to optimize damping for low closed loop gains.

Stabilized, Wideband Cable Driving Amplifier with Low Input Capacitance

Figure 6's amplifier has over 20MHz of small signal bandwidth driving 100mA loads, capacitance or cable. Input capacitance is below 1.5pF and bias current about 100pA. The output is fully protected. These features make this amplifier ideal as an ATE pin amplifier, video A-D input buffer, or cable driver. The amplifier also permits wideband probing when oscilloscope probe loading is not tolerable. The overall amplifier is composed of a low input capacitance FET, two LT1010 buffers, and a discrete gain stage. A3 acts as a DC restoration loop. The 33Ω resistors sense A1's operating current, biasing Q3 and Q4. These devices furnish complementary voltage gain to A2, which provides the circuit's output. Feedback is from A2's output to A1's output, which is a low impedance point. This "current mode" feedback permits fixed bandwidth over a wide range of closed loop gains. This contrasts with normal feedback schemes where bandwidth degrades as closed loop gain increases.

A3's stabilizing loop compensates large offsets in the signal path, which are dominated by mismatch in Q3 and Q4. A3 measures the DC difference between the amplifier's input and output and biases the signal path to correct for offset. Correction is implemented by controlling Q1's channel current via Q2. The channel current sets Q1's V_{GS}, allowing A3 to control overall circuit offset. The 9k-1k feedback divider feeding A3 is selected to equal the gain ratio of the circuit, in this case 10.

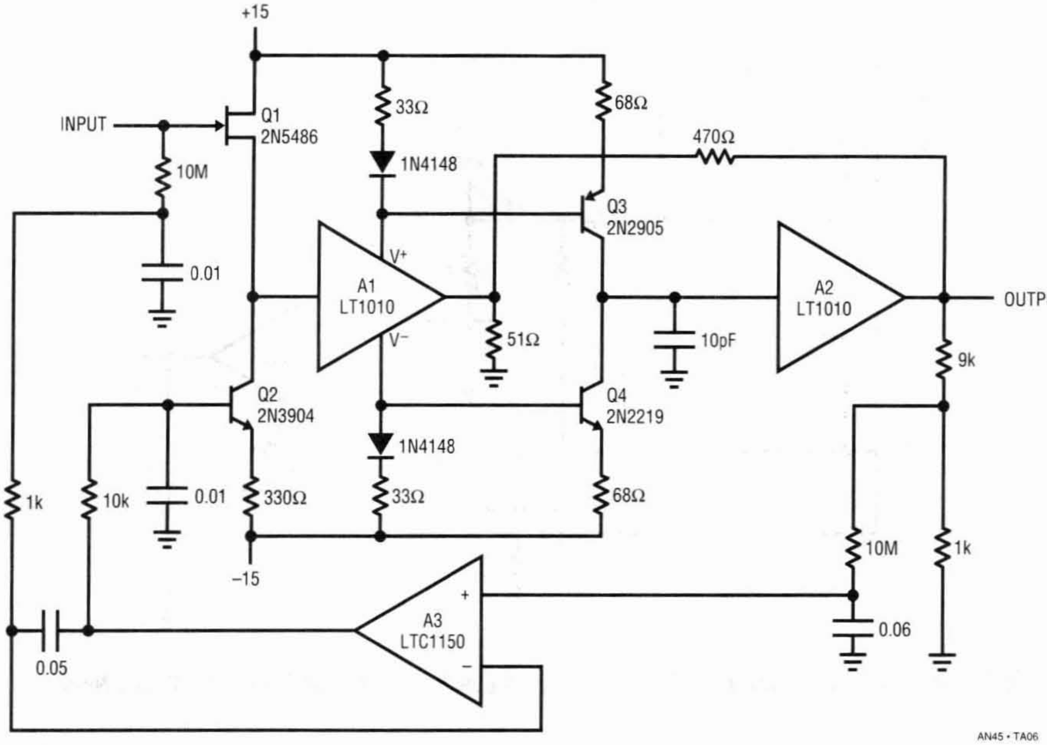

+15
INPUT
Q1
2N5486
10M
0.01
33Ω
1N4148
68Ω
470Ω
Q3
2N2905
V+
A1
LT1010
V–
51Ω
10pF
A2
LT1010
OUTPUT
9k
Q2
2N3904
Q4
2N2219
1N4148
1k
10k
0.01
330Ω
33Ω
68Ω
–15
10M
1k
A3
LTC1150
+
–
0.06
0.05
AN45 • TA06

Figure 6. Stabilized, Wideband Cable Driving Amplifier with Low Input Capacitance

The feedback scheme makes A1's output look like the negative input of the amplifier, with closed loop gain set by the ratio of the 470Ω and 51Ω resistors. The outstanding feature of this connection is that the bandwidth becomes relatively independent of closed loop gain over a reasonable range. For this circuit, small signal bandwidth exceeds 20MHz over gains of 1 to 20. The loop is quite stable, and the 10pF value at A2's input provides good damping over a wide range of gains.

Figure 7 shows large signal performance at a gain of 10 driving 10 feet of cable. A fast input pulse (trace A) produces the output shown (trace B). Response is quick and clean with no slew residue or poor dynamics.

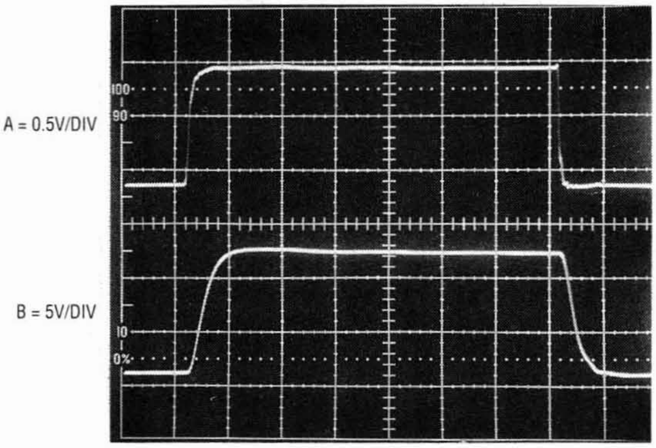


Figure 7. Wideband Amplifier's Response Driving A 10 Foot Cable

Voltage Programmable, Ground Referred Current Source

Precise, voltage programmable, ground referred current sources are usually complex and require trimming. Figure 8's simple, powerful configuration produces output current in strict accordance with the sign and magnitude of the control voltage. Dynamic response is well controlled, and no trimming is required. The circuit's accuracy and stability are almost entirely dependent upon resistor R.

A1, biased by V_{IN}, drives current through R (in this case 10Ω) and the load. Instrumentation amplifier A2, operating at a gain of 100, senses across R. A2's output closes a loop back to A1. Because A1's loop forces a fixed voltage

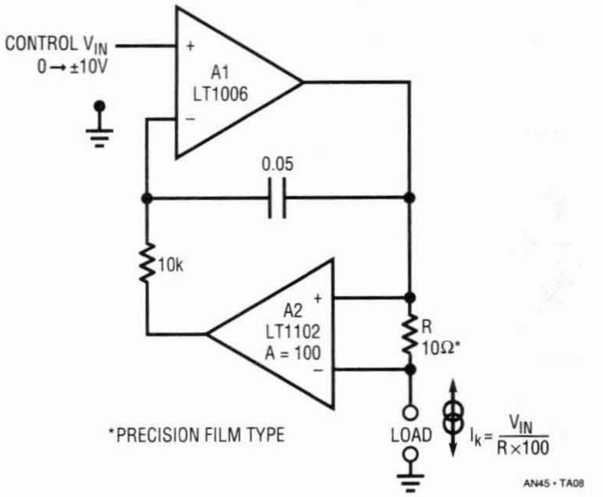


Figure 8. Voltage Programmable Current Source is Simple and Precise

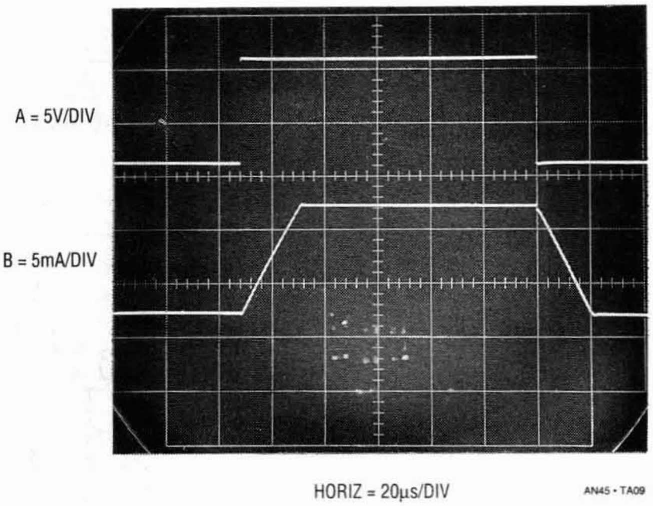


Figure 9. Current Source Dynamics are Clean, with No Slew Residue or Aberrations

across R, the current through the load is constant. The 10k-0.05μF combination sets A1's rolloff, and the circuit is stable.

Assuming an errorless component for R, the circuit's initial error is dominated by A2's 0.05% gain specification and its 5ppm/°C temperature coefficient. High grade film or wirewound resistors will maintain this level of performance.

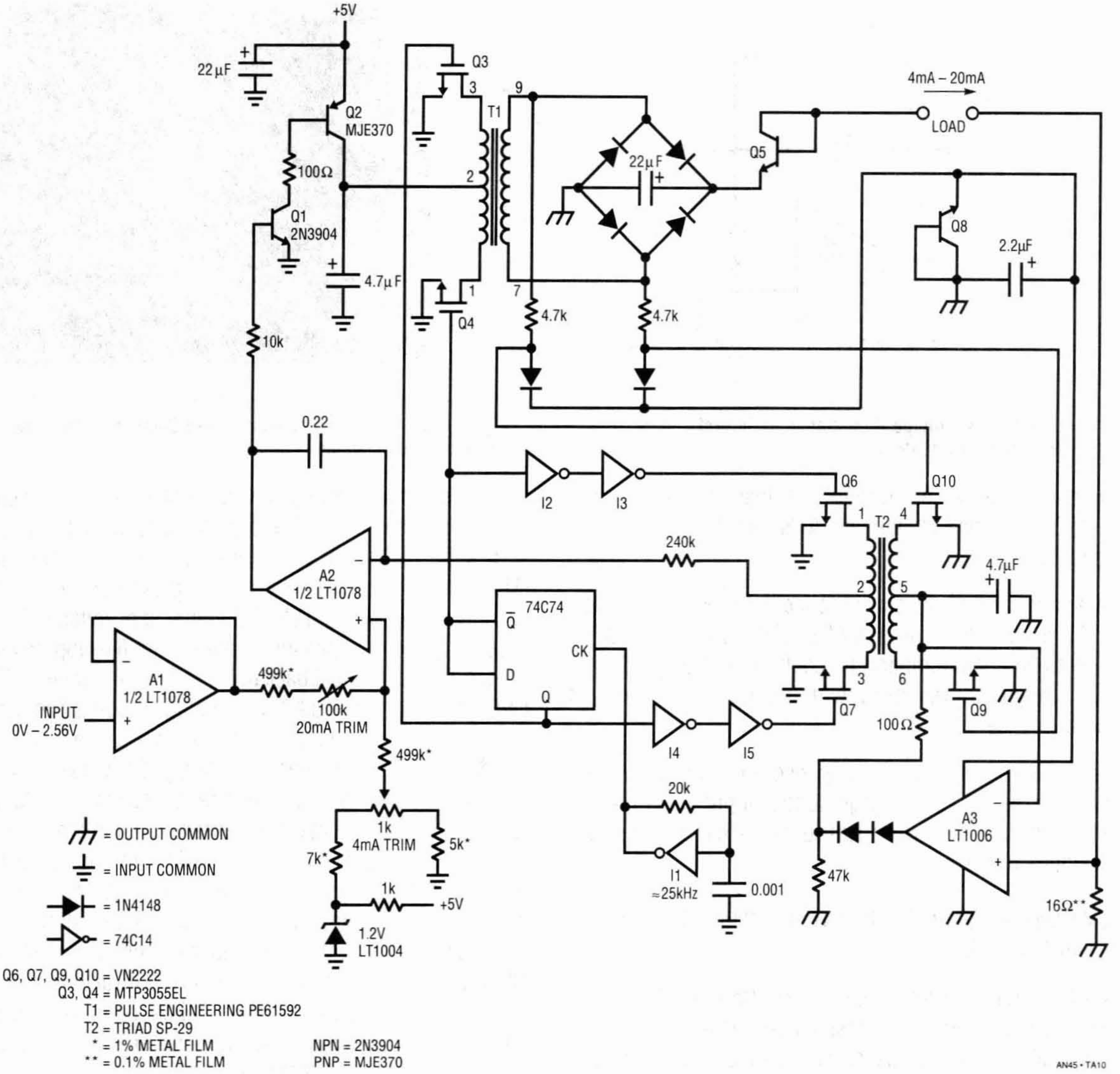
Figure 9 shows dynamic response for a full scale input step. Trace A is the voltage control input while trace B shows the output current. Response is clean, with no slew residue or aberrations.

5V Powered, Fully Floating 4mA to 20mA Current Loop Transmitter

4mA to 20mA current loop transmitters are frequently required in industrial process control. Often, because of uncertain or dangerous common mode voltages, it is desirable that the generated 4mA to 20mA current be completely galvanically isolated from the transmitter's input. Figure 10's circuit does this while operating from a single 5V supply.

A2's positive input assumes a bias dependent upon the input and the 4mA trim setting. Under these conditions A2's output heads positive, turning on Q1 and Q2. Q2's collector drives T1's primary, which is chopped by Q3 and Q4. Complementary chopper drive comes from the 74C74 flip-flop outputs, with oscillator I1 setting a 25kHz clock rate. T1's output, producing voltage step-up, is rectified, filtered, and applied to the load. A3 senses load current across the 16Ω shunt and drives T2's center tap. Q9 and Q10, receiving complementary drive picked-off from T1's secondary, modulate T2's DC center tap voltage. T2's secondary receives this information, with flip-flop driven Q6-Q7 demodulating it back to DC at T2's center tap. T2's center tap voltage is fed A2, completing an isolated control loop. Changes in the circuit's input voltage cause this loop to adjust the load current accordingly. Conversely, load resistance changes have no effect, because the loop forces whatever voltage is necessary to maintain a constant 16Ω shunt voltage. Because T1 can supply up to 50V, load current remains fixed over load resistance swings from 0Ω to 2500Ω. Power supply shifts are similarly rejected by the loop, and the transformer modulation-demodulation scheme permits 0.05% accuracy and stability over temperature and a 250V common mode range. Greater common mode voltages are possible with increased transformer breakdown ratings.

Several subtleties aid circuit performance. I2-I3 and I4-I5 provide drive delays to Q6 and Q7. These delays approximate the delay through T1 to modulator pair Q9/Q10. This helps the four transistors switch simultaneously, aiding modulator-demodulator accuracy. Zener connected Q5 ensures that T1 produces enough voltage to power A3 and Q9/Q10, even when the load is 0Ω. Q8, similarly zener connected, clamps gate drive to Q9 and Q10, improving modulator linearity by preventing excessive gate drive variations over operating conditions. The diodes in A3's


+5V
22µF
Q2
MJE370
100Ω
Q1
2N3904
4.7µF
10k
Q3
Q4
T1
3
9
2
1
7
22µF
Q5
4mA – 20mA
LOAD
Q8
2.2µF
4.7k
4.7k
0.22
A2
1/2 LT1078
A1
1/2 LT1078
INPUT
0V – 2.56V
499k*
100k
20mA TRIM
499k*
1k
4mA TRIM
7k*
5k*
1k
+5V
1.2V
LT1004
I2
I3
74C74
Q̄
D
CK
Q
I4
I5
20k
I1
≈25kHz
0.001
Q6
Q10
T2
240k
4.7µF
Q7
Q9
100Ω
A3
LT1006
47k
16Ω**
= OUTPUT COMMON
= INPUT COMMON
= 1N4148
= 74C14
AN45 • TA10

Q6, Q7, Q9, Q10 = VN2222
Q3, Q4 = MTP3055EL
T1 = PULSE ENGINEERING PE61592
T2 = TRIAD SP-29
* = 1% METAL FILM
** = 0.1% METAL FILM
NPN = 2N3904
PNP = MJE370

Figure 10. 5V Powered, Fully Floating 4mA-20mA Current Loop Transmitter

output ensure proper loop start-up. They prevent T2's center tap from receiving any bias until A3 has enough power supply voltage to function normally. To calibrate this circuit apply 0V input and adjust the 4mA trim for 4.00mA output (0.064V across the 16Ω shunt). Next, apply 2.56V input and set the 20mA trimmer for 20.00mA output (0.3200V across the 16Ω shunt). Repeat this procedure until both points are fixed. Note that the 2.56V input range is directly compatible with D-A converter outputs, permitting digital control.

Transistor ΔV_{BE} Based Thermometer

Low cost makes transistors potentially attractive as temperature sensors. Almost all transistor-sensed thermometer circuits utilize the base-emitter diode voltage shift with temperature as the sensing mechanism. Unfortunately, the absolute diode voltage is unpredictable, necessitating circuit calibration. Additionally, if the transistor sensor ever requires replacement, the calibration must be repeated. This constraint often negates the transistor sensor's cost and convenience advantages.

Figure 11's transistor sensor thermometer overcomes this difficulty. The circuit provides a 0V-10V output corresponding to a 0°C to 100°C temperature excursion at the sensor transistor. Accuracy is ±1°C. No calibration is required, and any common small signal NPN transistor can serve as the sensor. The circuit is based on the predictable relationship between current and voltage in a transistor V_{BE} junction.[1] At room temperature, the V_{BE} junction diode shifts 59.16mV per decade of current. The temperature dependence of this constant is 0.33%/°C, or 198μV/°C. This ΔV_{BE} versus current relationship holds, regardless of the V_{BE} diode's absolute value.

The LTC1043 contains switches whose state is controlled by an on-chip oscillator. The 0.01μF capacitor at pin 16 sets oscillator frequency at about 500Hz. Q1 operates as a switched value current source, alternating between about 10μA and 100μA (trace A, Figure 12) as the LTC1043 commutates switch pin 12 and pin 14. The two currents' exact value is unimportant, so long as their *ratio* remains constant. Because of this, Q1 requires no reference, although its emitter resistor's ratio is precise. The alternating 10μA-100μA stepped current to the sensor transistor

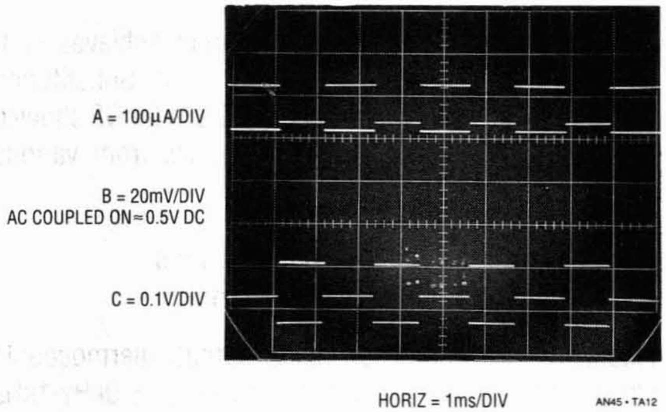
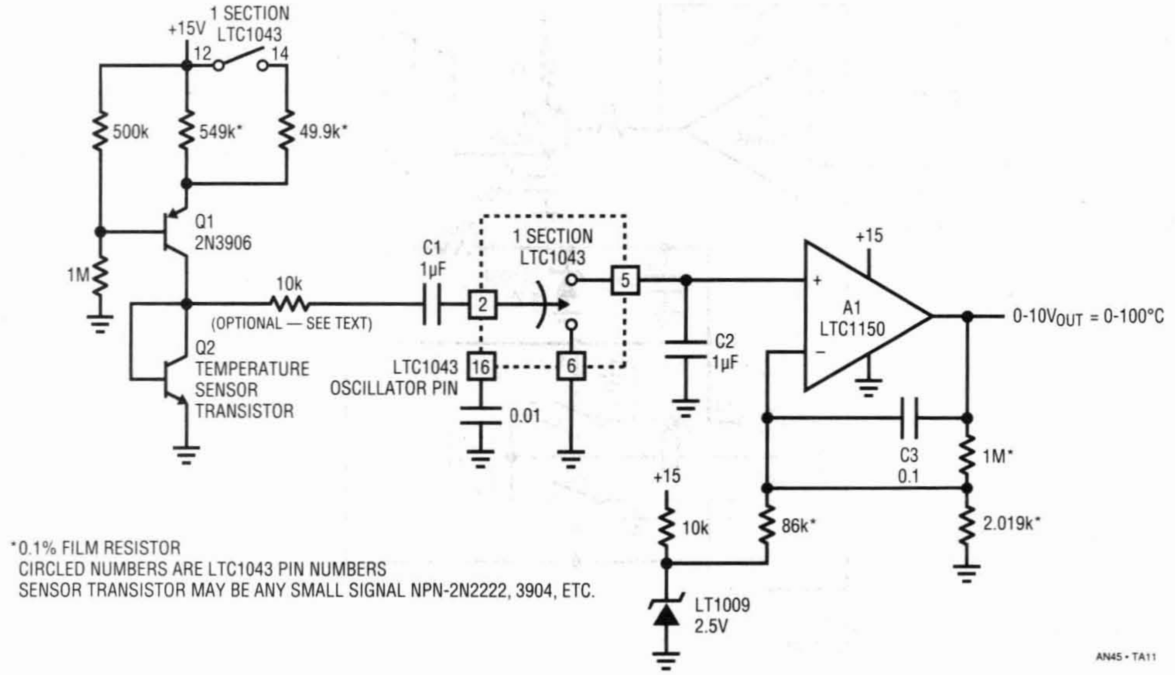


Figure 12. Waveforms for the ΔV_{BE} Based Thermometer


+15V
1 SECTION
LTC1043
12
14
500k
549k*
49.9k*
Q1
2N3906
1M
10k
(OPTIONAL — SEE TEXT)
Q2
TEMPERATURE
SENSOR
TRANSISTOR
C1
1μF
1 SECTION
LTC1043
2
5
16
6
LTC1043
OSCILLATOR PIN
0.01
C2
1μF
+15
A1
LTC1150
+
−
0-10V_OUT = 0-100°C
C3
0.1
1M*
+15
10k
86k*
2.019k*
LT1009
2.5V
AN45 • TA11

*0.1% FILM RESISTOR
CIRCLED NUMBERS ARE LTC1043 PIN NUMBERS
SENSOR TRANSISTOR MAY BE ANY SMALL SIGNAL NPN-2N2222, 3904, ETC.

Figure 11. ΔV_{BE} Based Thermometer Does Not Require Calibration

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Note 1: See References 1 through 4.

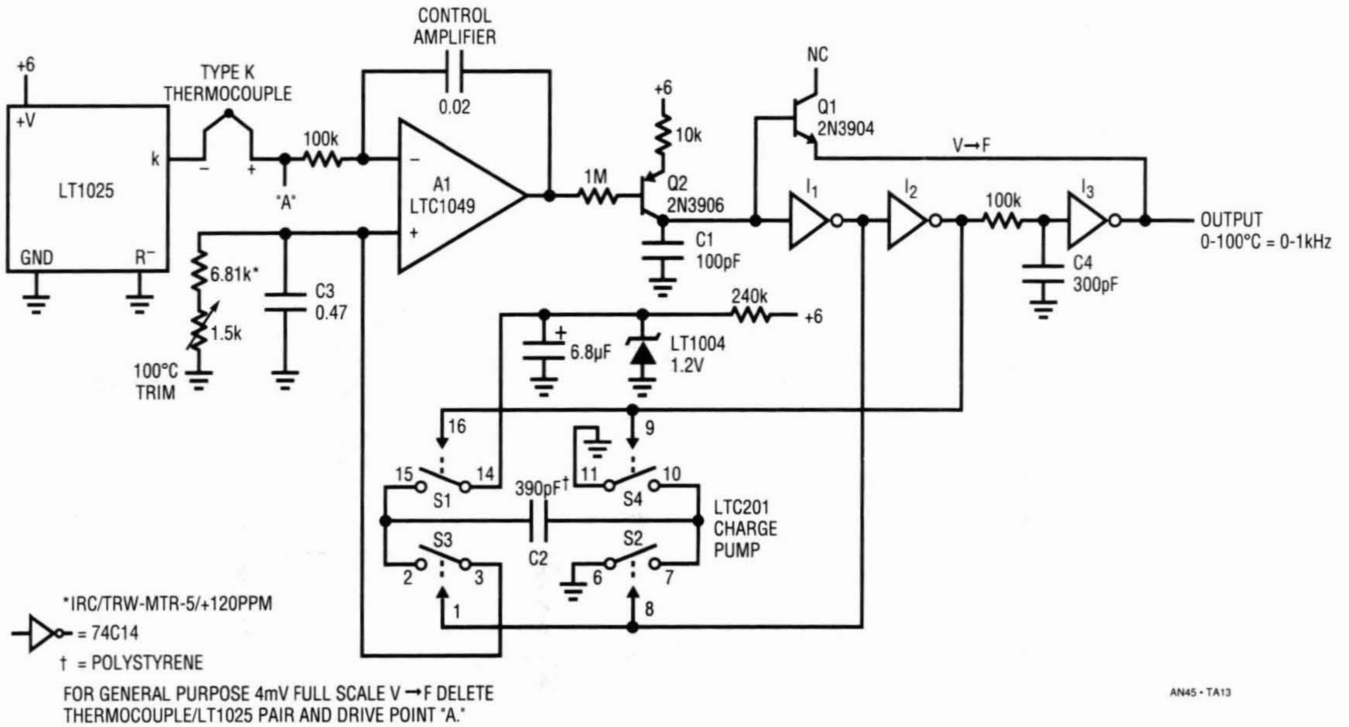
(Q2) causes the theoretical 59.16mV (25°C) excursion (trace B) to appear across the V_{BE} junction. This signal is coupled to a switched demodulator via C1, which strips off Q2's DC bias. LTC1043 switch pin 2 (trace C) sees only the 59mV waveform, which is referenced to ground via demodulator action at pin 5 and pin 6. Pin 5, connected to capacitor C2, sits at pin 2's DC peak value. A1 amplifies this DC signal, with the LT1004 providing offset so 0°C equals 0V. The optional 10k resistor protects against ESD events, which may occur if Q2 is located at the end of a cable.

Using the components shown, the circuit achieves ±1°C accuracy over a sensed 0°C to 100°C range. Substituting randomly selected 2N3904s and 2N2222s for Q2 showed less than 0.4°C spread over 25 devices from various manufacturers.

Micropower, Cold Junction Compensated Thermocouple-to-Frequency Converter

Figure 13 is a complete, digital output, thermocouple signal conditioner. The circuit produces a 0kHz-1kHz output in response to a sensed 0°C to 100°C temperature excursion. Cold junction compensation is included, and accuracy is within 1°C with stable 0.1°C resolution. Additionally, the circuit functions from a single supply, which may range from 4.75V to 10V. Maximum current consumption is 360µA.

The LT1025 provides an appropriately scaled cold junction compensation voltage to the type K thermocouple. As a result, the voltage at schematic point "A" varies from 0mV to 4.06mV over a sensed 0°C to 100°C range (type K slope is 40.6µV/°C). The remaining components form a voltage-to-frequency converter that directly converts this millivolt level signal without the usual DC gain stage. A1's negative input is biased by the thermocouple. A1's output drives a crude V-F converter, comprised of Q2, the 74C14 inverters, and associated components. Each V-F output pulse causes a fixed quantity of charge to be dispensed into C3 from C2 via the LTC201 based charge pump. C3 integrates the charge packets, producing a voltage at A1's positive input. A1's output forces the V-F converter to run at whatever frequency is required to balance the amplifier's inputs. This feedback action eliminates drift and nonlinearities in the V-F converter as an error term and the


CONTROL AMPLIFIER
0.02
+6
+V
LT1025
k
GND
R⁻
TYPE K THERMOCOUPLE
–
+
"A"
100k
A1
LTC1049
–
+
6.81k*
1.5k
100°C TRIM
C3
0.47
1M
+6
10k
Q2
2N3906
C1
100pF
NC
Q1
2N3904
V→F
I1
I2
I3
100k
C4
300pF
OUTPUT
0-100°C = 0-1kHz
240k
+6
6.8µF
LT1004
1.2V
16
15
14
S1
390pF†
11
10
S4
9
S3
S2
C2
2
3
6
7
1
8
LTC201 CHARGE PUMP
AN45 • TA13

*IRC/TRW-MTR-5/+120PPM

= 74C14

† = POLYSTYRENE

FOR GENERAL PURPOSE 4mV FULL SCALE V→F DELETE THERMOCOUPLE/LT1025 PAIR AND DRIVE POINT "A."

Figure 13. Thermocouple Sensed Temperature-to-Frequency Converter

output frequency is solely a function of the DC conditions at A1's inputs. The 0.02μF capacitor forms a dominant response pole at A1, stabilizing the loop. Chopper stabilized A1's low V_{OS} offset and drift eliminate offset error in the circuit, despite an output LSB value of only 4.06μV (0.1°C).

Figure 14 details circuit operation. A1's output biases current source Q2, producing a ramp (trace A, Figure 14) across C1. When the ramp crosses I1's threshold, the cascaded inverter chain switches, producing complementary outputs at I1 (trace B) and I2 (trace C). I3's RC delayed response (trace D) turns on diode connected Q1, discharging C1 and resetting the ramp. The ramp aberrations before the reset are due to transient I1 input currents during switching (near top of ramp). Q1's V_{BE} diode rounding and reverse charge transfer (bottom of ramp) account for the discontinuities during the ramp's low point.

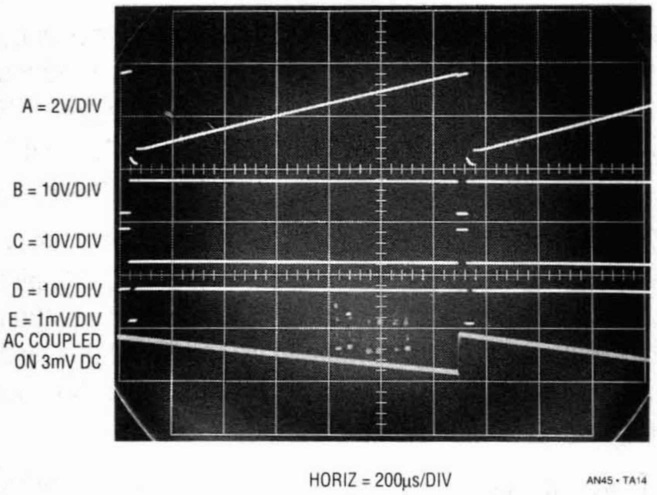


Figure 14. Waveforms for the Thermocouple-to-Frequency Converter

The complementary I1-I2 outputs clock the LTC201 switch based charge pump. C2 is alternately charged to the LT1004's reference voltage via S1 and S4 and discharged into C3 through S2 and S3. Each time this cycle occurs, C3's voltage is forced up (trace E). C3's average voltage is set by the 6.81k-1.5k trimmer resistance across it. A1 servo controls the repetition rate of the V-F to bring its inputs to the same value, closing a control loop. The 0.02μF capacitor smooths A1's response to DC.

To calibrate this circuit, disconnect the thermocouple and drive point "A" with 4.06mV. Next, set the 1.5k trimmer for exactly 1000Hz output. Connect the thermocouple and the circuit is ready for use. Recalibration is not required if the thermocouple is replaced.

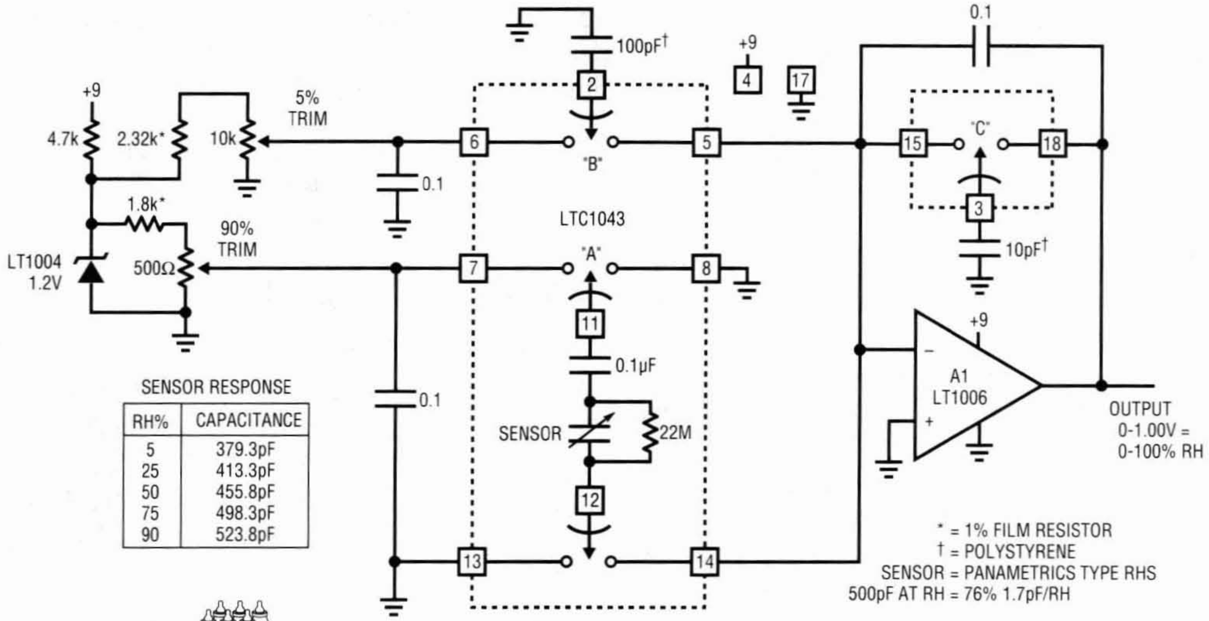
It is worth noting that this circuit can directly digitize any millivolt level signal by deleting the LT1025 thermocouple pair and directly driving point "A."

Relative Humidity Signal Conditioner

Relative humidity is a difficult physical parameter to transduce, and most transducers require fairly complex signal conditioning circuitry. Figure 15 combines simple circuitry with a capacitively based transducer to achieve good results. This circuit, which runs from a 9V battery, is accurate within 2% in the 5% to 90% relative humidity range.

The sensor specified has a nominal 500pF capacitance at RH = 76%, with a slope of 1.7pF/% RH. The average voltage across the device must be zero. This prevents deleterious electrochemical migration in the sensor. LTC1043 section "A," driven by an internal oscillator, alternately charges the sensor from a resistively scaled portion of the LT1004 reference and discharges it into A1's summing point. Note that the switching is arranged so that sensor related current flows out of A1's summing point. The 0.1μF series capacitor ensures the sensor sees the required zero average voltage, with the 22MΩ resistor preventing charge accumulation, which would stop current flow. The average current out of A1's summing point is balanced by packets of charge delivered by the LTC1043 switched capacitor section "C" in A1's feedback loop. The 0.1μF feedback capacitor gives A1 an integrator-like response, and its output is DC. As such, changes in sensor capacitance are seen as DC shifts in A1's output. A1 responds by raising its output positive to whatever DC potential is required to maintain its summing point at zero.

To allow 0% RH to equal 0V, offsetting is required. The signal and feedback terms biasing A1's summing point are expressed in charge form. Because of this, the offset must also be delivered to the summing point as charge, instead of a simple DC current. If this is not done, the circuit will be affected by drift in the LTC1043's internal oscillator. LTC1043 section "B" serves this function, delivering LT1004 referenced offsetting charge to A1.



SENSOR RESPONSE

RH%	CAPACITANCE
5	379.3pF
25	413.3pF
50	455.8pF
75	498.3pF
90	523.8pF

* = 1% FILM RESISTOR
† = POLYSTYRENE
SENSOR = PANAMETRICS TYPE RHS
500pF AT RH = 76% 1.7pF/RH

AN45 • TA15

Figure 15. Battery Powered Relative Humidity Signal Conditioner

Drift terms in this circuit include the LT1004 and the ratio stability of the sensor and the polystyrene capacitors. These terms are well within the sensor's 2% accuracy specification, and temperature compensation is not required. To calibrate this circuit, place the sensor in a 5% RH environment and set the "5% RH trim" for 50mV output. Next, place the sensor in a 90% RH environment and set the "90% trim" for 900mV output. Repeat this procedure until both points are fixed. If known RH environments are unavailable, the capacitance versus RH table in Figure 15 may be utilized, although it applies for an ideal sensor. The capacitor values may be built-up or directly dialed out on a precision variable air capacitor (General Radio #722D).

Inexpensive Precision Electronic Barometer

Until recently, precision electronically based pressure measurements required expensive transducers. Capacitive and bonded strain gauge based approaches provide unmatched results, but costs are often prohibitive. Additionally, if low power operation is desired, signal conditioning for these devices can become complex.

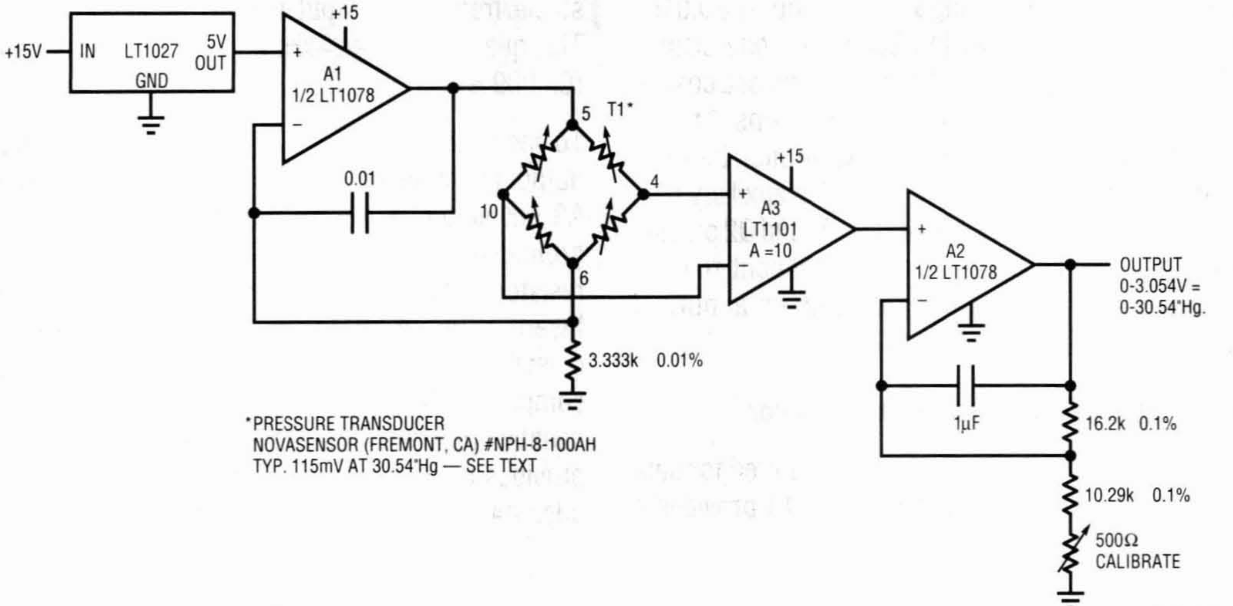
Semiconductor based pressure transducers becoming available offer significant improvement over earlier devices. Figure 16's circuit utilizes such a device to form a low cost barometer. The LT1027 reference and A1 form a current source to put precisely 1.5mA through transducer T1, in accordance with the manufacturer's specifications. Instrumentation amplifier A3 takes a differential gain of 10 from T1's bridge output. A2 provides additional gain to yield a calibrated output directly in inches of mercury.

T1's manufacturer specifies a nominal 115mV at full scale, although each device is supplied with precise calibration data. This information considerably simplifies calibration. To calibrate the circuit, simply adjust the potentiometer at A1 until the output corresponds to the scale factor supplied with the unit.

This circuit, compared to a long column mercury barometer, tracked ambient pressure variations from 29.75" to 30.32" over three months with only two counts of uncertainty. Additionally, over 50 turn-on/turn-off cycles had no measurable effect. Changes in pressure, particularly rapid ones, correlated quite nicely to changing weather conditions.

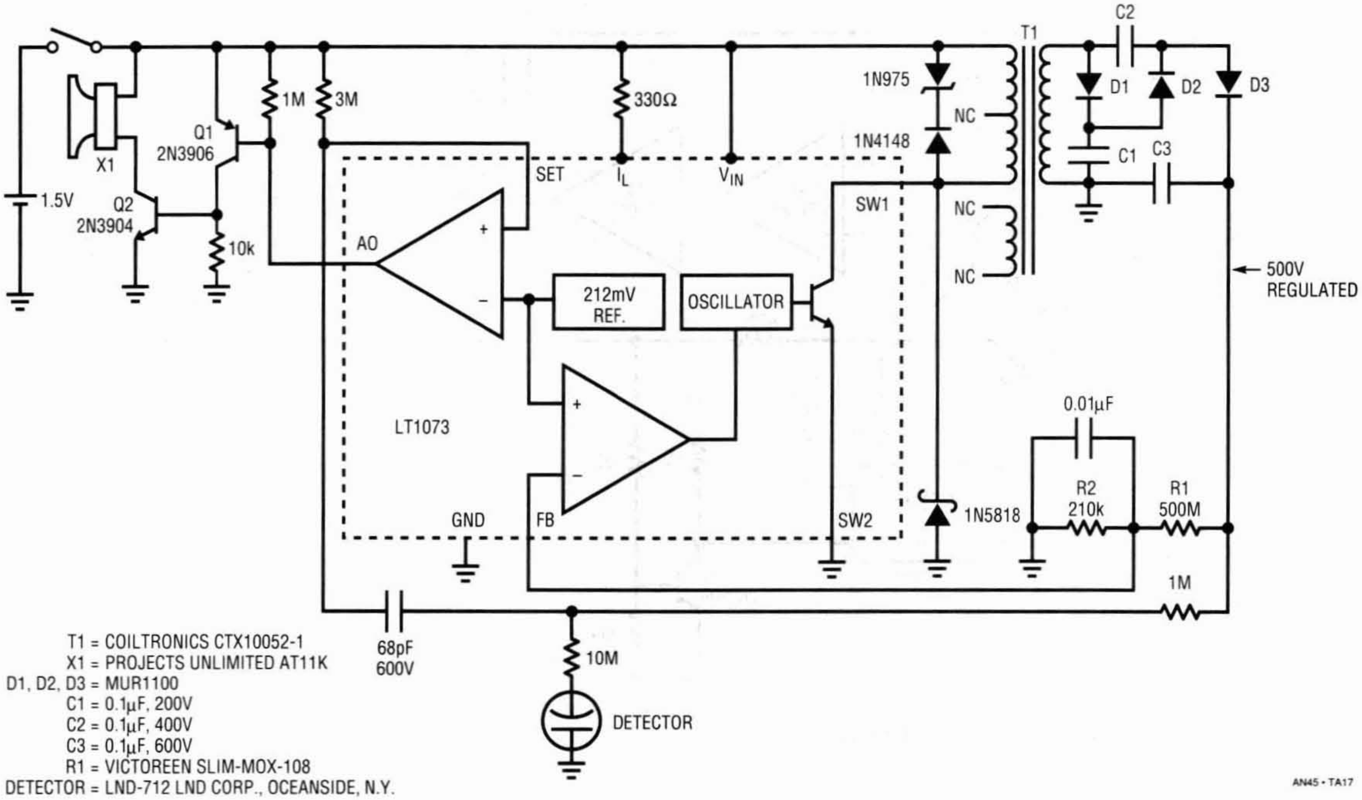
1.5V Powered Radiation Detector

Figure 17's circuit provides an audible "tick" signal each time radiation or a cosmic ray passes through the detector. The LT1073 switching regulator pulses T1. T1 takes gain via its turns ratio and drives a voltage tripler, providing 500V bias to the detector. R1 and R2 provide scaled


+15V
IN
LT1027
5V OUT
GND
+15
A1
1/2 LT1078
0.01
5
T1*
4
10
6
+15
A3
LT1101
A = 10
A2
1/2 LT1078
OUTPUT
0-3.054V =
0-30.54"Hg.
1µF
16.2k 0.1%
10.29k 0.1%
500Ω
CALIBRATE
3.333k 0.01%
AN45 • TA16

*PRESSURE TRANSDUCER
NOVASENSOR (FREMONT, CA) #NPH-8-100AH
TYP. 115mV AT 30.54"Hg — SEE TEXT

Figure 16. A Simple, Inexpensive Precision Barometer


1.5V
X1
Q1
2N3906
Q2
2N3904
10k
1M
3M
330Ω
SET
I_L
V_{IN}
AO
212mV REF.
OSCILLATOR
LT1073
GND
FB
SW1
SW2
1N975
1N4148
1N5818
T1
NC
NC
NC
C2
D1
D2
D3
C1
C3
500V REGULATED
0.01µF
R2
210k
R1
500M
1M
68pF
600V
10M
DETECTOR
AN45 • TA17

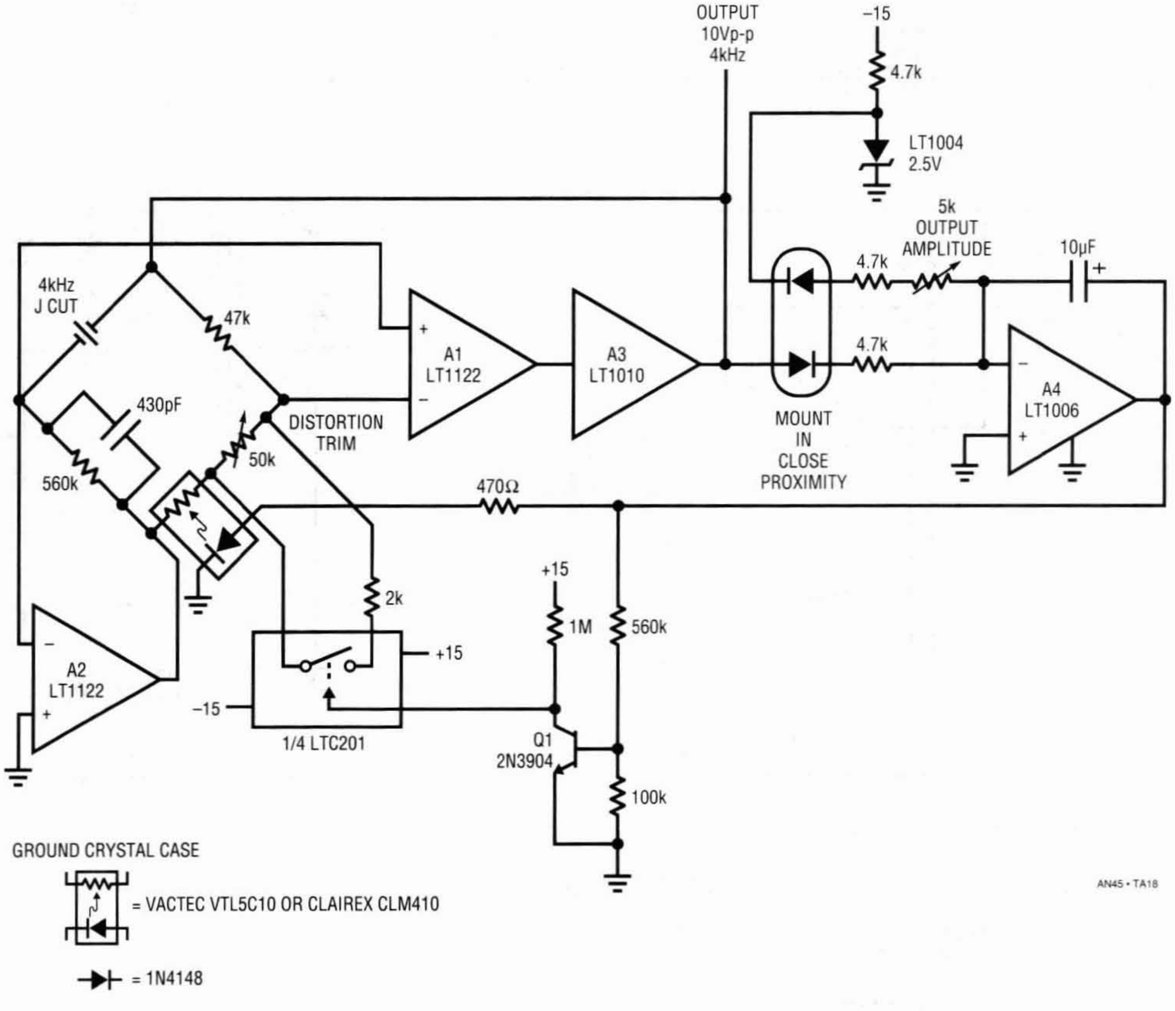
T1 = COILTRONICS CTX10052-1
X1 = PROJECTS UNLIMITED AT11K
D1, D2, D3 = MUR1100
C1 = 0.1µF, 200V
C2 = 0.1µF, 400V
C3 = 0.1µF, 600V
R1 = VICTOREEN SLIM-MOX-108
DETECTOR = LND-712 LND CORP., OCEANSIDE, N.Y.

Figure 17. 1.5V Powered Radiation Detector feedback to the LT1073, closing a control loop. The 0.01µF lag adds AC hysteresis and the Schottky diode clamps negative going T1 excursions. When radiation or a cosmic ray strikes the detector, impedance drops briefly, transferring a quick negative going spike through the 68pF capacitor. This spike triggers the LT1073's auxiliary gain block, configured here as a comparator. Q1 and Q2 provide additional gain to drive the audible beeper. About 10 to 15 cosmic rays per minute are recorded in a normal environment.

9ppm Distortion, Quartz Stabilized Oscillator

A spectrally pure sine wave oscillator is required for data converter, filter and audio testing. Figure 18 provides a stable frequency output with extremely low distortion. This quartz stabilized 4kHz oscillator has less than 9ppm (0.0009%) distortion in its 10Vp-p output.

To understand circuit operation, temporarily assume A2's output is grounded. With the crystal removed, A1 and the A3 power buffer form a non-inverting amplifier with a grounded input. The gain is set by the ratio of the 47k resistor to the 50k potentiometer — opto-isolator pair. Inserting the crystal closes a positive feedback path at the crystal's resonant frequency, and oscillations occur. A4 compares A3's positive peaks with the LT1004 2.5V negative reference. The diode in series with the LT1004 provides temperature compensation for A3's rectifier diode. A4 biases the LED portion of the opto-isolator,


OUTPUT
10Vp-p
4kHz
–15
4.7k
LT1004
2.5V
5k
OUTPUT
AMPLITUDE
10µF
4.7k
4.7k
4kHz
J CUT
47k
A1
LT1122
A3
LT1010
A4
LT1006
430pF
DISTORTION
TRIM
50k
560k
470Ω
MOUNT
IN
CLOSE
PROXIMITY
+15
2k
1M
560k
+15
A2
LT1122
–15
1/4 LTC201
Q1
2N3904
100k
AN45 • TA18

GROUND CRYSTAL CASE

= VACTEC VTL5C10 OR CLAIREX CLM410

= 1N4148

Figure 18. Quartz Stabilized 4kHz Oscillator with 9ppm Distortion

controlling the photoresistor's resistance. This sets loop gain to a value permitting stable amplitude oscillations. The 10µF capacitor stabilizes this amplitude control loop.

A2's function is to eliminate the common mode swing seen by A1. This dramatically reduces distortion due to A1's common mode rejection limitations. A2 does this by servo controlling the 560kΩ-photocell junction to maintain its negative input at 0V. This action eliminates common mode swing at A1, leaving only the desired differential signal.

Q1 and the LTC201 switch form a start-up loop. When power is first applied oscillations may build very slowly. Under these conditions A4's output saturates positive, turning on Q1. The LTC201 switch turns on, shunting the 2kΩ resistor across the 50kΩ potentiometer. This raises A1's loop gain, forcing a rapid build-up of oscillations. When oscillations rise high enough A4 comes out of saturation, Q1 and the switch go off and the loop functions normally.

The circuit is adjusted for minimum distortion by adjusting the 50kΩ potentiometer while monitoring A3's output with a distortion analyzer. This trim sets the voltage across the photocell to the optimum value for lowest distortion. The circuit's power supply should be well regulated and bypassed to ensure the distortion figures quoted.

After trimming, A3's output (trace A, Figure 19) contains less than 9ppm (0.0009%) distortion. Residual distortion components (trace B) include noise and second harmonic residue. Oscillation frequency, set by crystal tolerance, is typically within 50ppm with less than 2.5ppm/°C drift.

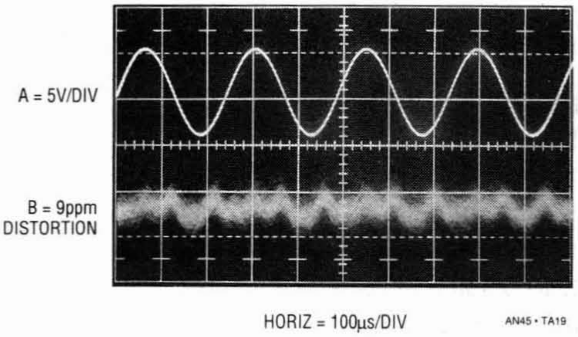


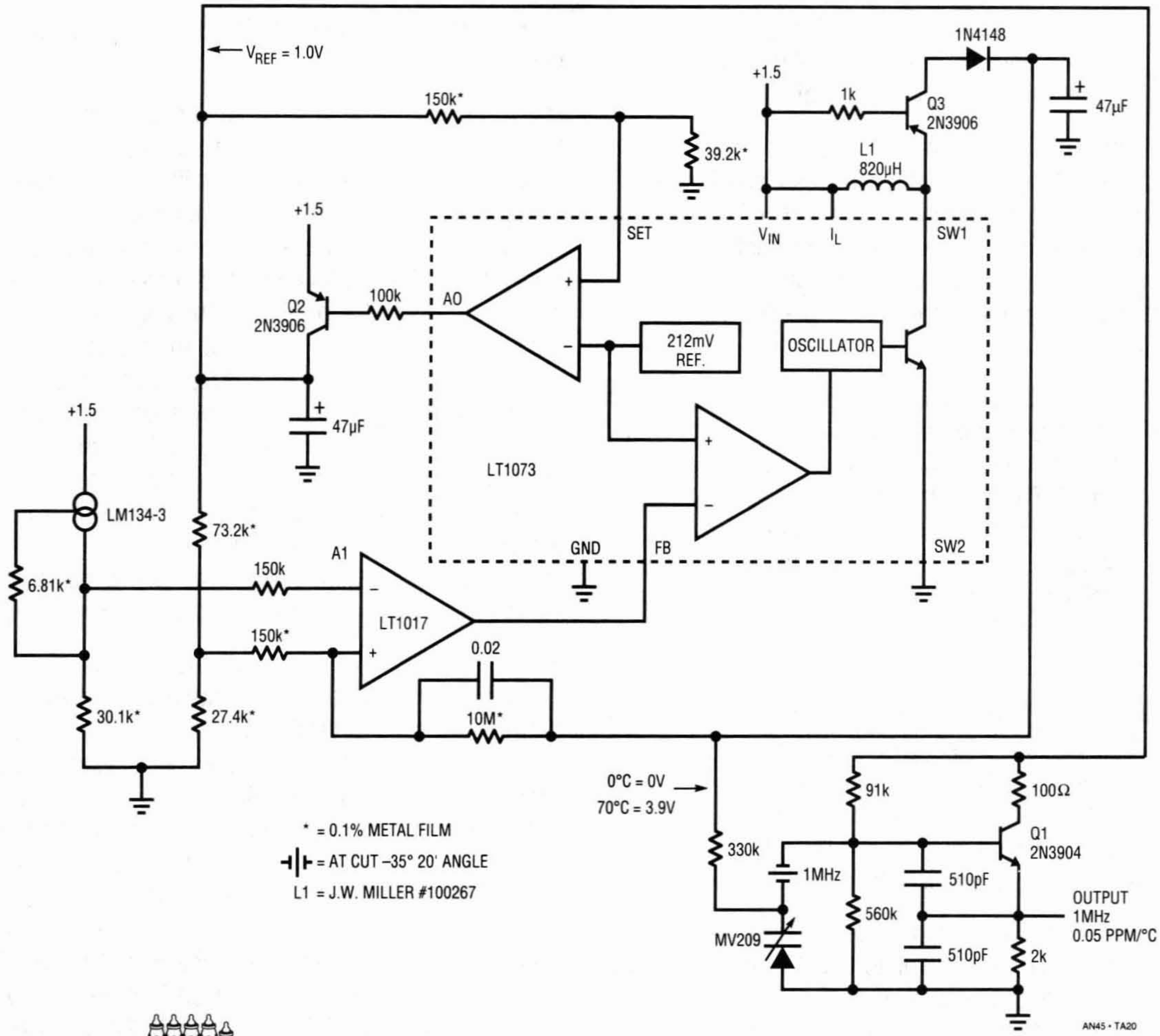
Figure 19. Oscillator Output and its 9ppm Distortion Residue

1.5V Powered Temperature Compensated Crystal Oscillator

Many single cell systems require a stable clock source. Crystal oscillators which run from 1.5V are relatively easy to construct. However, if good stability over temperature is required, things become more difficult. Ovenizing the crystal is one approach, but power consumption is excessive. An alternate method provides open loop, frequency correcting bias to the oscillator. The bias value is determined by absolute temperature. In this fashion, the oscillator's thermal drift, which is repeatable, is corrected. The simplest way to do this is by slightly varying the crystal's resonance point with a variable shunt or series impedance. Varactor diodes, the capacitance of which varies with reverse voltage, are commonly employed for this purpose. Unfortunately, these diodes require volts of reverse bias to generate significant capacitance shift, making direct 1.5V powered operation impossible.

Figure 20 improves the temperature stability of a 1.5V powered crystal oscillator by a factor of 20. It does this by slightly tuning the crystal's resonance as ambient temperature varies. Q1 and associated components form a 1MHz Colpitts oscillator which normally has a temperature coefficient of about 1ppm/°C. The remainder of the circuit implements the temperature correction. The LM134 senses ambient temperature, converting it to a current which flows through the 30.1k resistor. This resistor's voltage is subtracted from a reference potential by A1. The stable subtraction voltage is derived from the LT1073's 212mV reference via Q2 and the 73.2k-27.4k resistors. Feedback from Q2's collector to the LT1073's auxiliary amplifier closes the reference loop, which also powers the Colpitts oscillator. The 47µF capacitor frequency compensates the loop.

A1's output controls the remaining portion of the LT1073, which is configured as a voltage step-up switching regulator. L1's high voltage inductive events are rectified and stored in the 47µF output capacitor, resulting in a stepped-up DC potential. This potential is fed back to A1, closing a control loop. Because A1 is biased by the temperature sensitive LM134, the loop's output varies with ambient temperature in a controlled manner. Q3's drop forces the step-up converter to always run, regardless of the loop's required output voltage. This permits smooth and continuous varactor bias from 0 to 3.9V over a 0-70°C



V_REF = 1.0V
1N4148
+1.5
150k*
1k
Q3
2N3906
47µF
39.2k*
L1
820µH
+1.5
SET
V_IN
I_L
SW1
Q2
2N3906
100k
AO
212mV REF.
OSCILLATOR
+1.5
47µF
LT1073
LM134-3
73.2k*
A1
GND
FB
SW2
6.81k*
150k
150k*
LT1017
0.02
30.1k*
27.4k*
10M*
0°C = 0V
70°C = 3.9V
91k
100Ω
Q1
2N3904
* = 0.1% METAL FILM
= AT CUT –35° 20′ ANGLE
L1 = J.W. MILLER #100267
330k
1MHz
510pF
OUTPUT
1MHz
0.05 PPM/°C
560k
MV209
510pF
2k
AN45 • TA20

Figure 20. 1.5V Powered Temperature Compensated Crystal Oscillator

ambient operating environment. This output is applied to the varactor diode in the oscillator circuit. The varactor's capacitance, a function of its DC bias, thus varies with ambient temperature. This change in capacitance shifts the crystal's resonant frequency, opposing temperature induced crystal drift. For the values given in the circuit and the crystal cut specified, residual oscillator drift is only 0.05ppm/°C. This compares favorably with 1ppm/°C drift with no compensation used. The circuit functions from 1.7V down to 1.1V with no specification degradation. Current drain is only 230µA. Applications include portable high-accuracy clocks, survival radios, and secure communications.

90µA Precision Voltage-to-Frequency Converter

Figure 21 is a micropower voltage-to-frequency converter. A 0V-5V input produces a 0kHz-10kHz output with a linearity of 0.05%. Gain drift is 80ppm/°C. Maximum current consumption is only 90µA, almost 30 times lower than currently available V-F converters. To understand circuit operation, assume C1's positive input is slightly below its negative input (C2's output is low). The input voltage causes a positive going ramp at C1's positive input (trace A, Figure 22). C1's output is low, biasing the CMOS inverter output high. This allows current to flow from Q1's

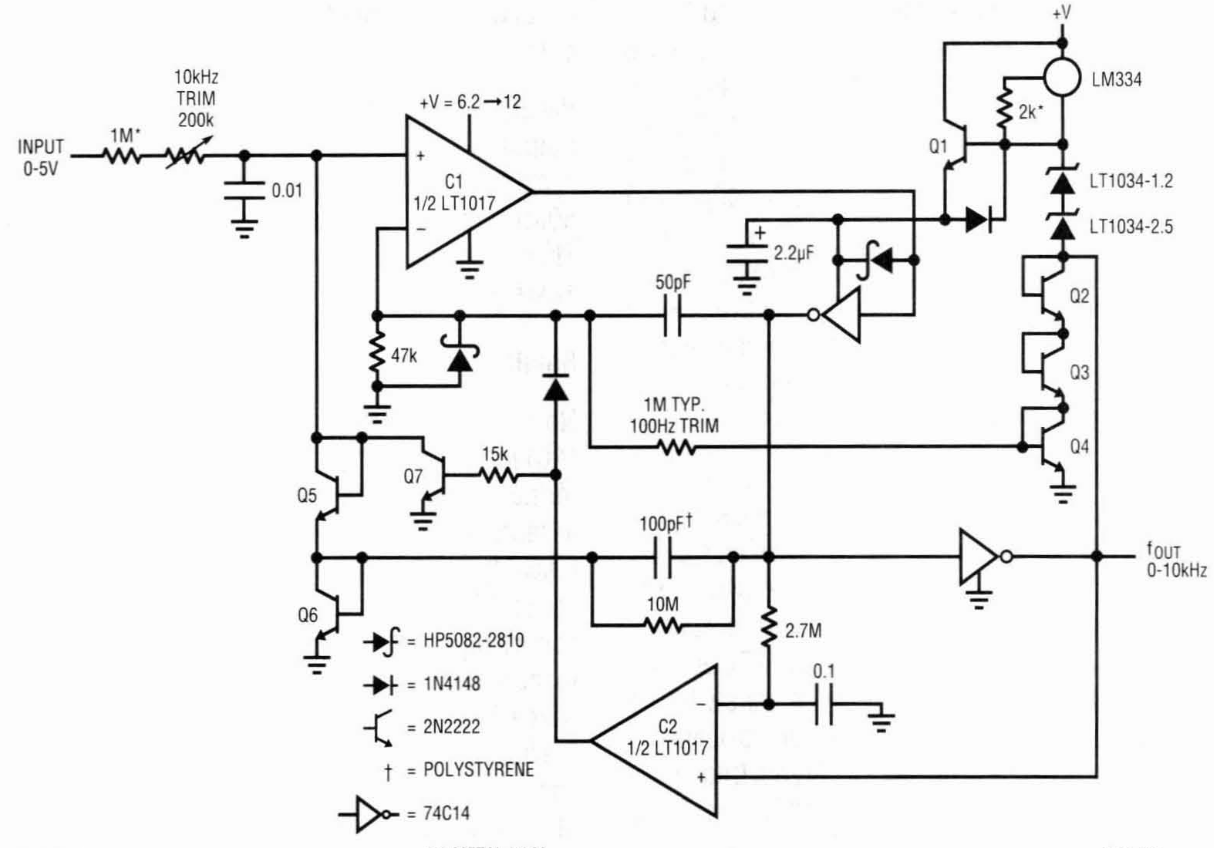

+V
LM334
2k*
Q1
LT1034-1.2
LT1034-2.5
Q2
Q3
Q4
10kHz
TRIM
200k
1M*
INPUT
0-5V
0.01
+V = 6.2 → 12
C1
1/2 LT1017
2.2µF
50pF
47k
1M TYP.
100Hz TRIM
15k
Q7
Q5
100pF†
10M
Q6
fOUT
0-10kHz
2.7M
0.1
C2
1/2 LT1017
= HP5082-2810
= 1N4148
= 2N2222
† = POLYSTYRENE
= 74C14
* = 1% METAL FILM
AN45 • TA21

Figure 21. V to F Converter Achieves 0.05% Linearity While Requiring Only 90µA Supply Current

emitter, through the inverter supply pin to the 100pF capacitor. The 2.2µF capacitor provides high frequency bypass, maintaining low impedance at Q1's emitter. Diode connected Q6 provides a path to ground. The 100pF unit charges to a voltage that is a function of Q1's emitter potential and Q6's drop. When the ramp at C1's positive input goes high enough, C1's output goes high (trace B) and the inverter switches low (trace C). The Schottky clamp prevents CMOS inverter input overdrive. This action pulls current from C1's positive input capacitor via the Q5-100pF route (trace D). This current removal resets C1's positive input ramp to a potential slightly below ground, forcing C1's output to go low. The 50pF capacitor furnishes AC positive feedback, ensuring that C1's output remains positive long enough for a complete discharge of the 100pF capacitor. The Schottky diode prevents C1's input from being driven outside its negative common mode limit. When the 50pF unit's feedback decays, C1 again switches low and the entire cycle repeats. The oscillation frequency depends directly on the input voltage derived current.

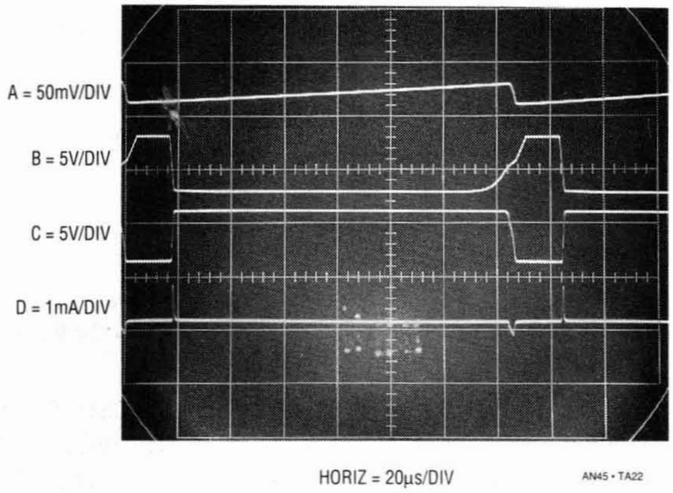


Figure 22. Micropower V to F Converter's Waveforms

Q1's emitter voltage must be carefully controlled to get low drive. Q3 and Q4 temperature compensate Q5 and Q6 while Q2 compensates Q1's V_{BE}. The two LT1034s are the actual voltage reference and the LM334 current source provides 35μA bias to the stack. The current drive provides excellent supply immunity (better than 40ppm/V) and also aids circuit temperature coefficient. It does this by utilizing the LM334's 0.3%/°C temperature coefficient to slightly temperature modulate the voltage drop in the Q2-Q4 trio. This correction's sign and magnitude directly oppose that of the –120ppm/°C, 100pF polystyrene capacitor, aiding overall circuit stability.

The Q1 emitter-follower efficiently delivers charge to the 100pF capacitor. Both base and collector current end up in the capacitor. The CMOS inverter provides low loss SPDT reference switching without significant drive losses. The 100pF capacitor draws only small transient currents during its charge and discharge cycles. The 50pF-47k positive feedback combination draws insignificantly small switching currents. Figure 23, a plot of supply current versus operating frequency, reflects the low power design. At zero frequency, the LT1017's quiescent current and the 35μA reference stack bias account for all current drain. There are no other paths for loss. As frequency scales-up, the charge/discharge cycle of the 100pF capacitor introduces the 1.5μA/kHz increase shown.

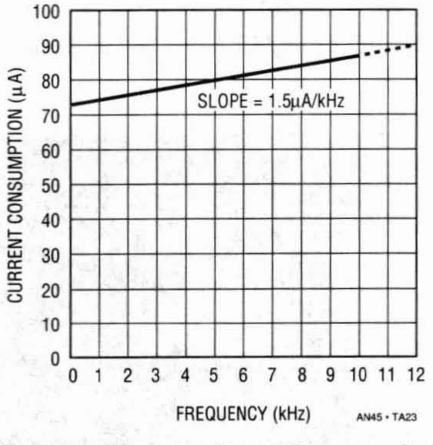


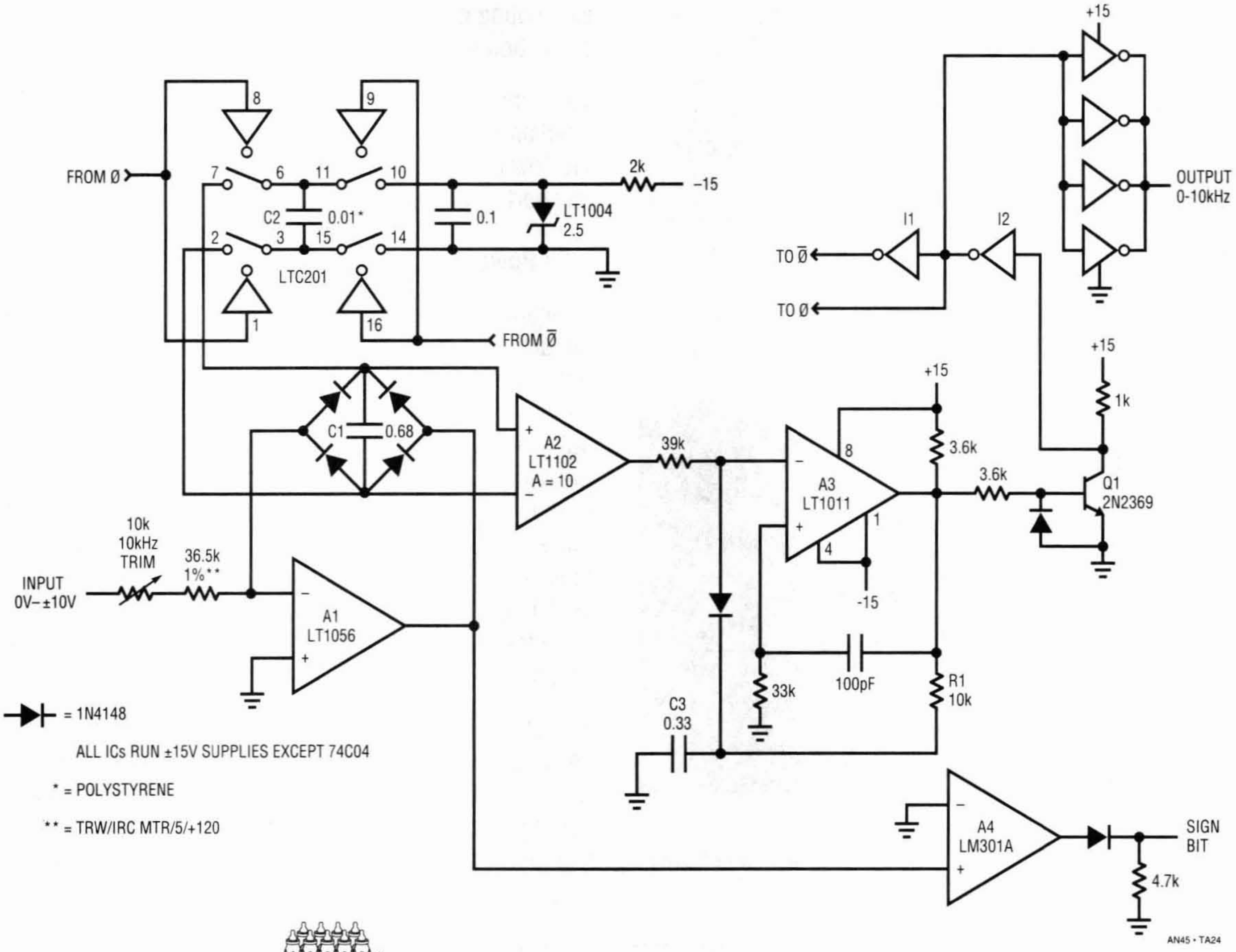
Figure 23. Current Consumption vs Frequency for the V to F Converter

Circuit start-up or overdrive can cause the circuit's AC-coupled feedback to latch. If this occurs, C1's output goes high. C2, detecting this via the inverter and the 2.7M-0.1μF lag, also goes high. This lifts C1's negative input and grounds the positive input with Q7, initiating normal circuit action.

Because the charge pump is directly coupled to C1's output, response is fast. The output settles within one cycle for a fast input step. To calibrate this circuit, apply 50mV and select the value at C1's input for a 100Hz output. Then, apply 5V and trim the input potentiometer for a 10kHz output.

Bipolar (AC) Input V-F Converter

No currently available V-F converter will accept bipolar (AC) inputs. This feature is desirable in power line monitoring and other applications. Figure 24's V-F converter accepts ±10V inputs, producing a 0kHz-10kHz output. Linearity is 0.04%, and temperature coefficient measures about 50ppm/°C. To understand circuit operation, assume a bipolar square wave (trace A, Figure 25) is applied to the input. During the input's positive phase, A1's output (trace B) swings negative, driving current through C1 via the full wave diode bridge. A1's current causes C1 to ramp linearly. Instrumentation amplifier A2, operating at a gain of 10, looks differentially across C1. A2's output (trace C) biases comparator A3's negative input. When A2's output crosses zero, A3 fires (trace D). AC positive feedback to A3's positive input (trace E) "hangs up" A3's output for about 20μs. The Q1 level shifter drives ground referred inverters I1 and I2 to deliver biphase drive (traces G and H) to the LTC201 switch. The LTC201, set-up as a charge pump, places C2 across C1 each time the inverters switch, resetting C1 to a lower voltage. The LT1004 reference, along with C2's value, determines how much charge is removed from C1 each time the charge pump cycles. Thus, each time A2's output tries to cross zero, C2 is switched across C1, resetting it to a small negative voltage and forcing A1 to begin recharging it. The frequency of this oscillatory behavior is directly proportional to the input derived current into A1. During the time C1 is ramping toward zero the LTC201 switches C2 across the LT1004, preparing it for the next discharge cycle. The action is the same for negative input excursions (see Figure 25), except that A1's output phasing is reversed. A2, looking differentially across A1's diode bridge, sees the same signal as for positive inputs and circuit action is identical. A4, detecting A1's output polarity, provides a sign bit output (trace F).



+15
8
9
FROM Ø
7
6
11
10
2k
−15
C2
0.01*
0.1
LT1004
2.5
2
3
15
14
LTC201
1
16
FROM Ø̅
OUTPUT
0-10kHz
I1
I2
TO Ø̅
TO Ø
+15
1k
+15
C1
0.68
A2
LT1102
A = 10
39k
A3
LT1011
8
3.6k
3.6k
Q1
2N2369
1
4
−15
10k
10kHz
TRIM
36.5k
1%**
INPUT
0V–±10V
A1
LT1056
100pF
33k
R1
10k
C3
0.33
= 1N4148
ALL ICs RUN ±15V SUPPLIES EXCEPT 74C04
* = POLYSTYRENE
** = TRW/IRC MTR/5/+120
A4
LM301A
SIGN
BIT
4.7k
AN45 • TA24

Figure 24. Bipolar (AC) Input V to F Converter

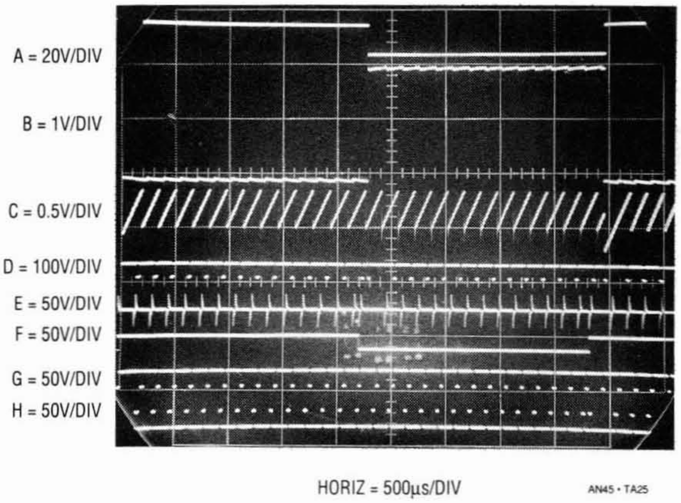


Figure 25. Waveforms for the Bipolar Input V to F Converter

Figure 26, an amplitude expanded version of A1 and A2's outputs, shows detail. Trace A is the input, while trace B and trace C are A1 and A2's outputs, respectively. Complementary bias points and ramping action are clearly visible in A1's output, while A2 responds identically for both input phases. A1's output bias points are established by the two conducting bridge diodes. When the input switches polarity, A1 responds immediately and oscillation frequency settles within 1 to 2 cycles of final value.

Start-up or overdrive conditions could cause this loop to latch. A start-up mechanism, adapted from oscilloscope trigger circuitry, precludes latch-up.[2] If C1 charges past the point where C2 can reset it, loop closure ceases. A2's

---

Note 2: See References 5 and 6.

output saturates positive, causing A3 to go negative. A3's prolonged negative state, detected by the R1-C3 filter, pulls its negative input toward –15V. When A3's negative input crosses zero, its output changes state and charges R1-C3 positively. A3's input rises above zero, causing output reversal and free-running oscillation commences. As in normal mode, the 100pF-33k RC aids transitions. A3's oscillations are transmitted to the LTC201 based charge pump via A1 and the inverters. C2 pumps charge out of C1, driving the voltage across it toward zero. A2 comes out of positive saturation and heads negative, eliminating positive bias at A3's input. A3's free-running oscillation stops, and normal loop action begins.

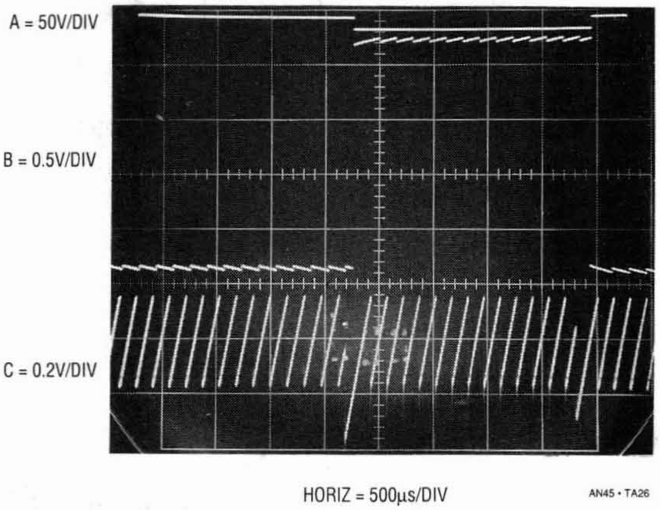


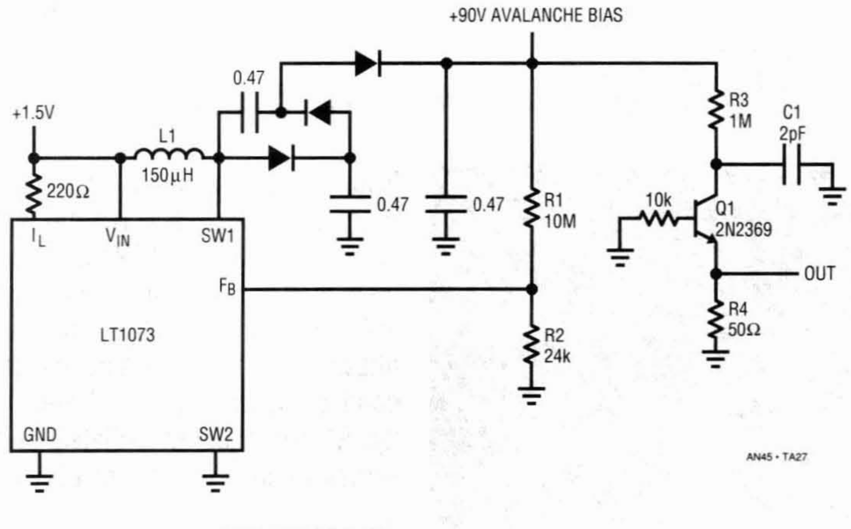
Figure 26. Detail of Integrator and Differential Amplifier Outputs

To calibrate this circuit apply either a –10V or a +10V input and set the 10kΩ trimmer for exactly 10kHz output. The low offsets of A1 and A2 permit operation down to a few hertz with no zero trim required.

1.5V Powered, 350ps Rise Time Pulse Generator

Verifying the rise time limit of wideband test equipment set-ups is a difficult task. In particular, the "end-to-end" rise time of oscilloscope-probe combinations is often required to assure measurement integrity. Conceptually, a pulse generator with rise times substantially faster than the oscilloscope-probe combination can provide this information. Figure 27's circuit does this, providing a 1ns pulse with rise and fall times inside 350ps. Pulse amplitude is 10V with a 50Ω source impedance. This circuit, built into a small box and powered by a 1.5V battery, provides a simple, convenient way to verify the rise time capability of almost any oscilloscope-probe combination.

The LT1073 switching regulator and associated components supply the necessary high voltage. The LT1073 forms a flyback voltage boost regulator. Further voltage step-up is obtained from a diode-capacitor voltage doubler network. L1 periodically receives charge, and its



L1 = TOKO #262-LYF-0095K
—▶|— = MUR120
SELECT Q1 AND 2pF VALUE — SEE TEXT

Figure 27. 350ps Rise Time Pulse Generator

flyback discharge delivers high voltage events to the doubler network. A portion of the doubler network's DC output is fed back to the LT1073 via the R1, R2 divider, closing a control loop.

The regulator's 90V output is applied to Q1 via the R3-C1 combination. Q1, a 40V breakdown device, non-destructively avalanches when C1 charges high enough.[3] The result is a quickly rising, very fast pulse across R4. C1 discharges, Q1's collector voltage falls and breakdown ceases. C1 then recharges until breakdown again occurs. This action causes free-running oscillation at about 200kHz. Figure 28 shows the output pulse. A 1GHz sampling oscilloscope (Tektronix 556 with 1S1 sampling plug-in) measures the pulse at 10V high with about a 1ns base. Rise time is 350ps, with fall time also indicating 350ps. The figures may actually be faster, as the 1S1 is specified with a 350ps rise time limit.[4]

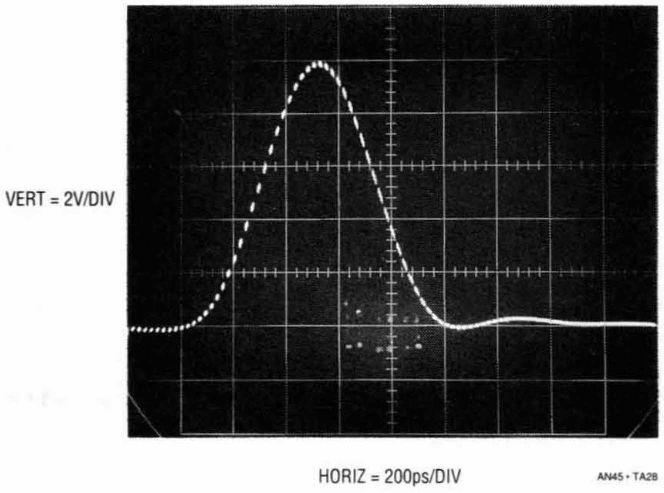
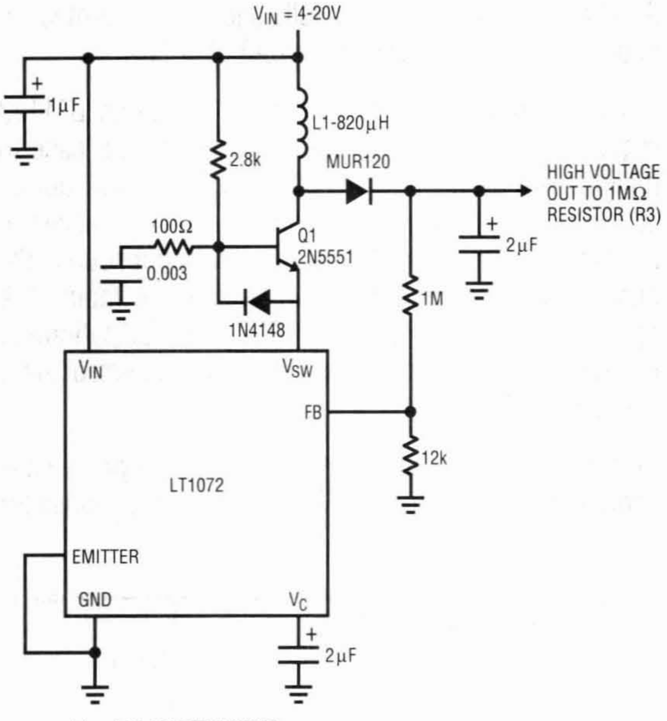


Figure 28. Avalanche Pulse Generator Output Pulse. Waveform Has 350ps Rise and Fall Times. Slightly Under Damped Turn-Off is Probably Due to Test Fixture Limitations

Q1 may require selection to get avalanche behavior. Such behavior, while characteristic of the device specified, is not guaranteed by the manufacturer. A sample of 50 Motorola 2N2369s, spread over a 12 year date code span, yielded 82%. All "good" devices switched in less than 600ps. C1 is selected for a 10V amplitude output. Value spread is typically 2pF to 4pF. Ground plane type construction with high speed layout techniques are essential for good results from this circuit. Current drain from the 1.5V battery version is about 5mA.



L1 = J. W. MILLER #100267

Figure 29. Alternate 90V DC-DC Converter

For those applications which must run from higher voltage inputs, Figure 29 is included. This circuit, which operates from inputs of 4V to 20V, will also power the avalanche stage. Cascoded high voltage transistor Q1 combines with the LT1072 switching regulator to form a high voltage switched mode control loop. The LT1072 pulse width modulates Q1 at its 40kHz clock rate. L1's inductive events are rectified and stored in the 2µF output capacitor. The 1MΩ-12kΩ divider provides feedback to the LT1072. The diode and RC at Q1's base damp inductor related parasitic behavior. The circuit's output drives the avalanche stage in similar fashion to the LT1073 based circuit.

A Simple Ultra-Low Dropout Regulator

Switching regulator post regulators, battery powered apparatus, and other applications frequently require low dropout linear regulators. Often, battery life is significantly affected by the regulator's dropout performance. Figure 30's simple circuit offers lower dropout voltage than any monolithic regulator. Dropout is below 50mV at 1A, increasing to only 450mA at 5A. Line and load regulation are within 5mV, and initial output accuracy is inside 1%.

Note 3: See Reference 7.
Note 4: I'm sorry, but 1GHz is the fastest scope in my house.

Additionally, the regulator is fully short circuit protected, and has a no load quiescent current of 600µA.

Circuit operation is straightforward. The 3-pin LT1123 regulator (TO-92 package) servo controls Q1's base to maintain its feedback pin (FB) at 5V. The 10µF output capacitor provides frequency compensation. If the circuit is located more than six inches from the input source, the optional 10µF capacitor should bypass the input. The optional 20Ω resistor limits LT1123 power dissipation and is selected based upon the maximum expected input voltage (see Figure 31).

Normally, configurations of this type offer unpredictable short circuit protection. Here, the MJE1123 transistor shown has been specially designed for use with the LT1123. Because of this, beta based current limiting is practical. Excessive output current causes the LT1123 to pull down harder on Q1 until beta limiting occurs. Under these conditions the controlled pull down current combines with Q1's beta and safe operating area characteristics to provide reliable short circuit limiting. Figure 32 details current limit characteristics for 30 randomly selected transistors.

Figure 33 shows dropout characteristics. Even at 5A, dropout is about 450mV, decreasing to only 50mV at 1A. Monolithic regulators cannot approach these figures, primarily because monolithic power transistors do not offer

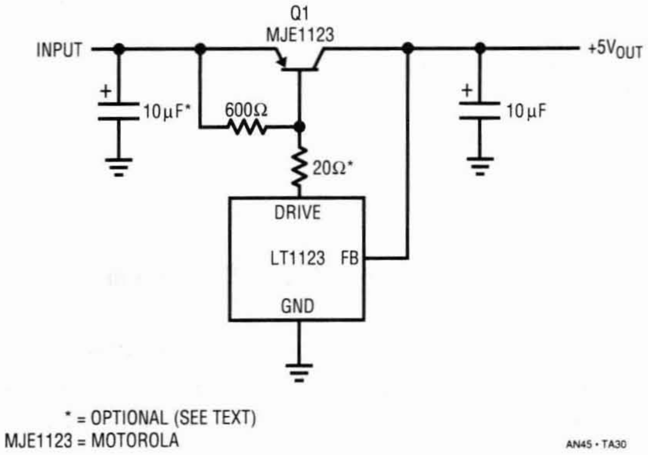


Figure 30. The Ultra-Low Dropout Regulator. LT1123 Combines with Specially Designed Transistor for Low Dropout and Short Circuit Protection

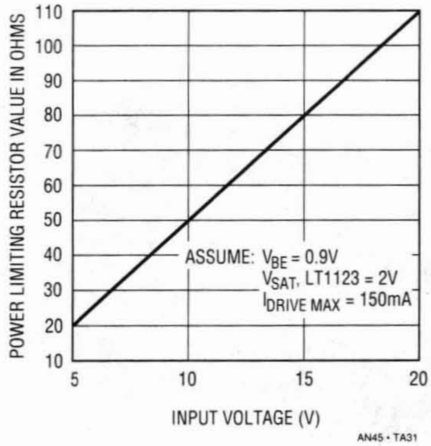


Figure 31. LT1123 Power Dissipation Limiting Resistor Value vs Input Voltage

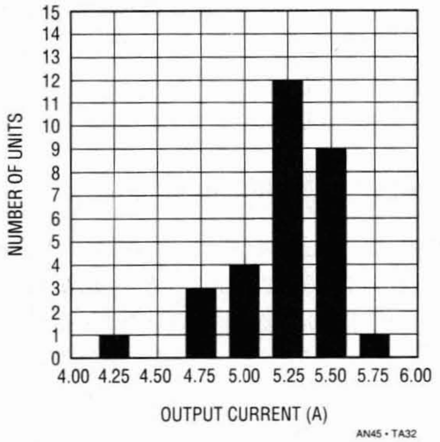


Figure 32. Short Circuit Current for 30 Randomly Selected MJE1123 Transistors at V_{IN} = 7V

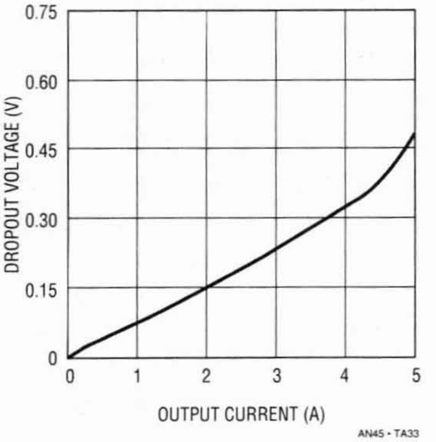


Figure 33. Dropout Voltage vs Output Current

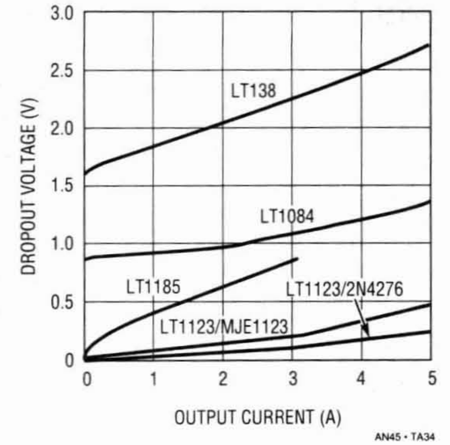


Figure 34. Dropout Voltage vs Output Current for Various Regulators

Q1's combination of high beta and excellent saturation. For comparison, Figure 34 compares the circuit's performance against some popular monolithic regulators. Dropout is 10 times better than 138 types, and significantly better than the other types shown. Because of Q1's high beta, base drive loss is only 1%-2% of output current, even at full 5A output. This maintains high efficiency under the low $V_{IN} - V_{OUT}$ conditions the circuit will typically operate at. As an exercise, the MJE1123 was replaced with a 2N4276, a Germanium device. This combination provided even lower dropout performance, although current limit characteristics cannot be guaranteed.

Figure 35 shows a simple way to add shutdown to the regulator. A CMOS inverter or gate biases Q2 to control LT1123 bias. When Q2's base is driven, the loop functions normally. With Q2 unbiased, the circuit goes into shutdown and pulls no current.

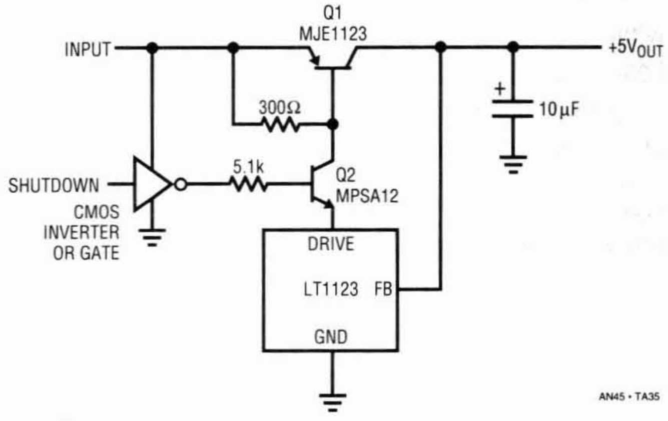
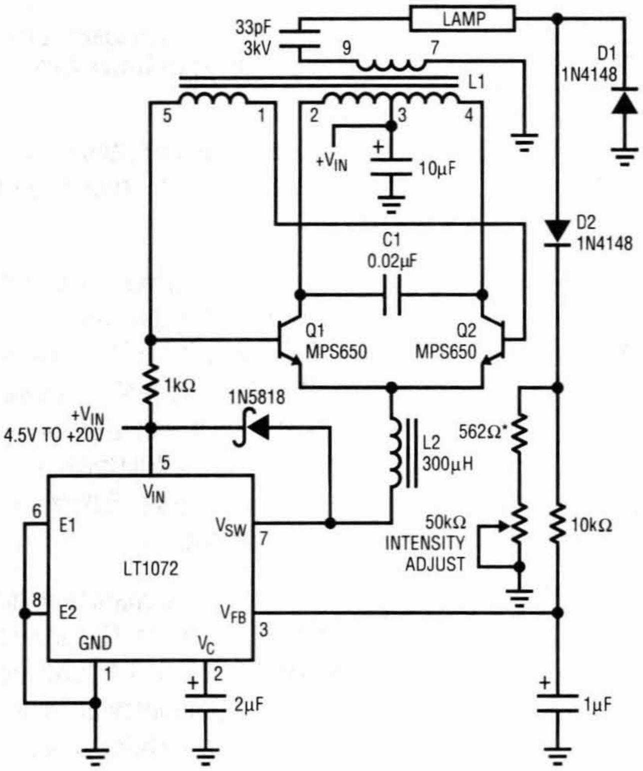

INPUT
Q1
MJE1123
+5V_OUT
300Ω
10μF
SHUTDOWN
CMOS
INVERTER
OR GATE
5.1k
Q2
MPSA12
DRIVE
LT1123
FB
GND
AN45 • TA35

Figure 35. Shutdown for the Low Dropout Regulator

Cold Cathode Fluorescent Lamp Power Supply

Current generation portable computers utilize back-lit LCD displays. Cold Cathode Fluorescent Lamps (CCFL) provide the highest available efficiency for back-lighting the display. These lamps require high voltage AC to operate, mandating an efficient, high voltage DC-AC converter. In addition to good efficiency, the converter should deliver the lamp drive in the form of a sine wave. This is desirable to minimize RF emissions. Such emissions can cause interference with other devices, as well as degrading overall operating efficiency.

Figure 36 meets these requirements. Efficiency is 78%, with an input voltage range of 4.5V-20V. 82% efficiency is possible if the LT1072 is driven from a low voltage (e.g., 3V-5V) source. Additionally, lamp intensity is continuously and smoothly variable from zero to full intensity.


33pF
3kV
LAMP
9
7
L1
D1
1N4148
5
1
2
3
4
+V_IN
10μF
D2
1N4148
C1
0.02μF
Q1
MPS650
Q2
MPS650
1kΩ
1N5818
+V_IN
4.5V TO +20V
L2
300μH
562Ω*
5
V_IN
6
E1
V_SW
7
50kΩ
INTENSITY
ADJUST
10kΩ
LT1072
8
E2
V_FB
3
GND
V_C
1
2
2μF
1μF
AN45 • TA36

C1 = MUST BE A LOW LOSS CAPACITOR.
METALIZED POLYCARB
WIMA FKP2 (GERMAN) RECOMMENDED.
L1 = SUMIDA-6345-020 OR COILTRONICS-CTX110092-1.
PIN NUMBERS SHOWN FOR COILTRONICS UNIT
L2 = COILTRONICS-CTX300-4
* = 1% FILM RESISTOR
DO NOT SUBSTITUTE COMPONENTS

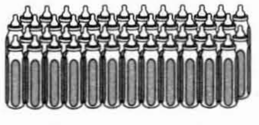


Figure 36. Cold Cathode Fluorescent Lamp Power Supply

When power is applied the LT1072 switching regulator's feedback pin is below the devices internal 1.23V reference, causing full duty cycle modulation at the V_{SW} pin (trace A, Figure 37). L2 conducts current (trace B), which flows from L1's center tap, through the transistors, into L2. L2's current is deposited in switched fashion to ground by the regulator's action.

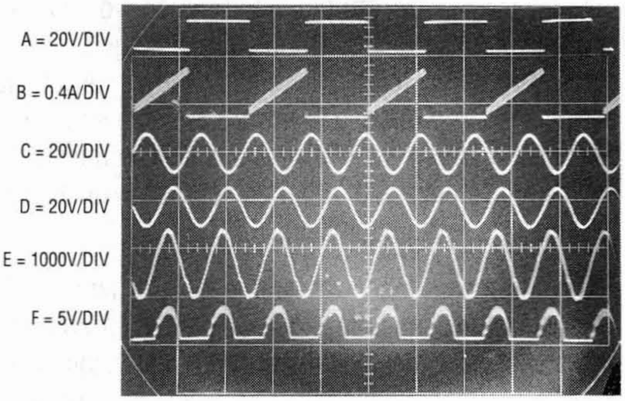


Figure 37. Waveforms for the Cold Cathode Fluorescent Lamp Power Supply. Note Independent Triggering on Traces A and B and C Through F.

L1 and the transistors comprise a current driven Royer class converter[5] which oscillates at a frequency primarily set by L1's characteristics and the 0.02µF capacitor. LT1072 driven L2 sets the magnitude of the Q1-Q2 tail current, and hence L1's drive level. The 1N5818 diode maintains L2's current flow when the LT1072 is off. The LT1072's 40kHz clock rate is asynchronous from the Royer converters (≈60kHz) rate, accounting for trace B's waveform thickening.

The 0.02µF capacitor combines with L1's characteristics to produce sine wave voltage drive at the Q1 and Q2 collectors (traces C and D, respectively). L1 furnishes voltage step-up, and about 1400Vp-p appears at its secondary (trace E). Current flows through the 33pF capacitor into the lamp. On negative waveform cycles the lamp's current is steered to ground via D1. Positive waveform cycles are directed, via D2, to the ground referred 562Ω-50k potentiometer chain. The positive half-sine appearing across these resistors (trace F) represents 1/2 the lamp current. This signal is filtered by the 10k-1µF pair and presented to the LT1072's feedback pin. This connection closes a control loop which regulates lamp current. The 2µF capacitor at the LT1072's V_C pin provides stable loop compensation. The loop forces the LT1072 to switch-mode modulate L2's average current to whatever value is required to maintain a constant current in the lamp. The constant current's value, and hence lamp intensity, may be varied with the potentiometer. The constant current drive allows full 0-100% intensity control with no lamp dead zones or "pop-on" at low intensities. Additionally, lamp life is enhanced because current cannot increase as the lamp ages.

Several points should be kept in mind when observing this circuit's operation. L1's high voltage secondary can only be monitored with a wideband, high voltage probe fully specified for this type of measurement. *The vast majority of oscilloscope probes will break down and fail if used for this measurement.*[6] Tektronix probe type P-6009 (acceptable) or types P6013A and P6015 (preferred) probes must be used to read L1's output.

Another consideration involves observing waveforms. The LT1072's switching frequency is completely asynchronous from the Q1-Q2 Royer converter's switching. As such, most oscilloscopes cannot simultaneously trigger and display all the circuit's waveforms. Figure 37 was obtained using a dual beam oscilloscope (Tektronix 556). LT1072 related traces A and B are triggered on one beam, while the remaining traces are triggered on the other beam. Single beam instruments with alternate sweep and trigger switching (e.g., Tektronix 547) can also be used, but are less versatile and restricted to four traces.

Note 5: See Reference 8.
Note 6: Don't say we didn't warn you!

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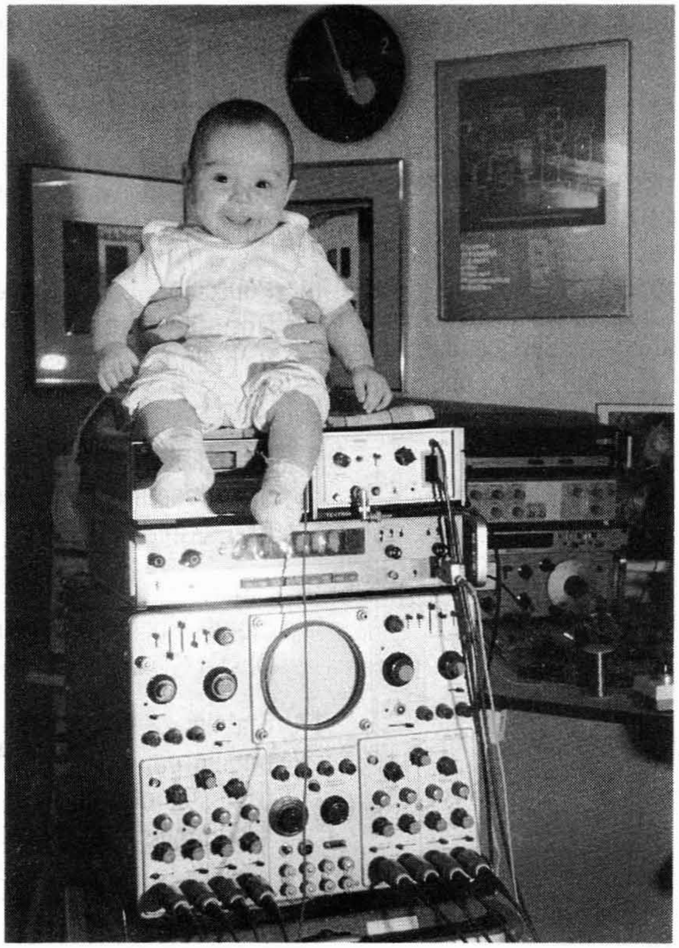


Application Note 46
November 1991

Efficiency and Power Characteristics of Switching Regulator Circuits

Brian Huffman

Efficiency is often the main objective when using switching regulators. High efficiency means less power drain on the input source (batteries, etc.) and less heat buildup around the regulator, allowing for smaller and lighter power supplies and system enclosures. Practical switching regulator efficiencies typically range from 70%-90%. The highest possible efficiency is desired when battery life is critical or when package size restrictions preclude effective heat removal.

Since switching power supplies are not 100% efficient, the lost power is dissipated as heat. Losses fall into a variety of categories including switching transistors, clamp diodes, filter capacitors, controllers, and inductors. Excessive temperature rise in any of these elements can stress the power supply leading to premature failure. Therefore, proper thermal design is essential for reliable operation of switching supplies.

Calculating the power loss and selecting the proper heat sink or package size for each switching regulator component is not a trivial task. Many variables influence power loss: circuit switching characteristics, DC and AC component characteristics, input and output voltages and load currents. Furthermore, power device contribution to efficiency loss varies with circuit configuration.

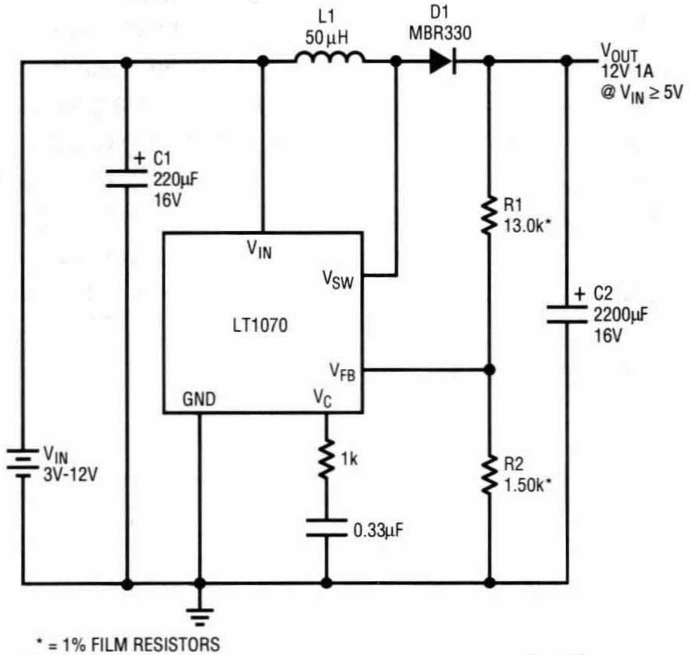
To satisfy design requirements various switching regulator approaches are possible. Before selecting the appropriate circuit, a review of the following considerations is useful.

- Input Voltage Range
- Output Voltage
- Maximum Output Current
- Efficiency
- Form Factor
- Maximum and Minimum Temperature Range
- Price

Efficiency varies widely between switching regulator architectures, input voltage and output load conditions. Therefore, efficiency plots for various input and output conditions accompany each circuit discussed in this application note, allowing comparisons. Squeezing the utmost efficiency out of a switching regulator requires that power components be selected properly. Trade-offs between circuit complexity and efficiency influence final circuit selection.

Basic Step-Up Switching Regulator

A common switching regulator requirement involves converting a lower voltage to a higher voltage. Figure 1 shows a basic step-up switching regulator. The LT1070 is a fully self-contained switching regulator that controls its internal switching transistor current to achieve output voltage regulation.



* = 1% FILM RESISTORS
D1 = MOTOROLA - MBR330
C1 = NICHICON - UPL1C221MPH
C2 = NICHICON - UPL1C222MRH
L1 = COILTRONICS - CTX50-5-52

(EQ1) $V_{OUT} = 1.24V\left(1+\frac{R1}{R2}\right)$

LTAN46 • TA01

Figure 1. LT1070 Step-Up Switching Regulator

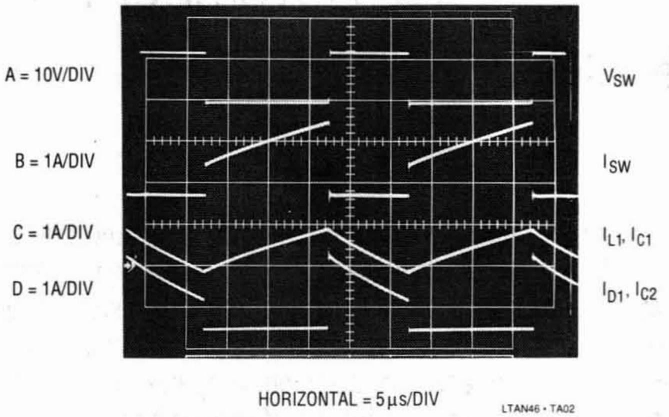


Figure 2. LT1070 Step-Up Converter Waveforms[1]

Figure 2 shows regulator operating waveforms. Since the LT1070 has a ground referred power switch, the input voltage is applied across the inductor when it is on. Trace A is the V_{SW} pin voltage and trace B is its current. The inductor current (trace C) rises very slowly as the magnetic field builds up. The rate of change of the current is determined by the voltage applied across the inductor and its inductance. During this interval energy is being stored in the inductor and no power is transferred to the output. When the switch is turned off, energy is no longer transferred to the inductor causing the magnetic field to collapse. The collapsing magnetic field induces a change in voltage across the inductor. The V_{SW} pin voltage rises until clamp diode D1 forward biases. The diode current (trace D) is distributed between the load and the output capacitor. When the diode is reverse biased, the output capacitor provides the load current. The 1% resistors control the regulator's feedback loop, setting output voltage. The RC network at the V_C pin provides loop compensation. Figure 3 shows the maximum output current for various input voltages and power devices.

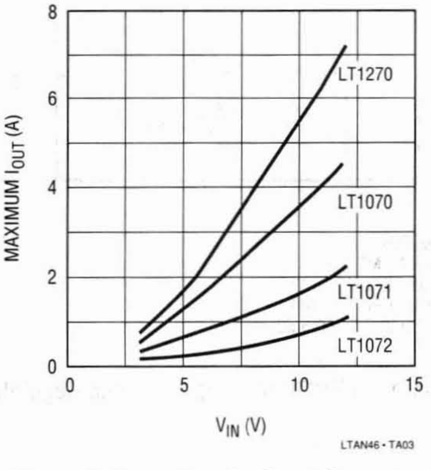


Figure 3. V_{IN} vs I_{OUT} for Boost Converter

Trace C is the input capacitor's (C1) current waveform. Capacitor current ramps up when the inductor is storing energy and down when the energy is transferred to the load. The input capacitor provides a low resistance AC return path for the inductor current during switch on and off times. Because of this, both the input capacitor and inductor have the same current waveform.

Trace D is the output capacitor's (C2) current waveform. The output capacitor's waveform is different than the input capacitor's. The output capacitor's current waveform ramps down when charging and goes flat when providing current to the load. The capacitor's ripple current waveform is often misinterpreted. The waveform shows peak to peak current. Capacitor current flows in both directions; into the capacitor when charging and out when discharging. The average capacitor current is zero, but its RMS value is not. Appendix B explains capacitor current waveforms in greater detail.

Figure 4 shows that efficiency for this circuit generally exceeds 75%.

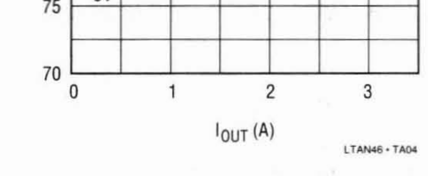


Figure 4. LT1070 Boost Converter Efficiency for Various Input Voltages and Load Currents

Semiconductor Losses

The output diode is often a major source of power loss in switching regulators, especially with output voltages below 10V. Inherent forward conduction losses limit the

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Note 1: Switching Regulator and DC-DC Converter are used interchangeably in this text.

diode's overall efficiency. For output voltages below 10V, Schottky switching diodes are recommended for their minimum forward voltage drop and fast recovery time characteristics. A Schottky rectifier, with a typical V_f of 0.5V, introduces a loss of 4% for a 12V output and 10% in a 5V output. Its low peak inverse voltage rating limits use to low voltage applications. In higher output voltage applications the silicon diode forward voltage loss is less significant, because the diode's DC loss is a much smaller percent of the total loss.

Another loss element is the LT1070's switching transistor and its control circuitry. The bulk of this power loss is due to the switching transistor's conduction losses. Switch conduction loss includes both actual switch saturation and driver circuitry losses. The internal power switch is a bipolar device with a forced beta of 40. At low input voltage and high switch currents, switch saturation losses dominate with driver losses dominating under converse conditions. Only at light load does the controller's quiescent current significantly affect efficiency.

Capacitor Losses and Considerations

Filter capacitors, if chosen properly, dissipate only a few hundred milliwatts under worse case operating conditions adding very little to overall power loss. The primary concern when choosing a filter capacitor is its RMS ripple current rating. The ripple current rating is selected to limit temperature rise in the capacitor. Capacitors must be kept within manufacturer's ripple current specifications for efficient operation and long lifetime. Power dissipation can be determined by multiplying the capacitor's Effective Series Resistance (ESR) by the square of the RMS current. Physically larger capacitors have higher RMS current ratings than smaller capacitors since they have lower ESR and more surface area to dissipate heat. Another alternative is to parallel several smaller capacitors to achieve low ESR and acceptable component height. Appendix A discusses thermal consideration for aluminum electrolytic capacitors.

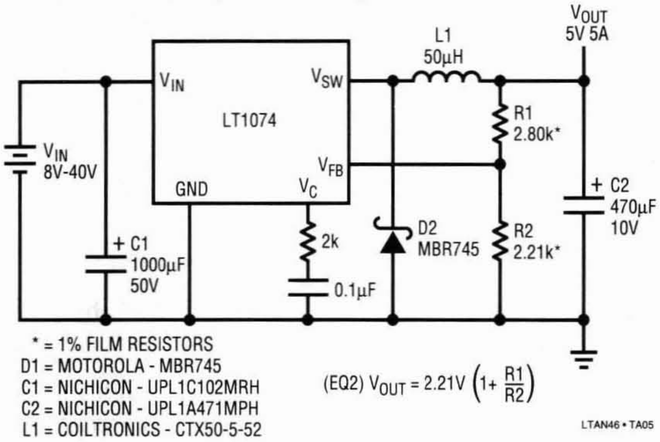
RMS current can vary significantly between input and output capacitors. For the boost circuit, the input capacitor RMS current is 400mA RMS, while the output capacitor is 1.3A RMS for a 1A load. Therefore, the output capacitor has to be larger than the input capacitor to handle the current. Appendix B details RMS current measuring techniques.

Inductor Loss Factors

A properly designed inductor will degrade efficiency by only a small percentage. Inductor losses are broken up into two categories: wire loss (copper loss) and core loss. Trade-offs associated with wire size, inductor value, core volume and core material influence final selection. Power loss in the copper wire only becomes significant at high current levels, since it is proportional to the square of the RMS current. Inductor losses also vary widely for different core materials and input voltages.

Basic Step-Down Switching Regulator

Many regulator requirements involve converting a higher voltage into a lower voltage. Although a linear regulator can do this, it cannot achieve the efficiency of switching regulator-based designs. Figure 5 shows a practical step-down switching regulator using the LT1074.



* = 1% FILM RESISTORS
D1 = MOTOROLA - MBR745
C1 = NICHICON - UPL1C102MRH
C2 = NICHICON - UPL1A471MPH
L1 = COILTRONICS - CTX50-5-52

(EQ2) $V_{OUT} = 2.21V\left(1+\frac{R1}{R2}\right)$

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Figure 5. LT1074 Positive Step-Down Switching Regulator

The operating waveforms for this circuit are shown in Figure 6. When the LT1074's high side switch turns on it pulls the V_{SW} pin to within 2.0V of the positive rail. Trace A is the V_{SW} pin voltage and trace B its current. During this period current flows from the input through the LT1074 and the inductor, and into the load. Inductor current is shown in trace C. When the LT1074 power switch turns off, the V_{SW} pin voltage drops until clamp diode D1 forward biases (trace D) providing a path for the inductor to transfer its energy to the output. Figure 7 shows maximum output current for various input conditions.

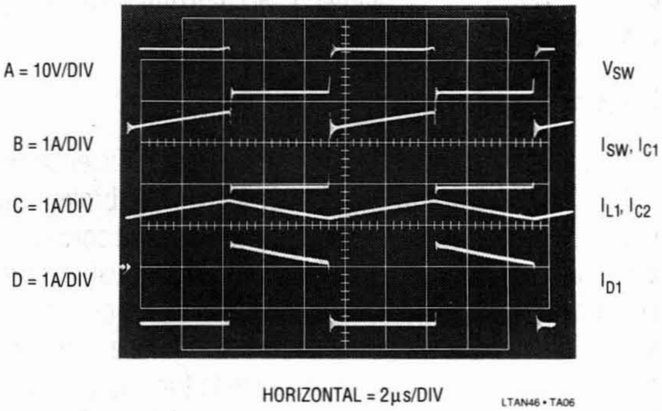


Figure 6. LT1074 Positive Step-Down Converter Waveforms

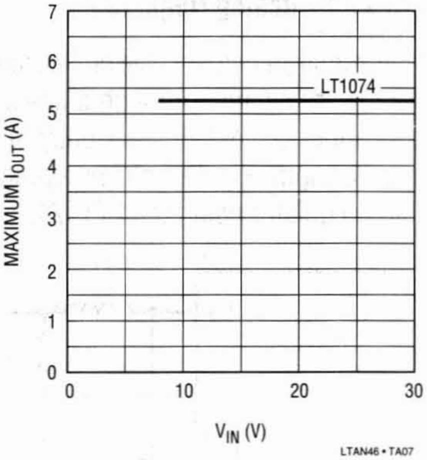


Figure 7. V_{IN} vs I_{OUT} for Positive Buck Converter

The filter capacitors provide a low impedance return path for AC current. The output capacitor's current waveform looks exactly like the inductor's current waveform (trace C), except the capacitor's current has no DC component. The RMS current for the output capacitor is quite low, approximately 150mA RMS with a 1A load. The input capacitor's current waveform is the same as the V_{SW} pin current (trace B). Its ripple current is approximately equal to 1/2 I_{OUT} (500mA) and is noticeably higher compared to the output capacitor current.

Figure 8 shows that efficiency can generally exceed 75%. The output diode and LT1074 switch are the two main loss elements. A Schottky diode is chosen for its low forward voltage drop. It introduces a 5% loss whereas a silicon diode would double this figure. The LT1074 switch has a relatively constant 2.0V loss. At low input voltages efficiency is degraded because this loss makes up a higher percentage of the available supply. Higher inputs make the fixed loss a smaller percentage, improving efficiency.

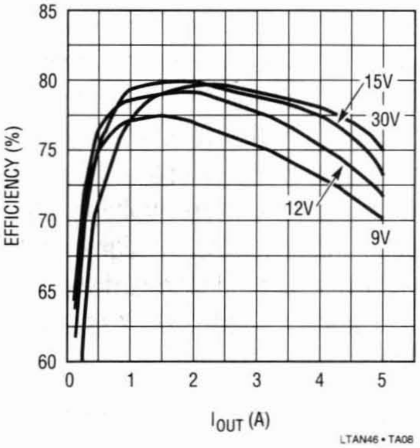


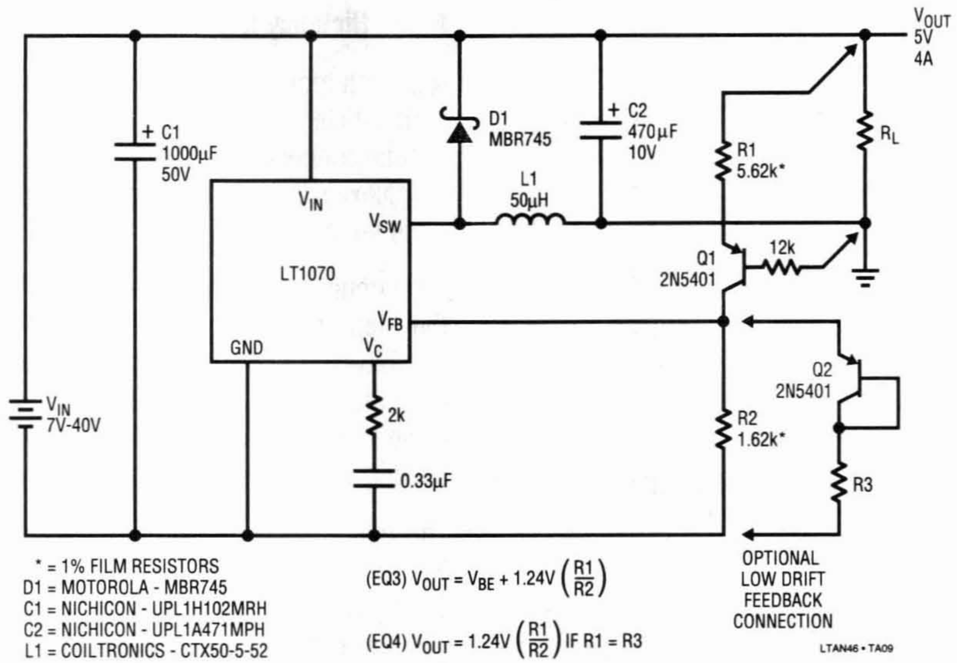
Figure 8. LT1074 Positive Buck Converter Efficiency for Various Input Voltages and Load Currents

Floating Input Step-Down Switching Regulator

Figure 9 shows a way to obtain significantly higher efficiency at low input voltages. This technique utilizes the low saturation characteristics of the LT1070 power switch to obtain efficiency in excess of 85% for a 9V input. In this circuit the input voltage negative terminal is not connected to the output voltage negative terminal. The input must be allowed to float. A floating input can either be a battery or a galvanically isolated transformer's winding. This circuit is particularly useful in battery application since battery voltages are usually low and maximizing efficiency is often a critical issue.

This circuit operates similarly to Figure 5. The primary difference between this circuit and Figure 5 is the power switch type and location. Here, one side of the inductor is at ground potential and the LT1070's NPN power switch connects the other side to the input supply negative terminal. The LT1074 connects the inductor between the output voltage and the positive supply rail. With the inductor connected to ground instead of the positive rail, a common emitter NPN can be used instead of the much higher loss composite PNP used in the LT1074. This minimizes the power transistor's voltage drop contribution to power loss. Appendix C compares the conduction losses between the two switch types.

Switching waveforms are shown in Figure 10. The current waveforms are identical to those of Figure 6. However, the


V_{OUT}
5V
4A
+ C1
1000µF
50V
D1
MBR745
+ C2
470µF
10V
L1
50µH
R1
5.62k*
R_L
V_{IN}
V_{SW}
LT1070
GND
V_{FB}
V_C
Q1
2N5401
12k
Q2
2N5401
2k
0.33µF
R2
1.62k*
R3
V_{IN}
7V-40V
OPTIONAL
LOW DRIFT
FEEDBACK
CONNECTION
LTAN46 • TA09

* = 1% FILM RESISTORS
D1 = MOTOROLA - MBR745
C1 = NICHICON - UPL1H102MRH
C2 = NICHICON - UPL1A471MPH
L1 = COILTRONICS - CTX50-5-52

(EQ3) $V_{OUT} = V_{BE} + 1.24V\left(\frac{R1}{R2}\right)$

(EQ4) $V_{OUT} = 1.24V\left(\frac{R1}{R2}\right)$ IF R1 = R3

Figure 9. LT1070 Floating Input Step-Down Switching Regulator

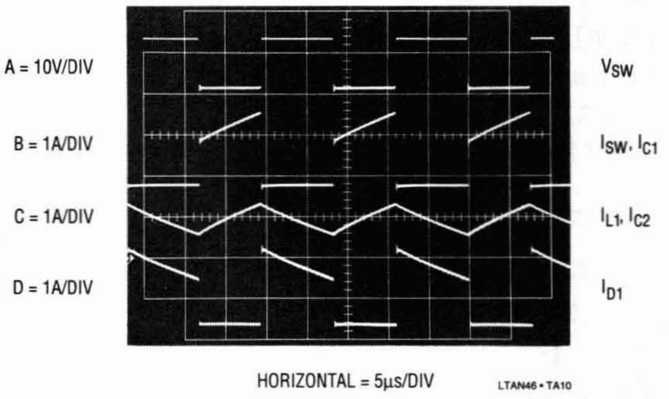


Figure 10. LT1070 Floating Input Step-Down Converter Waveforms

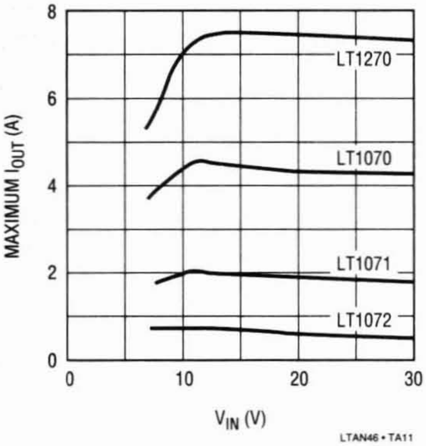


Figure 11. V_{IN} vs I_{OUT} Floating Input Buck Converter

V_{SW} pin voltage transitions are different. For the LT1070 circuit the V_{SW} pin voltage swings from the negative terminal of the input supply to a diode drop above the output voltage. In comparison, the LT1074's V_{SW} pin switches from the positive rail to a diode drop below ground. Figure 11 details the maximum output current for various input voltages and power devices. When the LT1070 operates at a duty cycle greater than 50% its maximum switch current is reduced, which causes the decrease in maximum output current seen at low input voltages.

The feedback senses the output with respect to the GND pin, so a level shift is required from the 5V output. Q1 serves this purpose, introducing only –2mV/°C drift, (see Equation 3). This is normally not objectionable in a logic supply, but can be compensated for with the optional appropriately scaled diode/resistor, (see Equation 4 in Figure 9).

Figure 12 shows this circuit's efficiency characteristics. Efficiency at low input voltages is significantly higher than the previous circuit because of lower power switch losses.

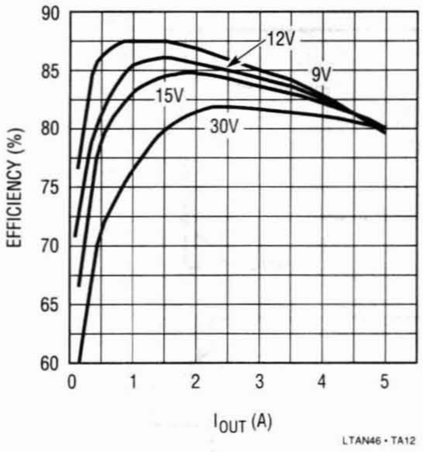


Figure 12. LT1070 Negative Buck Converter Efficiency for Various Input Voltages and Load Currents

At high input voltages and low output current levels the IC's quiescent current reduces the circuit's efficiency. The diode, filter capacitors, and inductor losses are comparable to the previous LT1074 buck circuit.

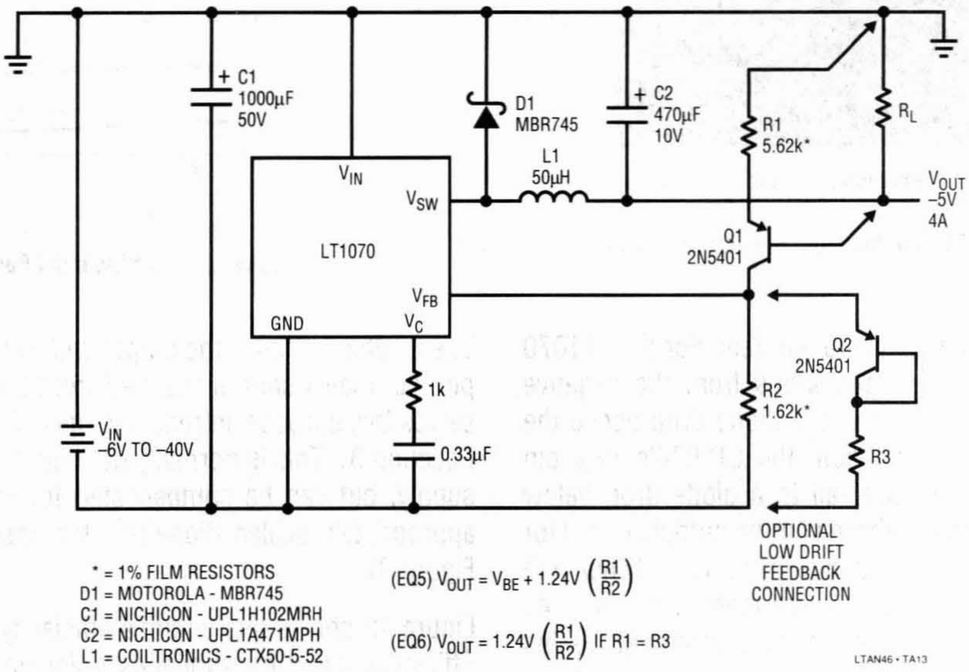
Figure 13 shows this circuit's topology used for negative buck conversion. Its operating waveforms are the same as shown in Figure 10. The common ground connection between the input and output voltage does not change the operating characteristics of the circuit.

High Efficiency Step-Down Switching Regulator

Although more complicated than the previous circuit, the high efficiency circuit in Figure 14 allows a common ground connection between input and output. Here, circuit complexity is traded off for increased efficiency at low input voltages.

The circuit operating characteristics are similar to that of the step-down regulator of Figure 5. In this case, an LT1070 common emitter NPN output switch is used to drive the inductor to the positive rail. Using an NPN switch achieves lower conduction losses than the composite PNP used in the LT1074.

The operating waveforms for this circuit are shown in Figure 15. When the LT1070's switch turns on, it pulls the GND pin to the input voltage. Trace A is the GND pin voltage and trace B is its current. During this period, current flows from the input through the LT1070 and the inductor, and into the load. Inductor current is shown in trace C. When the LT1070 switch turns off, the voltage on the GND pin drops until the clamp diode is forward biased (trace D is clamp diode current), providing a current path for the inductor to transfer its energy to the output. Maximum output current for various input voltages and power devices is shown in Figure 16.



* = 1% FILM RESISTORS
D1 = MOTOROLA - MBR745
C1 = NICHICON - UPL1H102MRH
C2 = NICHICON - UPL1A471MPH
L1 = COILTRONICS - CTX50-5-52

$$\text{(EQ5)}\quad V_{OUT} = V_{BE} + 1.24V\left(\frac{R1}{R2}\right)$$

$$\text{(EQ6)}\quad V_{OUT} = 1.24V\left(\frac{R1}{R2}\right)\text{ IF } R1 = R3$$

Figure 13. LT1070 Negative Step-Down Switching Regulator

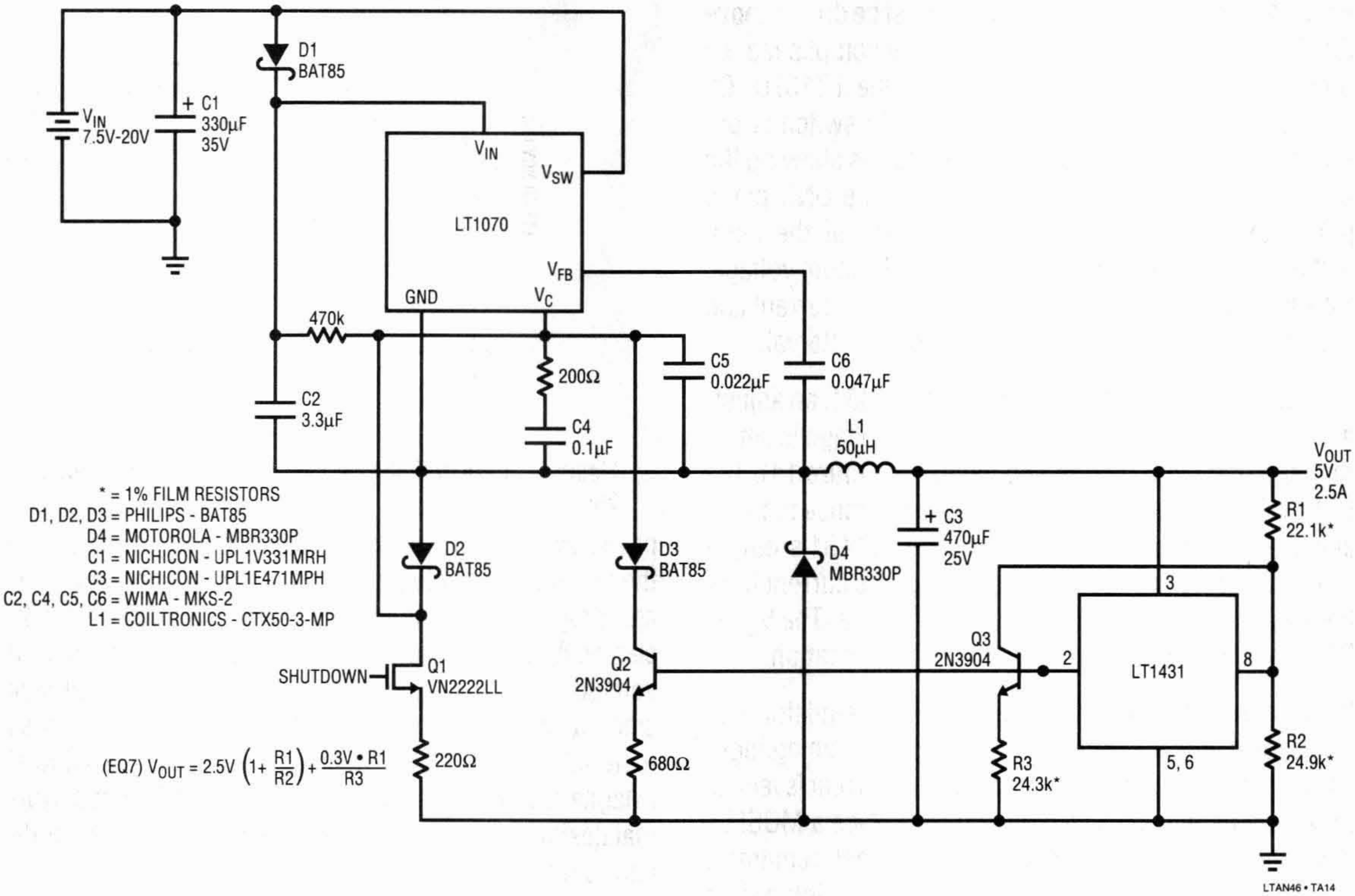

VIN 7.5V-20V
+ C1 330μF 35V
D1 BAT85
VIN
VSW
LT1070
VFB
GND
VC
470k
C2 3.3μF
200Ω
C4 0.1μF
C5 0.022μF
C6 0.047μF
L1 50μH
VOUT 5V 2.5A
R1 22.1k*
+ C3 470μF 25V
D4 MBR330P
D2 BAT85
D3 BAT85
3
LT1431
2
8
5, 6
Q3 2N3904
Q2 2N3904
Q1 VN2222LL
SHUTDOWN
220Ω
680Ω
R3 24.3k*
R2 24.9k*
* = 1% FILM RESISTORS
D1, D2, D3 = PHILIPS - BAT85
D4 = MOTOROLA - MBR330P
C1 = NICHICON - UPL1V331MRH
C3 = NICHICON - UPL1E471MPH
C2, C4, C5, C6 = WIMA - MKS-2
L1 = COILTRONICS - CTX50-3-MP
(EQ7) $V_{OUT} = 2.5V\left(1+\frac{R1}{R2}\right)+\frac{0.3V \bullet R1}{R3}$
LTAN46 • TA14

Figure 14. LT1070 High Efficiency Buck Converter

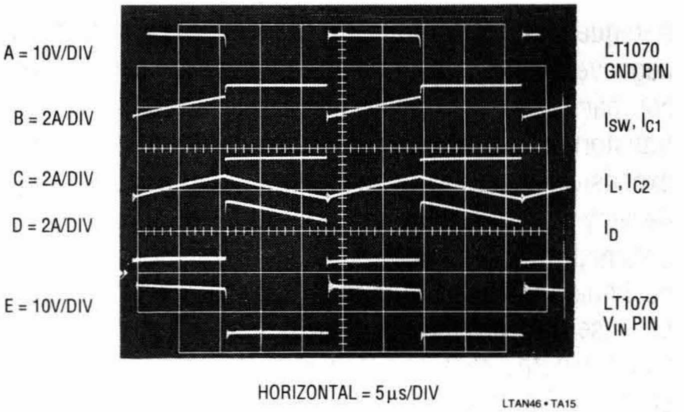


Figure 15. LT1070 High Efficiency Step-Down Converter Waveforms

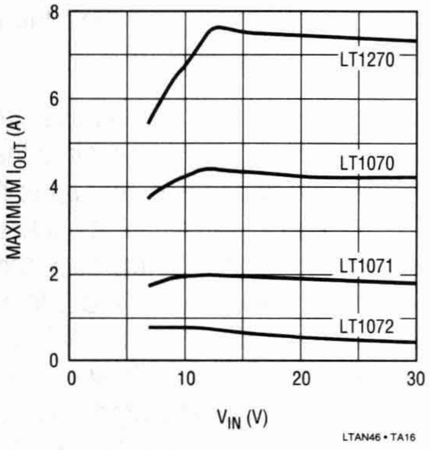


Figure 16. V_{IN} vs I_{OUT} for High Efficiency Buck Converter

For this circuit to function the V_{IN} pin must be driven above the input voltage (trace E). This is accomplished by bootstrapping C2 off the GND pin of the LT1070. C2 charges up through D1 when the LT1070 switch is off. When the switch turns on, D1 reverse biases allowing the V_{IN} pin to rise above the input voltage. The GND pin is pulled to within a few hundred millivolts of the input voltage. The V_{IN} pin voltage is now twice the input voltage. C2's stored charge provides adequate supply current and base drive for the power switch during this interval.

The output voltage is controlled by the LT1431, an adjustable shunt voltage regulator. The output voltage is set by the ratio of R1 and R2, (see Equation 7 in Figure 14). The LT1431's error amplifier compares the reference pin voltage to its internal 2.5V reference. The LT1431's output drives a shunt transistor, Q2, which absorbs current from the V_C pin of the LT1070, adjusting duty cycle. The V_C pin RC network provides sufficient loop compensation.

It is often desirable to put a switching regulator into "shutdown mode", a condition where the switching regulator is turned off and draws micropower current levels, to maximize battery life. One solution is to place a MOSFET switch in series with the input. This approach requires a large power device and reduces efficiency at high output currents. The LT1070 provides an elegant solution to this problem by integrating a shutdown feature. When the voltage between the V_C and GND pin is pulled below 150mV, the IC shuts down pulling only 150µA. This is implemented by turning on Q1, reducing the circuit's quiescent current from 6mA to 150µA.

When the input voltage is first applied to this circuit, the regulator dumps full short circuit current into the output capacitor, attempting to bring the output up to its regulated value. The output can overshoot its desired value before the control loop is able to idle back the output current. This condition could overdrive Q2, forcing it to pull the voltage between the V_C and GND pin below 150mV, and putting the LT1070 in its shutdown mode. The output voltage would momentarily drop to zero and remain there until the V_C pin rises above 900mV. To prevent this condition from occuring, the V_C pin is clamped by D3 and the 470k resistor is used as a pull up.

Figure 17 shows efficiency approaching 90%. Squeezing the utmost efficiency from this circuit requires care. The power switch and the catch diode conduction losses are the two main loss elements. These devices forward voltage drop must be minimized in order to maximize efficiency. A Schottky diode is used for its minimum forward voltage drop. The inductor selection is not a trivial task since it can add a couple percent loss. Low core loss material such as Molypermalloy, "high flux", "Kool Mu" (Magnetics, Inc.), and ferrite cores should be used. Normal design procedure for wire size may have to be modified to reduce copper loss.

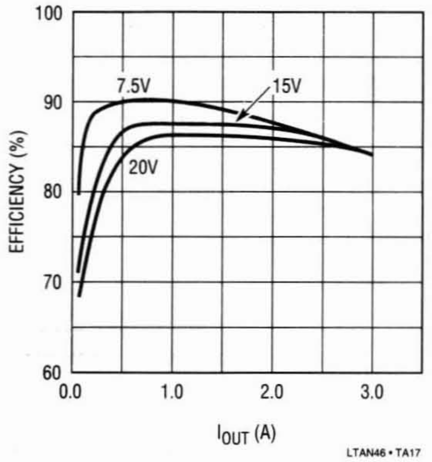


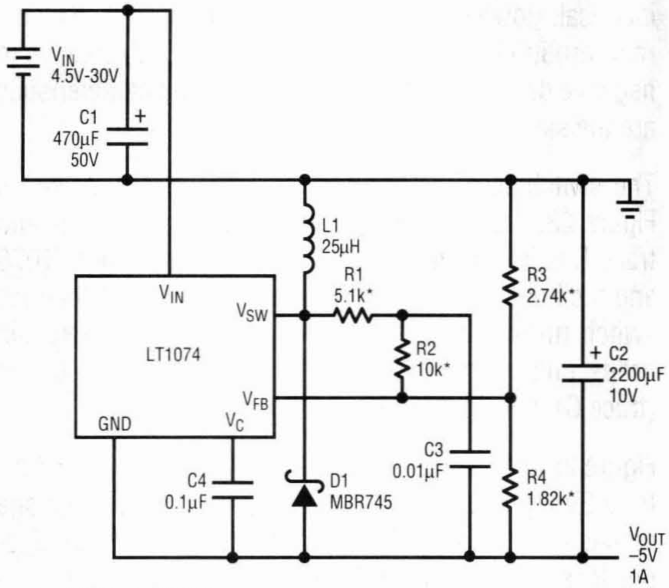
Figure 17. LT1070 High Efficiency Positive Buck Converter Efficiency

The LT1431 and associated control circuitry can be replaced by an LT1432. Refer to the LT1432 data sheet for further details.

Positive to Negative Buck Boost Switching Regulator

A frequent switching regulator application is to produce a negative output from a positive supply, usually 5V. One approach is to use a transformer in a flyback topology, but transformers are not off-the-shelf components. They are expensive, especially in low volumes, and can have long delivery times. Alternately, a negative output is easily obtained with a simple inductor. Inductors are more desirable than transformers in many converter designs because they are readily available and economical. The negative output requirement is easily fulfilled by the circuit shown in Figure 18.

The operating waveforms are shown in Figure 19. When the LT1074 switch turns on, current flows from the input through the LT1074 and into the inductor. Trace A is the switch pin voltage and trace B is its current. During this

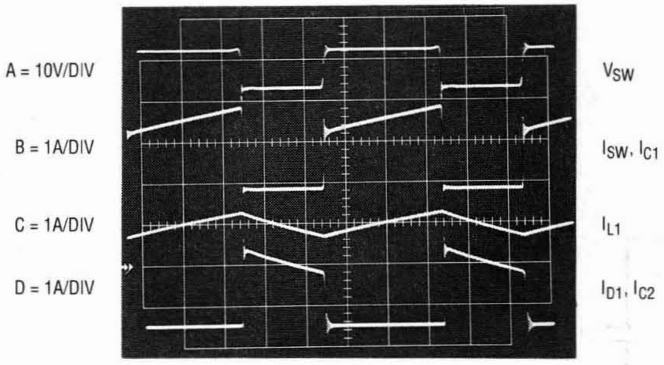


* = 1% FILM RESISTORS
D1 = MOTOROLA - MBR745
C1 = NICHICON - UPL1C471MRH
C2 = NICHICON - UPL1A222MRH
L1 = COILTRONICS - CTX25-5-52

$$V_{OUT} = 2.21V\left(1+\frac{[(R1+R2)//R3]}{R4}\right) \quad \text{(EQ8)}$$

LTAN46 • TA18

Figure 18. LT1074 Positive to Negative Switch



HORIZONTAL = 2µs/DIV

LTAN46 • TA19

Figure 19. LT1074 Positive to Negative Converter Waveforms

period current ramps up in the inductor (trace C) as energy is stored in the core. When the LT1074 power switch turns off, the voltage on the V_{SW} pin drops until clamp diode D1 forward biases (trace D). This provides a current path for the inductor to transfer its energy to the output. Figure 20 shows this circuit can provide a 1A output for a 4.5V input.

In this architecture the LT1074's GND pin is tied to the negative output rather than to ground. This technique eliminates a level shifting op amp in the feedback path. Feedback is sensed from circuit ground, and the regulator forces its feedback pin to 2.21V above its GND pin. The output voltage can be varied by changing the R1-R2-R3-R4 divider ratio, (see Equation 10 in Figure 26). The LT1074 controls duty, cycle to achieve output voltage regulation.

Positive to negative converters have a "right half plane zero" in the transfer function, which makes them particularly hard to frequency stabilize, especially with low input voltage. R1, R2 and C3 form an AC feedforward path needed for loop compensation at low input voltages. They can be omitted for $V_{IN} > 10V$, or $V_{IN}/V_{OUT} > 2$. This network along with C4 provides stable loop frequency compensation.

Efficiency generally exceeds 60% as shown in Figure 21. Efficiency is degraded at low input voltages where the LT1074 power switch is responsible for the majority of the efficiency loss. Its 2.0V switch voltage drop cuts the

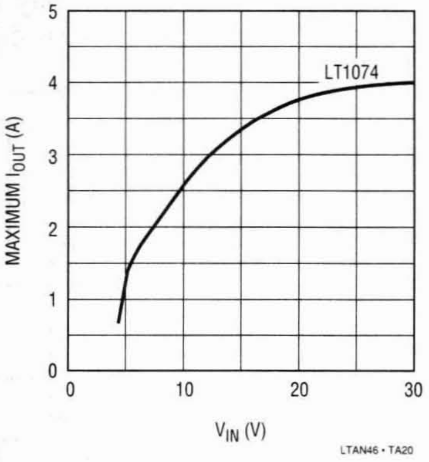


Figure 20. V_{IN} vs I_{OUT} for Positive to Negative Converter

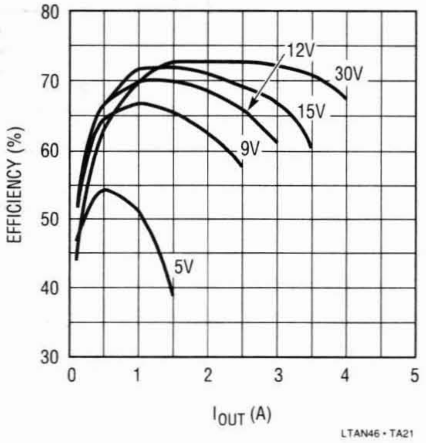


Figure 21. LT1074 Positive to Negative Converter Efficiency for Various Input Voltages and Load Currents

efficiency by 28% at a 5V input; another 10% is contributed by the output diode. Higher input voltages make the fixed LT1074 voltage drop a smaller percentage, improving efficiency.

High Efficiency Positive to Negative Switching Regulator

The previous circuit has excellent efficiency performance above a 12V input. However, at low input voltages the efficiency falls off dramatically. The LT1074's internal power switch voltage drop is the major contributor to the degradation of efficiency. Figure 22 shows an alternative approach to generate a negative output from a positive input. Here, the LT1070 low loss switching transistor achieves remarkable efficiency levels, even with a 5V input.

This circuit is reminiscent of the high efficiency buck converter of Figure 14. The control circuitry and the manner in which the LT1070 power switch is driven are identical. However, the power components route the current through the same course as the previous positive to negative design; therefore, their switching characteristics are the same.

The switching waveforms for this circuit are shown in Figure 23. Trace A is the LT1070's GND pin voltage and trace B is its current. Current flows through the LT1070 and the inductor when the power switch is on. When the switch turns off, the voltage on the LT1070's GND pin drops until diode D4 forward biases. Inductor current (trace C) then flows through D4 (trace D).

Figure 25 shows this circuit's efficiency approaches 70% for a 5V input. The higher efficiency at low input voltage results from the LT1070's extremely low switch conduction loss. The effect of switch loss can be seen by comparing the efficiency characteristics of Figure 21 and Figure 25. The LT1074-based circuit's efficiency drops dramatically at inputs below 9V.

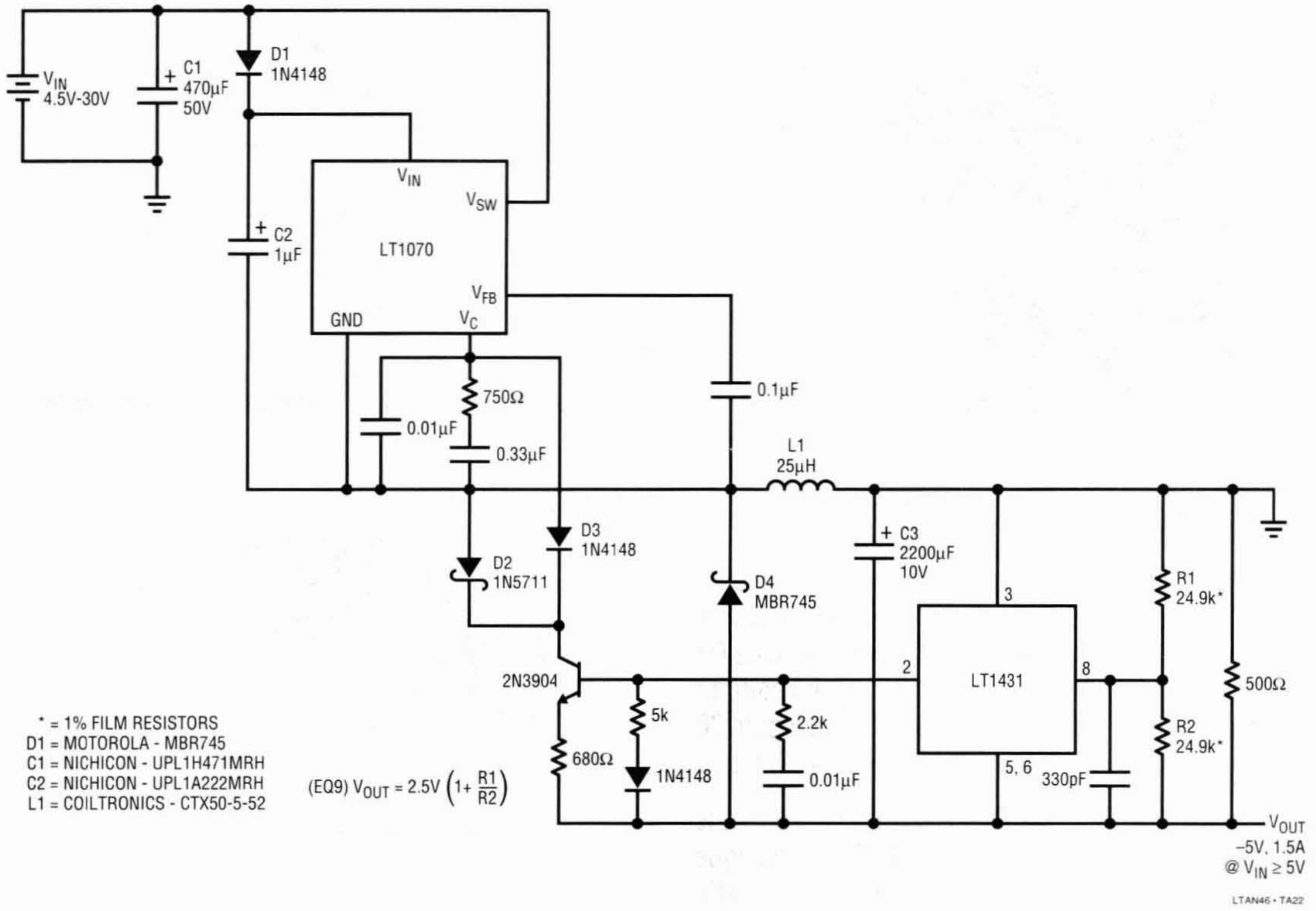

V_IN 4.5V-30V
C1 470µF 50V
D1 1N4148
V_IN
V_SW
LT1070
V_FB
GND
V_C
C2 1µF
750Ω
0.01µF
0.33µF
0.1µF
L1 25µH
D3 1N4148
D2 1N5711
D4 MBR745
C3 2200µF 10V
3
2
8
LT1431
5, 6
R1 24.9k*
R2 24.9k*
500Ω
330pF
2N3904
5k
680Ω
1N4148
2.2k
0.01µF
V_OUT –5V, 1.5A @ V_IN ≥ 5V
* = 1% FILM RESISTORS
D1 = MOTOROLA - MBR745
C1 = NICHICON - UPL1H471MRH
C2 = NICHICON - UPL1A222MRH
L1 = COILTRONICS - CTX50-5-52
(EQ9) V_OUT = 2.5V (1+ R1/R2)
LTAN46 • TA22

Figure 22. LT1070 High Efficiency Positive to Negative Switching Regulator

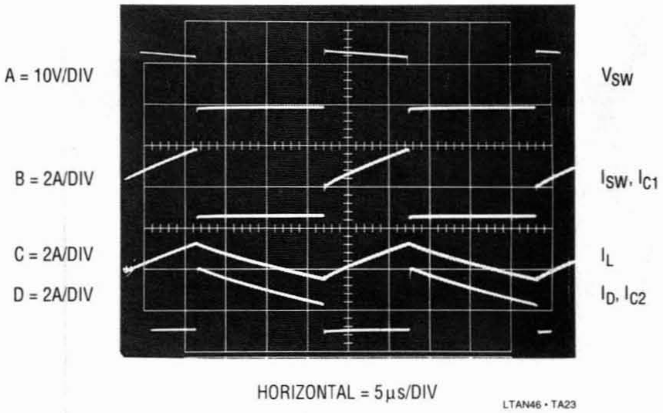


Figure 23. LT1070 High Efficiency Positive to Negative Converter Waveforms

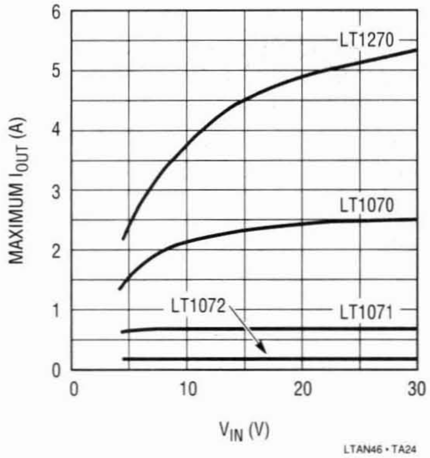


Figure 24. V_{IN} vs I_{OUT} for High Efficiency Positive to Negative Converter

LT1070 Negative to Positive Switching Regulator

This converter topology can maintain a constant output voltage whether the absolute value of the negative input voltage is greater or less than the positive output voltage. This is extremely desirable in battery operated electronic equipment. This flexibility reduces the number of battery cells required and provides a constant output voltage over the battery's complete operating range, maximizing battery life. The circuit is shown in Figure 26. This technique can be used only if the input and output voltage negative terminals are not connected to each other.

This circuit operates similar to the boost regulator of Figure 1, but is intended for buck-boost conversion. Here, the positive terminal of the battery is connected to ground and the LT1070's GND pin is connected to the negative terminal. The feedback pin senses with respect to GND pin, so Q1 provides a level shift from the 5V output.

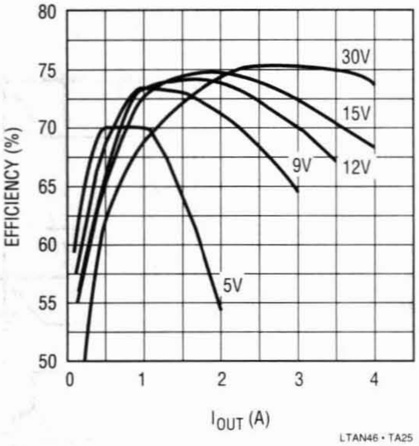


Figure 25. LT1070 High Efficiency Positive to Negative Converter Efficiency for Various Input Voltages and Load Current

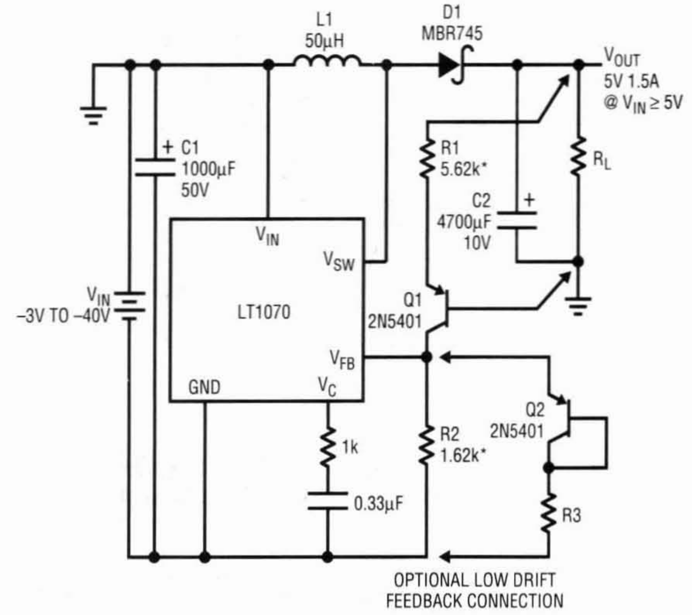
Figure 27 shows the circuit operating waveforms. They resemble those of the boost regulator (Figure 2). The primary difference between the two circuits is that the inductor current does not flow through input capacitor C1 during the switch off time. This is noticeable in the input capacitor's ripple current waveform (trace B). The ripple current is significantly higher, compared to the boost circuit, since the current is being pulled from the input capacitor in pulses. This increased ripple current necessitates a larger input capacitor. Maximum output current for various input voltages and power devices is shown in Figure 28.

Figure 29 shows circuit efficiency in excess of 75%. Once again the main contributors to power loss are the switching diode and LT1070's internal power switch.

Flyback Converter

Many applications require multiple regulated output potentials. A popular output combination is 5V and ±12V as implemented in the circuit shown in Figure 30.

This circuit is a basic flyback regulator. The transformer transfers energy from the 12V input to the 5V and ±12V outputs. Figure 31 shows the operating waveforms for this circuit. Trace A is the voltage at the V_{SW} pin and trace B is its current. During the V_{SW} on-time, the V_{SW} pin is pulled



* = 1% FILM RESISTORS
D1 = MOTOROLA - MBR745
C1 = NICHICON - UPL1H102MRH
C2 = NICHICON - UPL1A472MRH
L1 = COILTRONICS-CTX50-5-52

(EQ10) $V_{OUT} = V_{BE} + 1.24V\left(\frac{R1}{R2}\right)$

(EQ11) $V_{OUT} = 1.24\left(\frac{R1}{R2}\right)$ IF R1 = R3

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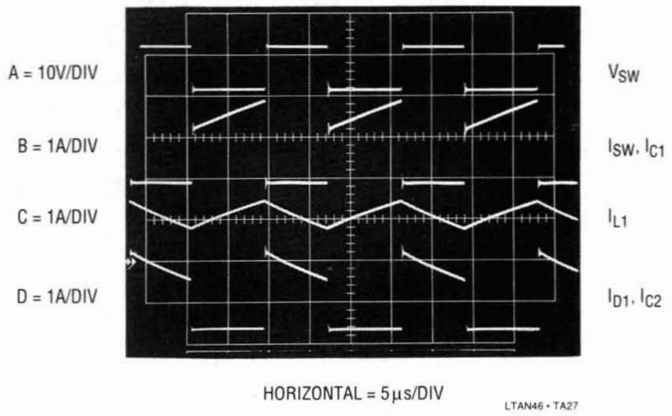
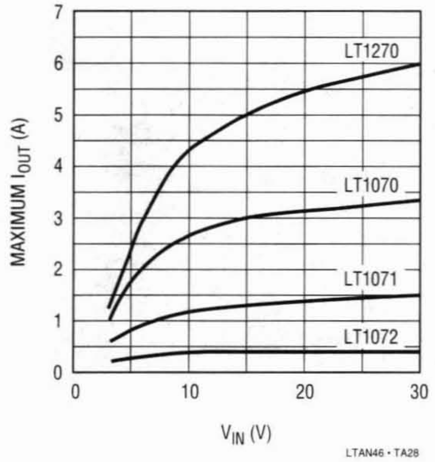
Figure 26. LT1070 Negative to Positive Switching Regulator



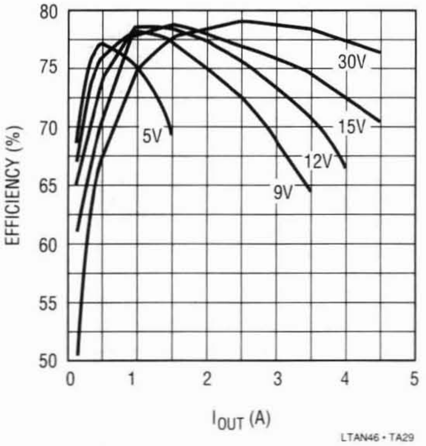
LTAN46 • TA27

Figure 27. LT1070 Negative to Positive Converter Waveforms



LTAN46 • TA28

Figure 28. V_{IN} vs I_{OUT} for Negative to Positive Converter

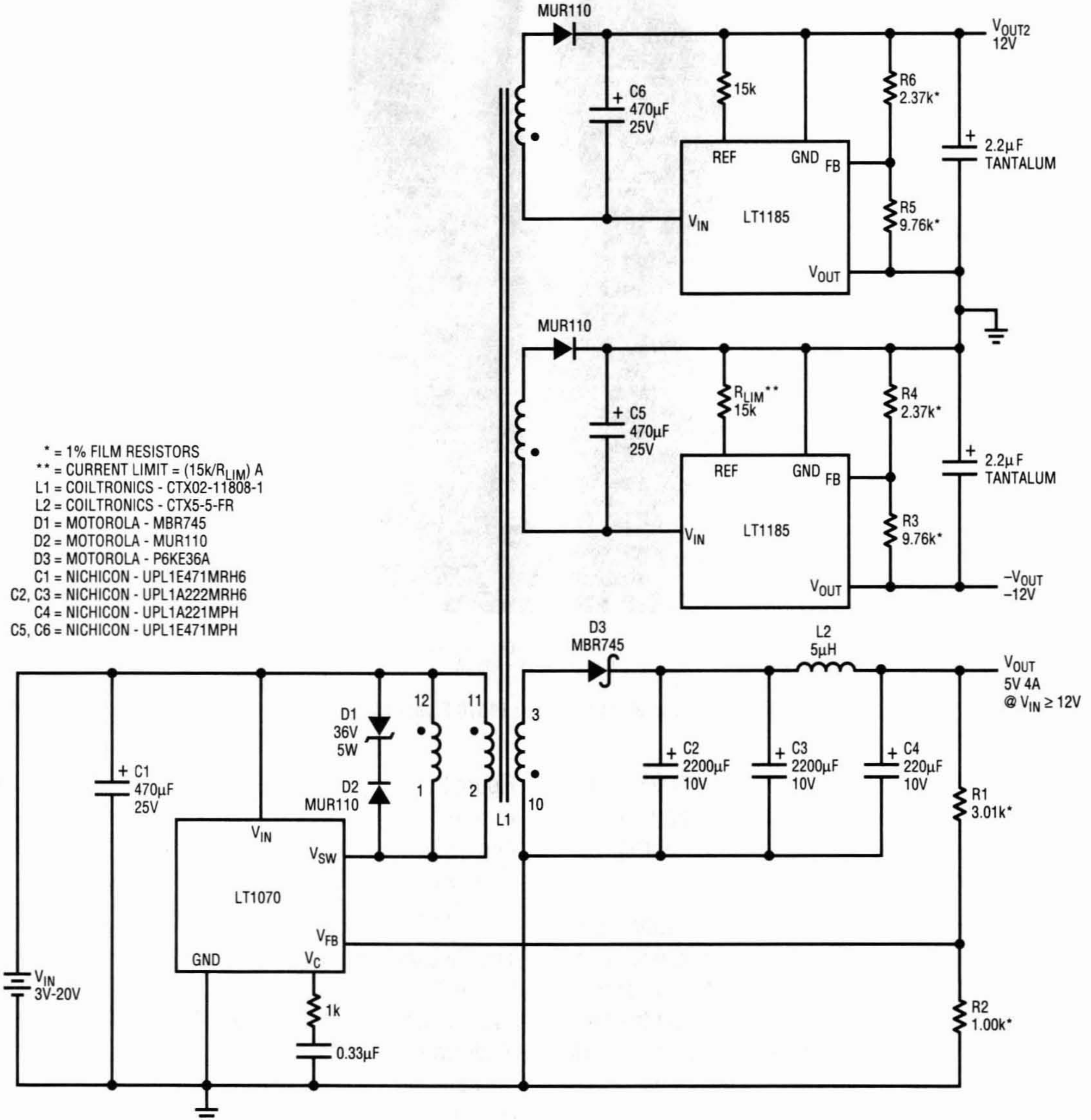


LTAN46 • TA29

Figure 29. LT1070 Negative to Positive Converter Efficiency for Various Input Voltages and Load Currents

to ground forcing the input voltage across the primary winding. After the initial jump, the primary current (trace C) rises slowly as the magnetic field builds up. The magnetic field in the core induces a voltage on the secondary windings, which is proportional to the input voltage times the turns ratio. However, no power is transferred to the outputs because the rectifier diodes are reverse biased. The energy is stored in the transformer's magnetic field. When the switch is turned off, energy is no longer transferred to the transformer causing the magnetic field to collapse. The collapsing magnetic field induces a change in voltage across the transformer's windings. During this transition the V_{SW} pin's voltage flies to a potential above the input voltage, the secondary forward biases the rectifier diodes, and the transformer's energy is transferred to the outputs. Trace D is the voltage seen on the 5V secondary and trace E is its current.

This is not an ideal transformer, so not all the energy is coupled into its secondary windings. The energy left in the primary winding causes the overvoltage spike seen on the V_{SW} pin (trace F). This phenomenon is modeled by an inductor term placed in series with the primary winding. When the switch is turned off, current continues to flow in the primary winding, causing D1 and D2 to conduct (trace G). This diode network clamps the flyback voltage spike,


MUR110
VOUT2
12V
C6
470μF
25V
15k
R6
2.37k*
2.2μF
TANTALUM
REF
GND
FB
LT1185
VIN
VOUT
R5
9.76k*
MUR110
RLIM**
15k
C5
470μF
25V
R4
2.37k*
2.2μF
TANTALUM
REF
GND
FB
LT1185
VIN
VOUT
R3
9.76k*
–VOUT
–12V
D3
MBR745
L2
5μH
VOUT
5V 4A
@ VIN ≥ 12V
D1
36V
5W
D2
MUR110
12
11
3
1
2
10
L1
C1
470μF
25V
C2
2200μF
10V
C3
2200μF
10V
C4
220μF
10V
R1
3.01k*
VIN
VSW
LT1070
VFB
GND
VC
1k
0.33μF
R2
1.00k*
VIN
3V-20V

* = 1% FILM RESISTORS
** = CURRENT LIMIT = $(15k/R_{LIM})$ A
L1 = COILTRONICS - CTX02-11808-1
L2 = COILTRONICS - CTX5-5-FR
D1 = MOTOROLA - MBR745
D2 = MOTOROLA - MUR110
D3 = MOTOROLA - P6KE36A
C1 = NICHICON - UPL1E471MRH6
C2, C3 = NICHICON - UPL1A222MRH6
C4 = NICHICON - UPL1A221MPH
C5, C6 = NICHICON - UPL1E471MPH

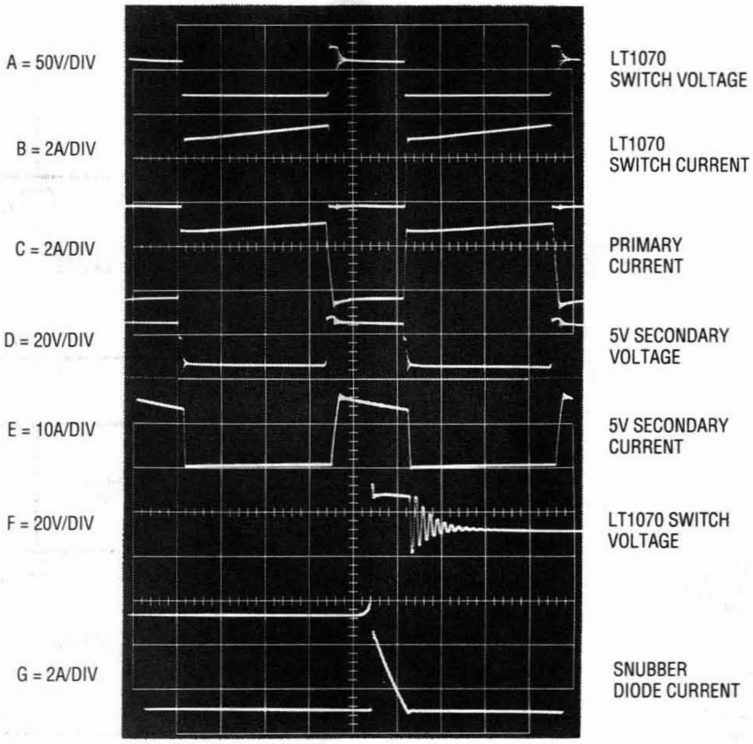
(EQ12) $V_{OUT} = 1.24V\left(1 + \frac{R1}{R2}\right)$

(EQ13) $-V_{OUT} = 2.37V\left(1 + \frac{R3}{R4}\right)$

(EQ14) $V_{OUT2} = 2.37V\left(1 + \frac{R5}{R6}\right)$

LTAN46 • TA30

Figure 30. LT1070 Flyback Switching Regulator



A, B, C, D, E HORIZONTAL = 5μs/DIV
F, G HORIZONTAL = 1μs/DIV

LTAN46 • TA31

Figure 31. Waveforms for the LT1070 Flyback Converter

preventing excessive voltage at the LT1070's V_{SW} pin. When the primary current reaches zero, the V_{SW} pin's voltage settles to a potential related to the turns ratio, output and input voltage.

How well the unregulated outputs track each other, often referred to as cross regulation, depends upon how tightly they are magnetically coupled to one another. Post regulators are needed on the unregulated outputs if the cross regulation error is too great. Such error can be as much as 20% depending upon output loading conditions.

The isolated secondaries allow a negative voltage regulator to be used to regulate the +12V output. The advantage of the LT1185 over standard linear regulators is its ability to control current limit to typically within 4%, between its 1A-3A range, allowing the use of smaller rectifier diodes, secondary windings wire size, and core size. The isolated secondary windings' allows the input of the LT1185 to float below ground. The LT1185 negative voltage regulators maintain both positive and negative outputs.

Figure 32 represents the total available output power for various input voltages and power devices. For simplicity the available output power is summed into the 5V output. If the auxiliary outputs are used, the maximum available current from the 5V output is reduced.

This flyback circuit's efficiency approaches 80% (see Figure 33). Power is primarily dissipated in the LT1070, catch diode D3, and zener diode D1. The LT1070 and catch diode impose losses in the same manner as they did in the previous circuits. The zener clamp diode is a power loss element commonly found in flyback designs. It dissipates energy stored in the transformer's leakage inductance. To keep leakage inductance losses to a reasonable level, leakage inductance should be kept to less than 1% of the primary inductance.

For the flyback topology, the output filter capacitor takes a real beating at high output currents. This is due to the transformer providing current to the output capacitor in pulses. In many flyback designs the turns ratio is less than

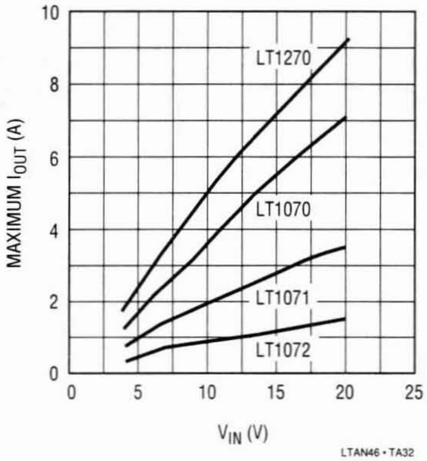


Figure 32. V_{IN} vs I_{OUT} for Flyback Converter

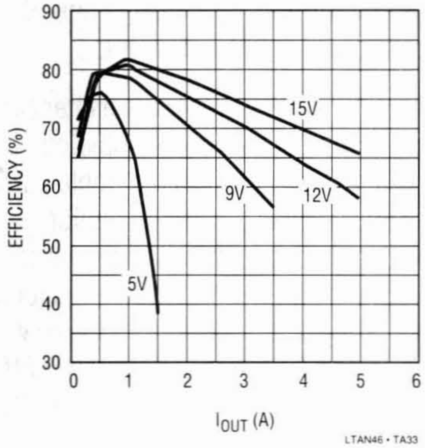


Figure 33. LT1070 Flyback Converter Efficiency for Various Input Voltages and Load Currents

one and the secondary current is 1/N times higher than the primary current (see Figure 31). The primary winding peak current (trace C) is 5A, whereas the secondary winding peak current (trace E) is 15A. In this case two capacitors connected in parallel are needed to handle the RMS ripple current.

References

1. Coiltronics
984 S.W. 13th Court
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APPENDIX A

Thermal Considerations for Aluminum Electrolytic Filter Capacitors

Aluminum electrolytic capacitors often fail in switching regulators because many designers do not view them as power components. Like any power device, capacitors have thermal limitations which must be observed for acceptable performance and reliability. Excessive capacitor temperature can cause an open or short circuit, capacitance drop, electrolyte leakage, increased leakage current or safety venting.

Increased temperature causes a gradual evaporation of the electrolyte through the capacitor's seal. As the electrolyte is lost, the capacitance is reduced and Effective Series Resistance (ESR) rises, causing increased power dissipation. If this regenerative process continues it can cause the capacitor to exceed its maximum thermal rating. In poorly designed power supplies it is not uncommon to have early field failures because the electrolyte in a filter capacitor has dried up.

Filter capacitors are chosen by physical size rather than capacitance value, since larger size capacitors have higher ripple current ratings, lower ESR and more heat dissipation capability. Selecting the appropriate size for a given application depends upon several factors:

- Ripple current rating/ESR
- Position on the PC board
- Maximum ambient temperature
- Load life

Additional factors include output voltage ripple and loop stability. These secondary considerations are not treated here.

The capacitor's operating ripple current sets the minimum acceptable capacitance size. Maximum allowable ripple current is selected to limit temperature rise in the capacitor. This internal temperature rise is proportional to the square of the capacitor's ripple current. Typical core to ambient temperature rise is between 5°C to 10°C. For reliable operation the capacitor must operate below the maximum allowable ripple current. Appendix B explains how to measure operating ripple current.

There is a tendency for designers to select filter capacitors based on capacitor value instead of ripple current. This approach can be catastrophic because ripple current ratings vary widely between capacitor technologies, manufacturers and voltage ratings. Figure A1 shows how varied the ripple current rating is for similar value capacitors with different voltage ratings. In this example, the 63V part can handle over twice the RMS current of the 6.3V device because the higher voltage capacitor is physically larger.

Voltage Rating	6.3V	10V	16V	25V	35V	50V	63V
I_{RMS} (mA)	950	1060	1410	1660	1989	2120	2370

Nichicon PL series 105µF-105°C

Figure A1. Ripple Current Ratings for Different Voltage Ratings

High ripple currents require capacitors to have low ESR, greater surface area, and a high heat transfer constant. Figure A2 shows the relationship between volume and ripple current rating. Tall capacitors of equal volume as short, fat ones tend to be able to dissipate more heat since they can transfer the heat to the case surface more easily.

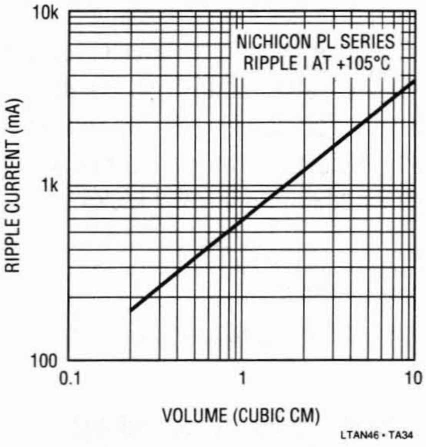


Figure A2. Ripple Current vs Volume

When the required ripple current is greater than the maximum rated ripple current, it becomes necessary to parallel capacitors. Paralleling allows sharing of the ripple current between capacitors. The ESR of each capacitor acts as a current ballasting impedance. In some instances it may be preferable to parallel capacitors even when a single device of higher ripple current rating is available. This allows smaller size capacitors to be utilized. Heat flow increases from multiple capacitors when compared to a single device with a higher current rating because the heat is spread over a greater area.

The ESR of the capacitor is the predominant cause of internal temperature rise above ambient. The power loss in the capacitor is determined by:

$$P_{CAP} = (I_{RMS})^2 \bullet ESR$$

ESR = Effective Series Resistance

I_{RMS} = Capacitor Ripple Current

Capacitor size versus ESR rating varies widely for different capacitor technologies and between manufacturers. Figure A3 shows ESR vs Volume for Different Capacitor Manufacturers.

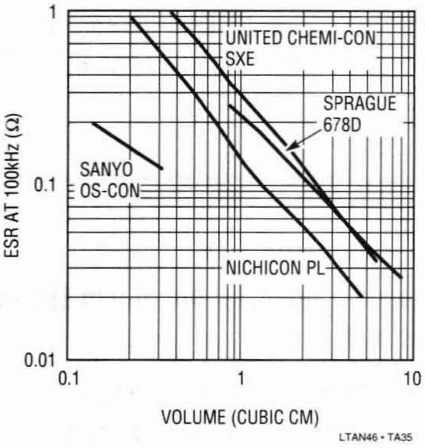


Figure A3. ESR vs Volume for Different Capacitor Manufacturers

Printed circuit board layout can have a dramatic effect on a capacitor's operating temperature. For example, one terminal of an output capacitor is often connected to a catch diode. During full load conditions the diode can reach junction temperatures in excess of 100°C, dissipating several watts. The diode's leads conduct the heat into the PC board traces, where it can be transferred into the filter capacitor, elevating its internal temperature. Wide PC board traces at the diode will dissipate this heat, reducing capacitor heating.

Another frequently overlooked layout consideration is the capacitor's location relative to heatsinks. Heatsinks radiate heat, increasing an adjacent capacitor's temperature.

Capacitor load life includes both parametric and catastrophic failures. A capacitor is considered failed if capacitance, ESR or leakage current exceeds maximum allowable variation. ESR variation is the parameter of primary concern for switching regulators because, as ESR increases, output voltage ripple and thermal dissipation go up. The load life of a capacitor is rated in hours, typically between 1,000 hours and 10,000 hours, with full rated voltage applied across its terminals at a specified temperature, usually 105°C. Load life definitions vary for different type of capacitors.

Load life increases for larger case diameters; refer to Figure A4. Load life is primarily limited by electrolyte loss. One reason for the increased load life between case sizes is that larger devices hold more electrolyte; it simply takes longer for the electrolyte to dry up.

Case Diameter (mm)	0.5	0.6	0.8
Load Life (hours)	2,000	3,000	5,000

Nichicon PL series 105µF-105°C

Figure A4. Load Life Rating for Different Case Diameters

The load life specification of a capacitor can be a little confusing. For example, a Nichicon PL series capacitor with a case diameter of between 8mm-10mm has a load life of 3,000 hours while being operated at 105°C. This information as stated is not very useful, since most products are designed to last longer than 18 weeks (3,000 hours), and will not be subject to 105°C.

The relationship between thermal stress and expected life of the capacitor can be predicted by:

$$L_X = L_O * 2^{\frac{105^\circ C - (T_X + \Delta T_X)}{10}} \qquad (A1)$$

L_X : Life expectancy in actual operation (hrs)
L_O : Load life at maximum operating temperature (hrs)
T_X : Ambient temperature in actual operation (°C)
ΔT_X : Temperature rise produced by ripple current (°C)

$$\Delta T_X = \frac{I_X^2 \bullet ESR}{B \bullet A} \qquad (A2)$$

I_X : Operating ripple current (A)
ESR : Effective Series Resistance (Ω)
B : Heat transfer constant — determined by case size (W/cm²/°C)
A : Case surface area (cm²)

$$A = \frac{\pi \bullet \phi D \left(\phi D + 4L\right)}{4} \qquad (A3)$$

ϕD : Case diameter
L : Case length

Heat transfer constants are not normal data sheet parameters, but can be obtained from the manufacturer. Figure A5 shows the heat transfer constant for United Chemi-Con electrolytic capacitors. The heat transfer constant is predominately affected by the thermal characteristics of the capacitor's aluminum case and its surface area. Since the aluminum material is the same for all series capacitors, the heat transfer constant depends only on surface area. These thermal parameters assume that the case is completely filled with the foil winding. Not all capacitors' cans are full, and should be checked by disassembling a sample.

Equation A1 shows that with aluminum electrolytic capacitors, load life doubles for every 10°C drop in operating temperature. The equation includes the effects of operating ripple current, ambient temperature and heat transfer constant of the package.

For example, a United Chemi-Con SXE25VB471M10X20LL capacitor operating at a ripple current of 860mA and an ambient temperature of 60°C would have an calculated life time of 3.1 years.

$$I_X = 860mA,\ ESR = 0.14\Omega,\ L_O = 2{,}000\ hrs,\ T_X = 60^\circ C$$

$$\phi D \times L = 10 \times 20\ (mm),\ B = 0.0019,\ A = 7.1cm^2$$

$$\Delta T_X = \frac{0.860A^2 \bullet 0.14\Omega}{0.0019 \bullet 7.1\,cm^2} = 7.06^\circ C$$

$$L_X = 2{,}000\ hrs \bullet 2^{\frac{105^\circ C - (60^\circ C + 7.06^\circ C)}{10}}$$

$$L_X = 27{,}665\ hrs = 3.1\ yrs$$

The total lifetime and operating duty cycle of a product must first be defined in order to generate a capacitor's actual total operating hours. Then the lifetime equation (A1) is used to select a filter capacitor that can meet these operating conditions. Lap top computers, for instance,

ϕD × L (mm × mm)	A (cm^2)	B ($W/cm^2/°C$)	B • A (W/°C)
5 × 11	1.9	0.00210	0.00399
6.3 × 11	2.5	0.00208	0.00520
8 × 11.5	3.3	0.00206	0.00680
8 × 14	4.0	0.00200	0.00800
10 × 12.5	4.7	0.00201	0.00945
10 × 16	5.8	0.00198	0.0115
10 × 20	7.1	0.00190	0.0135
12.5 × 20	9.1	0.00182	0.0166
12.5 × 25	11.0	0.00178	0.0196
13 × 20	9.5	0.00182	0.0173
13 × 25	11.5	0.00178	0.0205
13 × 30	13.5	0.00170	0.0230
16 × 25	14.6	0.00164	0.0240
16 × 31.5	17.8	0.00156	0.0276
16 × 35.5	19.9	0.00146	0.0291
16 × 40	22.1	0.00140	0.0310
18 × 31.5	20.3	0.00146	0.0297
18 × 35.5	22.6	0.00140	0.0317
18 × 40	25.1	0.00130	0.0327
18 × 45	26.0	0.00122	0.0342
22.4 × 30	25.0	0.00130	0.0325
22.4 × 40	32.1	0.00112	0.0360
22.4 × 50	39.1	0.00102	0.0399
25 × 30	28.5	0.00120	0.0342
25 × 40	36.3	0.00106	0.0385
25 × 50	44.2	0.00097	0.0429
30 × 40	44.8	0.00097	0.0435
30 × 50	54.2	0.00090	0.0488
30 × 60	63.6	0.00085	0.0541
35 × 40	53.6	0.00090	0.0482
35 × 50	64.6	0.00084	0.0543
35 × 60	75.6	0.00080	0.0605
35 × 70	86.6	0.00076	0.0658
35 × 80	97.5	0.00074	0.0722
35 × 100	119.5	0.00070	0.0837
40 × 50	74.5	0.00080	0.0603
40 × 60	88.0	0.00075	0.0660
40 × 70	100.6	0.00074	0.0744
40 × 80	113.1	0.00072	0.0814
40 × 90	125.7	0.00070	0.0880
40 × 100	138.2	0.00070	0.0967
40 × 110	150.8	0.00070	0.106
50 × 60	113.8	0.00072	0.0819
50 × 70	129.6	0.00070	0.0907
50 × 80	145.3	0.00070	0.102
50 × 90	161.0	0.00070	0.113
50 × 100	176.7	0.00070	0.124
50 × 110	192.4	0.00070	0.135
50 × 120	208.1	0.00070	0.146

(Courtesy of United Chemi-Con)

Figure A5. Heat Transfer Constants for Various Case Sizes

might be expected to operate no more than four hours a day on an average, so a ten year life is only 15,000 actual operating hours.

A capacitor's ripple current multiplier can be used to increase the maximum allowable ripple current, allowing smaller size capacitors to be used. However, this method of increasing the maximum ripple current rating assumes load life is kept constant, so it must be used with extreme caution. For example, a Nichicon PL series capacitor rated at 1A RMS at 105°C has a load life of 3,000 hours and a ripple current multiplier of 2.2 at 65°C. If the ripple current multiplier is used, the capacitor's ripple current rating can be increased to 2.2A RMS as long as the operating temperature does not exceed 65°C; however, the load life of the capacitor is still 3,000 hours. Eighteen weeks is a rather short operating life.

References

1. United Chemi-Con Inc., "Understanding Aluminum Electrolytic Capacitors."
2. Nichicon (America) Corp., "Technical Notes on Aluminum Electrolytic Capacitors."

Capacitor Manufacturers

1. Nichicon (America) Corporation
927 East State Parkway
Schaumburg, IL 60195
(708) 843-7500

2) Sanyo Video Components (USA) Corporation
1201 Sanyo Avenue
San Diego, CA 92073
(619) 661-6322

3) United Chemi-Con, Inc.
9801 West Higgins Road
Rosemount, IL 60018
(708) 696-2000

4) Sprague Electric Company
Aluminum Electrolytic Div.
9800 Kincey Ave. Suite 100
Huntersville, NC 28078
(704) 875-8070

5) Kemet Electronics
P.O. Box 5928
Greenville, SC 29606
(803) 675-1760

6) Marcon
998 Forest Edge Drive
Vernon Hills, IL 60061
(708) 913-9980

7) Wima
2269 Saw Mill River Rd
Bldg. 4C
P.O. Box 217
Elmsford, NY 10523
(914) 347-2474

APPENDIX B

Measuring RMS Current in Switching Regulator Filter Capacitors

One of the most critical parameters on a capacitor's data sheet is its ripple current rating, specified in RMS current. The operating ripple current must be accurately determined in order to select the proper size capacitor. The current waveforms are usually square or triangular and their RMS value can be determined by either measurement or an analytical approach.

The preferred method of determining ripple current is to measure it. This can easily be accomplished using a true-RMS voltmeter (HP3400A or Fluke 8920A or equivalent) and a current probe (Tektronix P6021).

Thermally based RMS voltmeters provide the high bandwidth and crest factor capability necessary to accurately measure the RMS current through a filter capacitor. The RMS voltmeter's bandwidth must exceed 1MHz, since current transients can exceed 100A/μs. Do not use average responding or logarithmic based RMS voltmeters. Most hand held voltmeters are average responding and only good for low frequency sinewaves, typically under 10kHz. The logarithmic approach measures true RMS, but bandwidths are limited to well below 1MHz.

There are two types of current probes available: the traditional AC only probe and the true DC Hall Effect type. AC only current probes (P6021) use a transformer to convert current flux into AC signals and have a frequency response from a few hundred hertz to 60MHz. Therefore, do not use a P6021 if the ripple current waveform has a low frequency component. Hall Effect current probes (P6042) include semiconductors to provide a frequency response from DC to 50MHz. Both types have saturation limitations which, when exceeded, cause erroneous results.

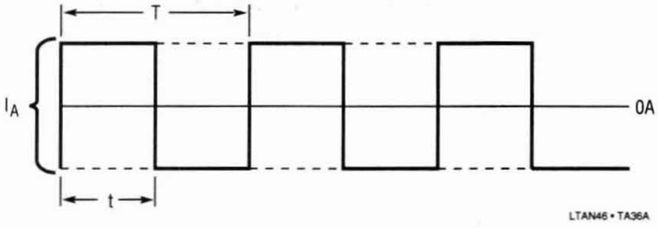
The following procedure will accurately determine the maximum RMS current for a capacitor no matter how complex the ripple current waveforms are. The current probe is clipped on the capacitor's lead and the other end of the probe is connected to the RMS voltmeter. Set the P6021 terminator to its 10mA/mV scale. It is always a good idea to view the current waveform on an oscilloscope to verify that the converter is working properly before measuring the RMS voltage. Next, apply maximum load current to the output of the regulator. The RMS current can be calculated by multiplying the current probe scale factor by the RMS voltmeter reading:

I_{RMS} = Scale Factor * V_{RMS} Reading
10mA/mV * 100mV = 1A RMS

Vary the switching regulator's input voltage over its entire operating range. The maximum RMS voltage reading will be the worst case operating condition for the capacitor. Select the capacitor based on this RMS current reading.

If a true RMS voltmeter is not available, the RMS current can be estimated by analyzing the capacitor ripple current waveform. Capacitor RMS current waveforms vary for different converter topologies, and between input and output capacitors.

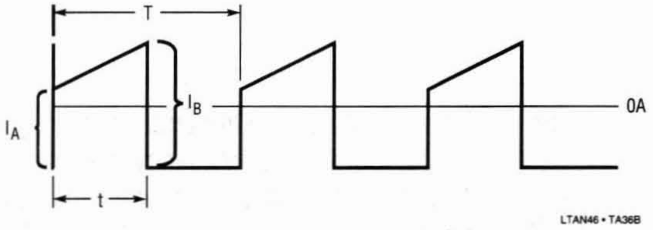
Figure B1 shows some common filter capacitor waveforms and equations used to derive the values of I_{RMS}. Current waveforms generally fall into one of four cases. Case 1 is not an actual ripple current waveform, but it is often used to approximate the RMS current since only two variables are used. Here, worst case ripple occurs at 50% duty cycle. Case 2 is the ripple current waveform for an



$$I_{RMS} = I_A\sqrt{DC(1-DC)}$$

$$DC = \frac{t}{T}$$

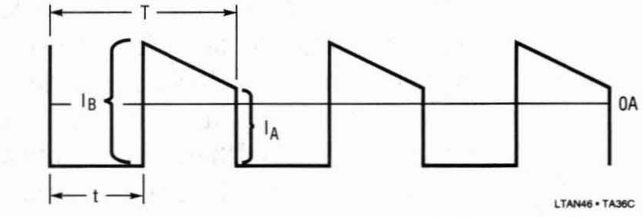
Case 1. Rectangular



$$I_{RMS} = \sqrt{DC\left[\frac{I_A^2 + I_A \bullet I_B + I_B^2}{3} - \frac{DC}{4}(I_A + I_B)^2\right]}$$

$$DC = \frac{t}{T}$$

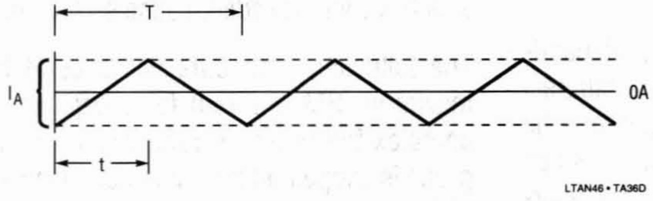
Case 2. Trapezoid



$$I_{RMS} = \sqrt{(1-DC)\left[\frac{I_A^2 + I_A \bullet I_B + I_B^2}{3} - \frac{(1-DC)}{4}(I_A + I_B)^2\right]}$$

$$DC = \frac{t}{T}$$

Case 3. Trapezoid



$$I_{RMS} = \frac{I_A}{\sqrt{12}}$$

Case 4. Saw Tooth

Figure B1. Typical Filter Capacitor Ripple Current Waveforms

input capacitor for buck, buck-boost, or flyback topology. Case 3 is for an output capacitor for boost, buck-boost, or flyback topology. Case 4's waveform is for the input capacitor for boost and output capacitor for buck mode.

Figure B2 summarizes these equations and shows equations that can be used to make a quick approximation of ripple current. Here the RMS current is calculated from output current and duty cycle. As long as the ratio of I_B over I_A is < 2, these equations approximate the RMS current to within 10% of the actual value.

There exists a little confusion about where zero current is located on the capacitor's current waveform. Figure B3 shows an input capacitor's ripple current for a buck, buck-boost and flyback topology. The zero point is always in the middle since the average current through the capacitor must be zero, assuming negligible leakage current. The two shaded areas are equal because the average current flowing into the capacitor equals the average outgoing current.

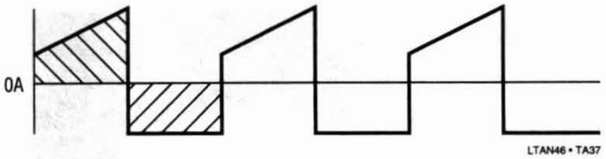


Figure B3. The Average Current Through the Filter Capacitor is Zero

In many switching regulator applications the input supply consists of a 60Hz single phase step-down transformer followed by a rectifier whose output is smoothed by a filter capacitor. Figure B4 shows the filter capacitor's ripple current waveform for a full wave bridge rectifier. The ripple current flowing through the input capacitor consists of the high frequency switching ripple current superimposed on the120Hz ripple (trace A). Trace B details the content of the 100kHz ripple current which is produced by a LT1074 buck switching regulator.

To select the proper size input capacitor, the effects of the 120Hz and the 100kHz ripple current waveforms must be considered. The best way to determine the input capacitor's

TOPOLOGY	FLYBACK	BOOST	BUCK	BUCK-BOOST
C_{IN} I_{RMS}*	$\sqrt{DC\left[\frac{I_A{}^2+I_A \bullet I_B+I_B{}^2}{3}-\frac{(DC)}{4}\left(I_A+I_B\right)^2\right]}$	$\frac{I_A}{\sqrt{12}}$	$\sqrt{DC\left[\frac{I_A{}^2+I_A \bullet I_B+I_B{}^2}{3}-\frac{(DC)}{4}\left(I_A+I_B\right)^2\right]}$	
C_{OUT} I_{RMS}*	$\sqrt{(1-DC)\left[\frac{I_A{}^2+I_A \bullet I_B+I_B{}^2}{3}-\frac{(1-DC)}{4}\left(I_A+I_B\right)^2\right]}$		$\frac{I_A}{\sqrt{12}}$	$\sqrt{(1-DC)\left[\frac{I_A{}^2+I_A \bullet I_B+I_B{}^2}{3}-\frac{(1-DC)}{4}\left(I_A+I_B\right)^2\right]}$
C_{IN} $\approx I_{RMS}$*	$\frac{I_{OUT} \bullet V_{OUT}}{V_{IN}}\sqrt{\frac{1-DC}{DC}}$	$0.3\Delta I$	$I_{OUT}\sqrt{DC-(DC)^2}$	$\frac{I_{OUT} \bullet V_{OUT}}{V_{IN}}\sqrt{\frac{1-DC}{DC}}$
C_{OUT} $\approx I_{RMS}$*	$I_{OUT}\sqrt{\frac{DC}{1-DC}}$	$I_{OUT}\sqrt{\frac{DC}{1-DC}}$	$0.3\Delta I$	$I_{OUT}\sqrt{\frac{DC}{1-DC}}$
ΔI		$\frac{V_{IN} \bullet DC}{L \bullet f}$	$\frac{\left(V_{IN}-V_{OUT}\right) \bullet DC}{L \bullet f}$	
DC	$\frac{V_{OUT}}{V_{OUT}+N\,V_{IN}}$	$\frac{V_{OUT}-V_{IN}}{V_{OUT}}$	$\frac{V_{OUT}}{V_{IN}}$	$\frac{V_{OUT}}{V_{OUT}+V_{IN}}$

*Refer to Figure B1 for details on I_A and I_B

Figure B2. Filter Capacitor RMS Current Equations

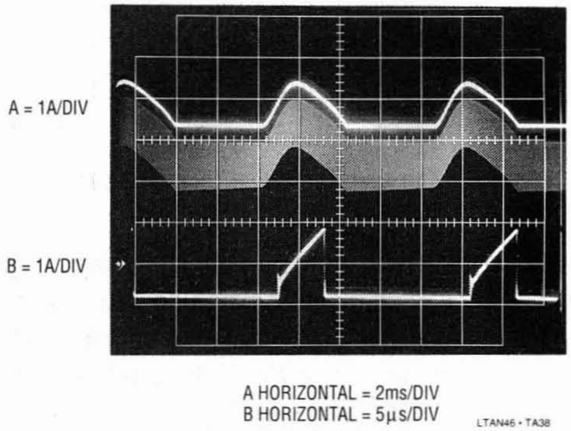


Figure B4. Input Capacitor's Ripple Current Waveform When Input Supply is a 60Hz Full Wave Bridge Circuit

ripple current is to measure it. A DC current probe must be used to measure the 120Hz content of the waveform. An AC current probe can measure the 100kHz ripple but can not accurately measure the 120Hz ripple since its lower bandwidth limit is a few hundred hertz. The HP3400A RMS voltmeter can be used here since its frequency range extends from 10Hz to10MHz.

APPENDIX C

Bipolar Power Switch Conduction Losses

Power transistor conduction losses limit power conversion efficiency. It can be a substantial limitation when input voltage is low. Conduction losses include both switch driver and switch on losses. Switch driver losses occur because bipolar devices require base current to turn on and switch on losses are a product of the power transistor saturation characteristic.

Figure C1 shows the type and location of the power switch used in the LT1070 step-up (Case 1) and LT1074 step-down (Case 2) converters. These two switching configurations have different power transistor architectures and saturation characteristics. The boost circuit, implemented with an LT1070, uses a ground referred NPN transistor as the switch device, whereas the buck circuit, implemented with an LT1074, uses a supply referred composite PNP high side switch.

Figure C2 shows the saturation characteristics for each power transistor. The switch voltage drop for the composite PNP in the LT1074 (Case 2) is noticeably higher than the NPN used in the LT1070 (Case 1) because of the way the switch is configured.

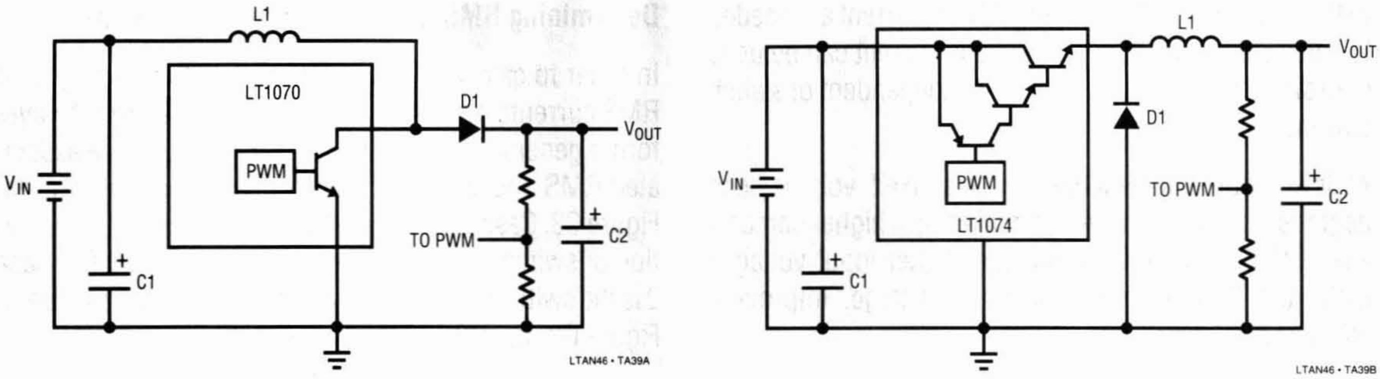
NPN Switch

Figure C2, Case 1 shows Current vs Voltage Characteristics of the LT1070 NPN power switch. In saturation, the NPN switch can be modeled as resistance. The slope of the curve indicates switch on resistance, which is found by dividing the collector to emitter voltage by the collector current. The on resistance of the NPN determines both its voltage drop and power dissipation. The NPN switch conduction loss can be calculated from:

$$P_C \approx (I_{RMS})^2 \bullet R_{ON} \qquad (C1)$$

Another dissipation factor associated with the NPN transistor is the base drive loss. Driving the base requires current, resulting in power loss in a driver transistor.

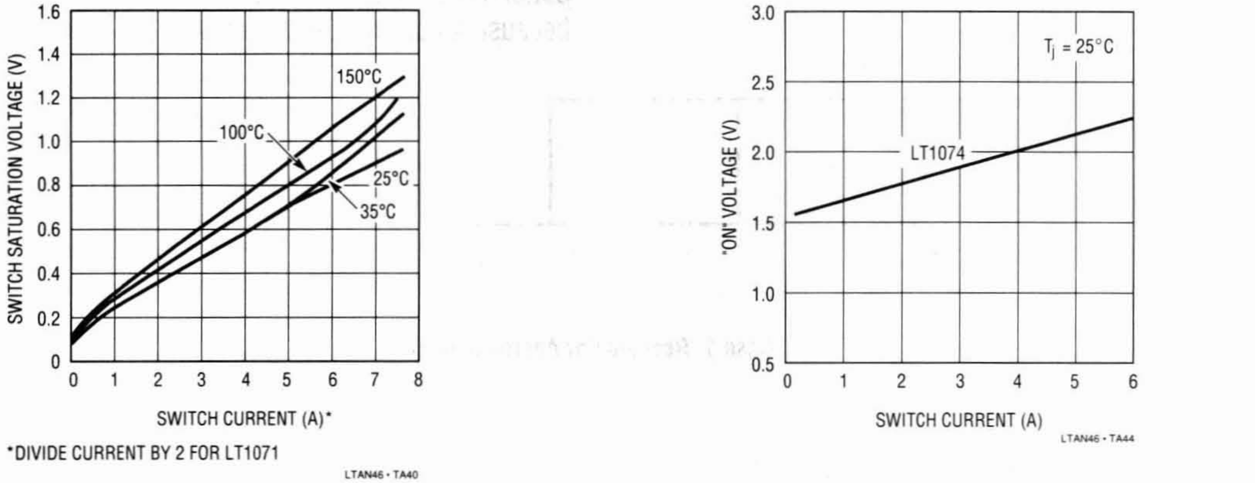
To optimize efficiency, the LT1070 uses a constant beta drive circuit to control base current. This scheme provides a base drive that is proportional to the collector current. The LT1070 operates with a constant beta drive of 40, which means with a collector current of 5A, the base drive current would be 125mA, but at I_C=1A, I_B is only 25mA. This technique is very efficient over a wide range of collector currents.



Case 1. LT1070 Step-Up (Boost) Converter

Case 2. LT1074 Step-Down (Buck) Converter

Figure C1. Types and Location of Bipolar Power Switches



Case 1. LT1070 Switch Current vs Voltage Characteristics

Case 2. LT1074 Switch Current vs Voltage Characteristics

Figure C2. Switch Current vs Voltage Characteristics of Bipolar Power Switches

The base drive current is drawn from the input pin of the LT1070 when the power transistor is on; therefore, driver losses are duty cycle dependent. The LT1070 dissipation because of base drive losses becomes:

$$P_{DRV} = V_{IN} \bullet I_{SW}/40 \bullet DC \qquad (C2)$$

The total LT1070 power dissipation is the sum of the switch conduction and driver losses and is given by:

$$P_{TOT} = (I_{RMS})^2 \bullet R_{ON} + V_{IN} \bullet I_{AVG}/40 \qquad (C3)$$

At low switch currents and high input voltages, driver losses dominate; switch losses dominate at low input voltages and high switch currents.

Composite PNP Switch Conduction Losses

Figure C2, Case 2 shows the Current vs Voltage Characteristics of the LT1074 composite PNP power switch. Its power switch can be modeled by a resistance and a series offset voltage, typically 1.8V. The fixed 1.8V drop of the composite switch is made up of $2V_{BE}$ ($\approx$0.75V ea.) drops across the Darlington-connected NPN and a PNP saturation drop ($\approx$0.3V). The composite PNP power dissipation can be predicted by the following formula:

$$P_{D\,TOT} = 1.8V \bullet I_{AVG} + 0.1\Omega \bullet (I_{RMS})^2 \qquad (C4)$$

In this case, both the average and RMS current are needed to calculate power loss. The average current can be used here since the fixed voltage drop is independent of switch current.

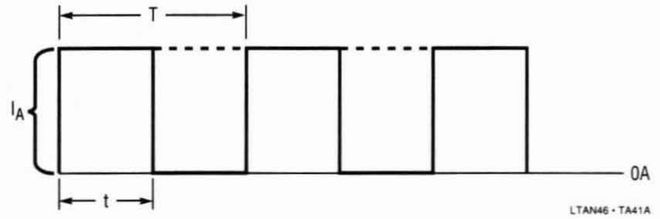
At low input voltages the switch's fixed voltage loss degrades efficiency because it makes up a higher percentage of the available input supply. Higher input voltages make the fixed loss a smaller percentage, improving efficiency.

The composite PNP high gain configuration needs only 5mA of driver current to fully saturate the switch. This small current introduces negligible loss.

Determining RMS and Average Switch Currents

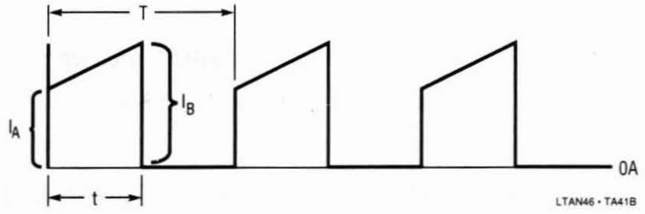
In order to calculate efficiency, the switch's average and RMS currents must be determined. Switch current waveforms generally look like those of Figure C3. The associated RMS and average current equations are also given. Figure C3, Case 1 can be used to make a quick approximation of switch RMS and average current. Figure C3, Case 2 is the switch current waveform for continuous mode and Figure C3, Case 3 for discontinuous mode.

Using the thermal RMS voltmeter to measure switch RMS current as discussed in appendix B will work here, but **the RMS meter must be able to measure DC. The DC current probe must be properly zeroed!** For example, the Fluke 8920A RMS voltmeter will work and the HP 3400A will not because it has an AC-coupled input.



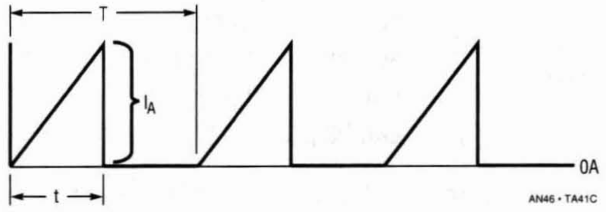
$$I_{RMS} = I_A\sqrt{DC}$$
$$I_{AVG} = DC \bullet I_A$$
$$DC = \frac{t}{T}$$

Case 1. Rectangular Approximation



$$I_{RMS} = \sqrt{DC\left[\frac{I_A^{\,2} + I_A \bullet I_B + I_B^{\,2}}{3}\right]}$$
$$I_{AVG} = \frac{DC\left(I_A + I_B\right)}{2}$$
$$DC = \frac{t}{T}$$

Case 2. Trapezoid Continuous Mode



$$I_{RMS} = I_A\sqrt{\frac{DC}{3}}$$
$$I_{AVG} = \frac{DC \bullet I_A}{2}$$
$$DC = \frac{t}{T}$$

Case 3. Trapezoid Discontinuous Mode

Figure C3. Typical Switch Current Waveforms

APPENDIX D

Diode Conduction Losses

The output diode conduction loss is often the major source of power loss in switching regulators. It exhibits a forward voltage drop (V_f) which limits efficiency. Efficiency loss due to V_f is most significant at low output voltages, and should be as low as possible to optimize efficiency. At high output voltages, the forward voltage drop's effect on efficiency is small, because it makes up a very small percentage of output voltage.

For low output voltages, Schottky diodes are recommended over silicon diodes because they have a lower forward voltage drop for the same current rating. In a flyback topology with 5V output, a Schottky diode with a V_f of 0.6V introduces a loss of 12% of the output power; whereas a silicon diode with a V_f of 1.0V contributes a 20% loss. However, Schottkys are limited to low voltage applications since they have low Peak Inverse Voltage (PIV) limits.

Diode conduction loss can be approximated by the following formula:

$$P_D \approx I_{D\,AVG} \bullet V_f \qquad \text{(D1)}$$

$I_{D\,AVG}$: Average Diode Current

V_f: Diode forward voltage drop at average peak diode current ($I_{f\,AVG}$)

Power loss due to diode leakage current is assumed to be negligible.

The expression for P_D looks simple, but is deceiving because V_f is a function of the diode's instantaneous forward current (I_f), not average diode current ($I_{D\,AVG}$). The dependence of V_f on I_f is shown in Figure D1.

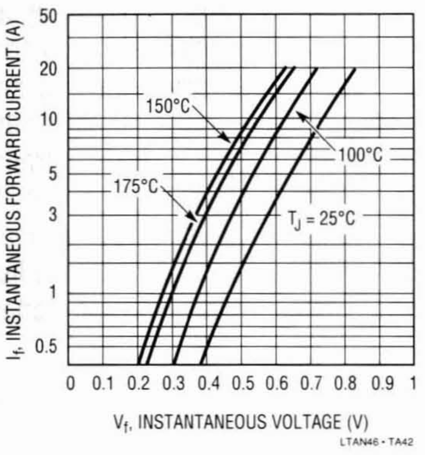
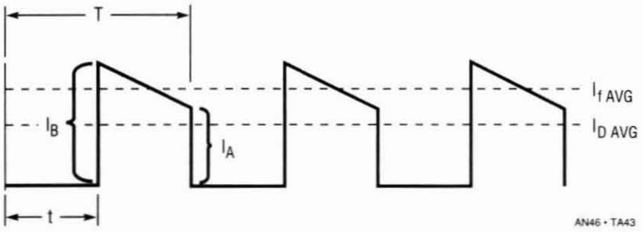


Figure D1. Typical Forward Voltage



$$I_{f\,AVG} = \frac{I_A + I_B}{2} \qquad \text{(D2)}$$

$$I_{D\,AVG} = (1 - DC)\frac{I_A + I_B}{2} \qquad \text{(D3)}$$

$$DC = \frac{t}{T} \qquad \text{(D4)}$$

Figure D2. Typical Diode Current Waveform

The value to use for I_f can be determined by examining the diode's current waveform. Figure D2 shows a typical diode current waveform. During the diode on-time, the diode current (I_f) is not constant; however, it can be approximated by taking the average peak diode current ($I_{f\,AVG}$) during this period and is given by Equation D2. This approximation assumes that the diode forward voltage drop is relatively linear for the different peak current values and is reasonably accurate if the ratio of I_B/I_A is less than three.

The average diode current ($I_{D\,AVG}$) can be determined by using Equation D3. In the boost, flyback and buck-boost topology the average diode current is equal to the output current (I_{OUT}), since the diode has to conduct the full output current. With the buck topology, the average diode current is only a fraction of the output current; therefore, it has lower conduction losses then the other converter topologies for the same output current level.

The most stressful condition for the output diode is overload or short circuit conditions. The internal current limit of the LT1070 is typically 8A at low switch duty cycles. This is almost a factor of 1.6 higher than the 5A rated switch current. If full load output current requires only a fraction of the 5A rated switch current, the ratio of diode short circuit current to full load current may be much higher than 2:1. **A regulator designed to withstand continuous short conditions must either use diodes rated for full short circuit current or it must incorporate some form of external current limiting.**

The boost topology does not provide short circuit protection, therefore the output diode and inductor can fail if the output is shorted to ground. If the converter must survive a short without blowing a fuse, other circuit techniques must be used.

Application Note 46

LT1432 High Efficiency Step-down Switching Regulator Controller

PRELIMINARY

October 1991

FEATURES

- Accurate preset +5 Volt output
- Up to 90% efficiency
- Optional burst mode for light loads
- Can be used with many LTC switching ICs
- Accurate ultra-low-loss current limit
- Operates with inputs from 6V to 30V
- Shutdown mode draws only 15µA
- Uses small 50µH inductor

APPLICATIONS

- Lap-top and palm-top computers
- Portable data gathering instruments
- DC bus distribution systems
- Battery powered digital widgets

DESCRIPTION

The LT1432 is a control chip designed to operate with the LT1070 family of switching regulators to make a very high efficiency 5V step-down (buck) switching regulator. A minimum of external components is needed.

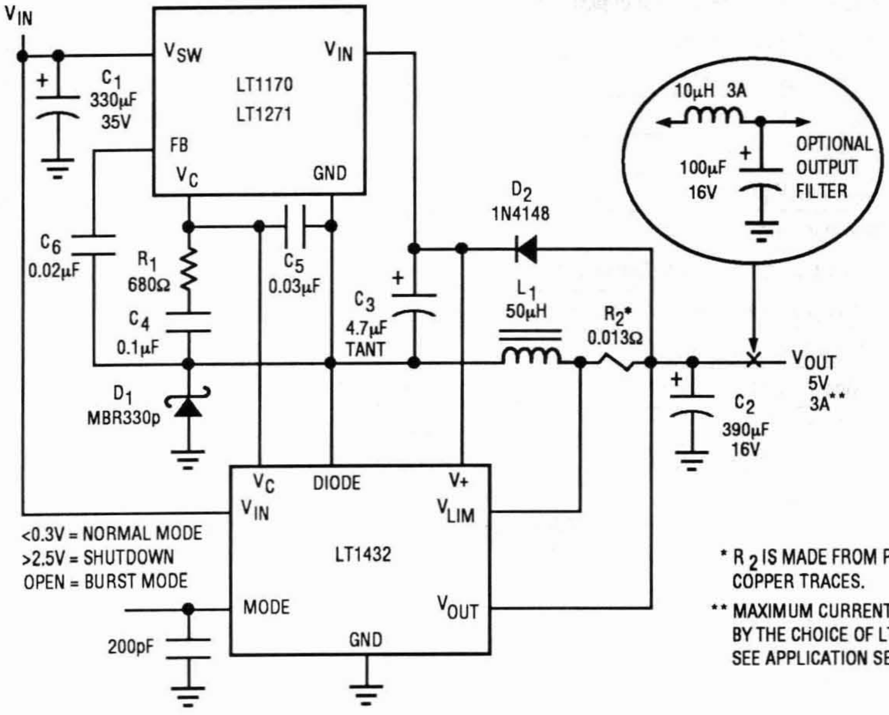
Included is an accurate current limit which uses only 60mV sense voltage and uses "free" pc board trace material for the sense resistor. Logic controlled electronic shutdown mode draws only 15µA battery current. The switching regulator operates down to 6 volts input.

The LT1432 has a logic controlled "burst" mode to achieve high efficiency at very light load currents (0 to 100mA) such as memory keep alive. In normal switching mode, the standby power loss is about 60mW, limiting efficiency at light loads. In burst mode, standby loss is reduced to approximately 15mW. Output current in this mode is typically in the 5-100mA range.

The LT1432 is available in 8-pin surface mount and DIP packages. The LT1070 family will also be available in a surface mount version of the 5-pin TO-220 package.

TYPICAL APPLICATION

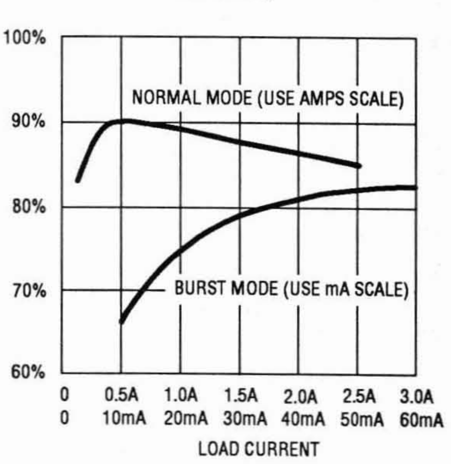
High Efficiency 5V Buck Convertor


VIN
VSW
VIN
LT1170
LT1271
FB
VC
GND
C1
330µF
35V
C6
0.02µF
R1
680Ω
C5
0.03µF
C4
0.1µF
D1
MBR330p
C3
4.7µF
TANT
D2
1N4148
L1
50µH
R2*
0.013Ω
10µH 3A
100µF
16V
OPTIONAL
OUTPUT
FILTER
VOUT
5V
3A**
C2
390µF
16V
VC
DIODE
V+
VIN
VLIM
LT1432
MODE
VOUT
GND
<0.3V = NORMAL MODE
>2.5V = SHUTDOWN
OPEN = BURST MODE
200pF

* R 2 IS MADE FROM PC BOARD COPPER TRACES.

** MAXIMUM CURRENT IS DETERMINED BY THE CHOICE OF LT1070 FAMILY. SEE APPLICATION SECTION.

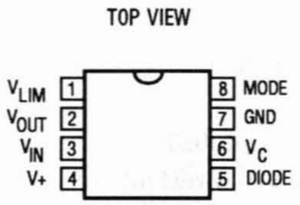
Efficiency



ABSOLUTE MAXIMUM RATINGS

V_{IN} Pin	30V
V+ Pin	40V
V_C	35V
V_{LIM} and V_{OUT} Pins	7V
V_{LIM} and V_{OUT} Pin Differential Voltage	0.5V
Diode Pin Voltage	30V
Mode Pin Current (Note 2)	1mA
Operating Ambient Temperature Range	0°C to 70°C
Storage Temperature Range	-65°C to 150°C
Lead Temperature (Soldering, 10 sec.)	300°C

PACKAGE/ORDER INFORMATION



N8 PACKAGE
8-LEAD PLASTIC DIP

S8 PACKAGE
8-LEAD PLASTIC SOIC

ORDER PART NUMBER

LT1432CN8
LT1432CS8

ELECTRICAL CHARACTERISTICS

V_C = 6V, V_{IN} = 6V, V+ = 10V, V_{DIODE} = 5V, I_C = 220µA, V_{LIM} = V_{OUT}, V_{MODE} = 0V, T_J = 25°C
Device is in standard test loop unless otherwise noted.

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Regulated output voltage		●	4.9	5.0	5.1	V
Output voltage line regulation	V_{IN} = 6V to 30V	●		5	20	mV
Input supply current (Note 1)	V_{IN} = 6V to 30V, V+ = Vin + 4V	●		0.3	0.5	mA
Quiescent output load current		●		0.9	1.2	mA
Mode pin current	V_{MODE} = 0V, (Current is out of pin)	●		30	50	µA
	V_{MODE} = 5V (shutdown)	●		15	30	µA
Mode pin threshold voltage (normal to burst)	I_{MODE} = 1µA out of pin	●	0.6	0.9	1.5	V
V_C pin saturation voltage	V_{OUT} = 5.5V (forced)	●		0.25	0.45	V
V_C pin maximum sink current	V_{OUT} = 5.5V (forced)	●	0.45	0.8	1.5	mA
V_C pin source current	V_{OUT} = 4.5V (forced)	●	40	60	100	µA
Current limit sense voltage	Device in current limit loop		56	60	64	mV
V_{LIM} pin current	Device in current limit loop (Current is out of pin)	●	30	45	70	µA
Supply current in shutdown	Vmode > 3V, Vin < 30V	●		15	40	µA
Burst mode output ripple	Device in burst test circuit			100		mV_{P-P}
Burst mode average output voltage	Device in burst test circuit	●	4.8	5	5.2	V
Clamp diode forward voltage	I_F = 1mA	●		0.5	0.65	V
Startup drive current	V_{OUT} = 4.5V (forced),V+=5V to 25V	●	30	45		mA

The ● denotes specifications which apply over the operating temperature range.

Note 1: Does not include current drawn by the LT1070 IC. See operating parameters in standard circuit.

Note 2: Breakdown voltage on the mode pin is 7V. External current must be limited to value shown.

LINEAR TECHNOLOGY
Application Note 47
August 1991

High Speed Amplifier Techniques

A Designer's Companion for Wideband Circuitry

Jim Williams

PREFACE

This publication represents the largest LTC commitment to an application note to date. No other application note absorbed as much effort, took so long or cost so much. This level of activity is justified by our belief that high speed monolithic amplifiers greatly interest users.

Historically, monolithic amplifiers have represented packets of inexpensive, precise and controllable gain. They have partially freed engineers from the constraints and frustrations of device level design. Monolithic operational amplifiers have been the key to practical implementation of high level analog functions. As good as they are, one missing element in these devices has been speed.

Devices presently coming to market are addressing monolithic amplifiers' lack of speed. They bring with them the ease of use and inherent flexibility of op amps. When Philbrick Researches introduced the first mass produced op amp in the 1950's (K2-W) they knew it would be used. What they couldn't possibly know was just how widely, and how many different types of applications there were. As good a deal as the K2-W was (I paid $24.00 for mine - or rather, my father did), monolithic devices are far better. The combination of ease of use, economy, precision and versatility makes modern op amps just too good to be believed.

Considering all this, adding speed to op amps' attractions seems almost certain to open up new application areas. We intend to supply useful high speed products and the level of support necessary for their successful application (such high minded community spirit is, of course, capitalism's deputy). We hope you are pleased with our initial efforts and look forward to working together.

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INTRODUCTION

Most monolithic amplifiers have been relatively slow devices. Wideband operation has been the province of discrete and hybrid technologies. Some fast monolithic amplifiers have been available, but the exotic and expensive processing required has inflated costs, precluding widespread acceptance. Additionally, many of the previous monolithic designs were incapable of high precision and prone to oscillation or untoward dynamics, making them unattractive.

Recent processing and design advances have made inexpensive, precision wideband amplifiers practical. Figure 1 lists some amplifiers, along with a summary of their characteristics. Reviewing this information reveals extraordinarily wideband devices, with surprisingly good DC characteristics. All of these amplifiers utilize standard op amp architecture, except the LT1223 and LT1228, which are so-called current mode feedback types (see Appendix H, "About Current Mode Feedback"). It is clear that the raw speed capabilities of these devices, combined with their inherent flexibility as op amps, permit a wide range of applications. What is required of the user is a familiarity with the devices and respect for the requirements of high speed circuitry.

This effort's initial sections are devoted to familiarizing the reader with the realities and difficulties of high speed circuit work. The mechanics and subtleties of achieving precision circuit operation at DC and low frequency have been well documented. Relatively little has appeared which discusses, in practical terms, how to get fast circuitry to work. In developing such circuits, even veteran designers sometimes feel that nature is conspiring against them. In some measure this is true. Like all engineering endeavors, high speed circuits can only work if negotiated compromises with nature are arranged. Ignorance of, or contempt for, physical law is a direct route to frustration. Mother Nature laughs at dilettantism and crushes arrogance without even knowing she did it. Even without Einstein's revelations, the world of high speed is full of surprises. Working with events measured in nanoseconds requires the greatest caution, prudence and respect for Mother Nature. Absolutely nothing should be taken for granted, because nothing is. Circuit design is very much the art of compromise with parasitic effects. The "hidden schematic" (this descriptive was originated by Charly Gullett of Intel Corporation) usually dominates the circuit's form, particularly at high speed.

In this regard, much of the text and appendices are directed at developing awareness of, and respect for, circuit parasitics and fundamental limitations. This approach is maintained in the applications section, where the notion of negotiated compromises is expressed in terms of resistor values and compensation techniques. Many of the application circuits use the amplifier's speed to improve on a standard circuit. Some utilize the speed to implement a traditional function in a non-traditional way, with attendant advantages. A (very) few operate at or near the state-of-the-art for a given circuit type, regardless of approach. Substantial effort has been expended in developing these examples and documenting their operation. The resultant level of detail is justified in the hope that it will be catalytic. The circuits should stimulate new ideas to suit particular needs, while demonstrating fast amplifiers' capabilities in an instructive manner.

PERSPECTIVES ON HIGH SPEED DESIGN

A substantial amount of design effort has made Figure 1's amplifiers relatively easy to use. They are less prone to oscillation and other vagaries than some much slower amplifiers. Unfortunately, laws of physics dictate that the circuit's *environment* must be properly prepared. The performance limits of high speed circuitry are often determined by parasitics such as stray capacitance, ground impedance and layout. Some of these considerations are present in digital systems where designers are comfortable describing bit patterns, delays and memory access times in terms of nanoseconds. Figure 2's test circuit provides valuable perspective on just how fast these amplifiers are. Here, the pulse generator (Trace A, Figure 3) drives a 74S04 Schottky TTL inverter (Trace B), an LT1223 op amp connected as an inverter (Trace C), and a 74HC04 high speed CMOS inverter (Trace D). The LT1223 doesn't fare too badly. Its delay and fall times are about 2ns slower than the 74S04, but significantly faster than the 74HC04. In fact, the LT1223 has completely finished its transition before the 74HC04 even begins to move! Linear circuits operating with this kind of speed make many engineers justifiably wary. Nanosecond domain linear circuits are widely associated with oscillations, mysterious shifts in

PARAMETER	LT1122	LT1190	LT1191	LT1192	LT1193 DIFFERENTIAL	LT1194 DIFFERENTIAL	LT1220	LT1221	LT1222	LT1223	LT1224
Slew Rate	60V/µs	450V/µs	450V/µs	450V/µs	450V/µs	450V/µs	250V/µs	250V/µs	200V/µs	1000V/µs	300V/µs
Bandwidth	14MHz	50MHz	90MHz	400MHz	70MHz	70MHz	45MHz	150MHz	350MHz	100MHz	45MHz
Delay-Rise Time	15ns-65ns	4ns-7ns	3.5ns-1.6ns	5ns-7ns	4ns-7ns	4ns-7ns	4ns-4ns	5ns-5ns	5ns-5ns	3.5ns-3.5ns	4ns-4ns
Settling Time	340ns-0.01%	100ns-0.1%	100ns-0.1%	80ns-0.1%	100ns-0.1%	100ns-0.1%	90ns-0.1%	90ns-0.1%	90ns-0.1%	75ns-0.1%	90ns-0.1%
Output Current	6mA	50mA	50mA	50mA	50mA	50mA	24mA	24mA	24mA	50mA	40mA
Offset	600µV	4mV	2mV	2mV	3mV	3mV	2mV	1mV	1mV	3mV	1mV
Drift	6µV/°C						20µV/°C	15µV/°C	10µV/°C		20µV/°C
Bias Current	75pA	500nA	500nA	500nA	500nA	500nA	300nA	300nA	300nA	3µA	6µA
Gain	500,000	22,000	45,000	200,000	Adjustable	10	20,000	50,000	100,000	90dB	80dB
Gain Error (Minimum Gain)				$A_{VMIN} = 10$	0.1%	0.1%		$A_{VMIN} = 4$	$A_{VMIN} = 10$		$A_{VMIN} = 1$
Gain Drift											
Power Supply	40V	$18V_{MAX}$	$18V_{MAX}$	$18V_{MAX}$	$18V_{MAX}$	$18V_{MAX}$	36V	36V	36V	$36V_{MAX}$	36V

Figure 1. Characteristics of Some Different Fast IC Amplifiers

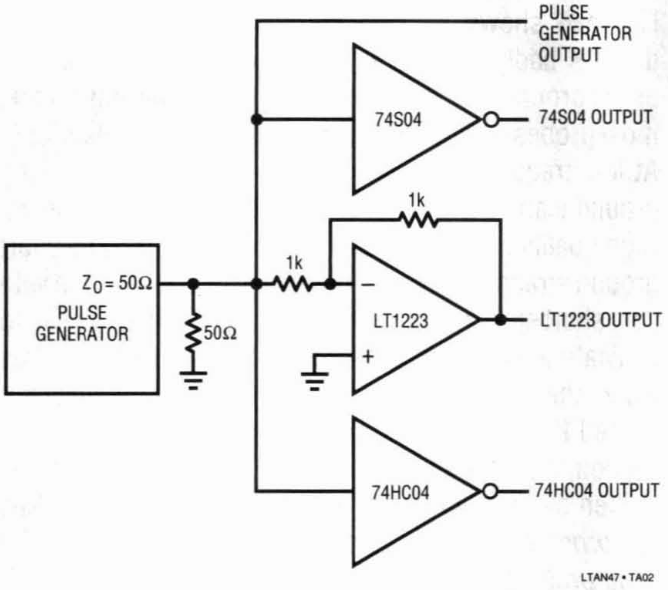

Figure 2. A Race Between the LT1223 Amplifier and Some Fast Logic Inverters

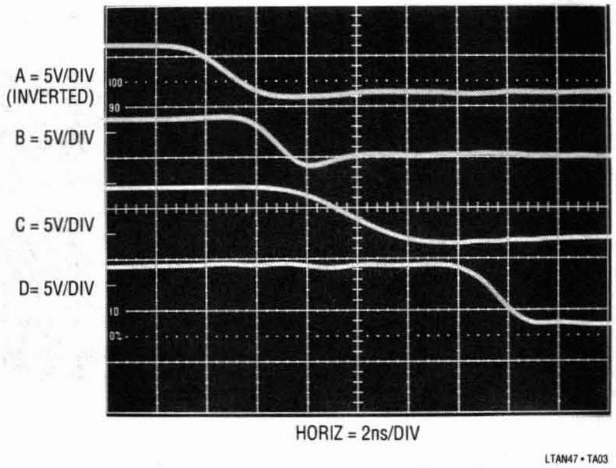

Figure 3. The Amplifier (Trace C) is 3ns Slower than 74S Logic (Trace B), but 5ns Faster than High Speed HCMOS (Trace D)!

circuit characteristics, unintended modes of operation and outright failure to function.

Other common problems include different measurement results using various pieces of test equipment, inability to make measurement connections to the circuit without inducing spurious responses, and dissimilar operation between two identical circuits. If the components used in the circuit are good and the design is sound, all of the above problems can usually be traced to failure to provide a proper circuit environment. To learn how to do this requires studying the causes of the aforementioned difficulties.

The following segments, "Mr. Murphy's Gallery of High Speed Amplifier Problems" and the "Tutorial Section", address this. The "Problems" section alerts the reader to trouble areas, while the "Tutorial" highlights theory and techniques which may be applied towards solving the problems shown. The tutorials are arranged in roughly the same order as the problems are presented.

MR. MURPHY'S GALLERY OF HIGH SPEED AMPLIFIER PROBLEMS

It sometimes seems that Murphy's Law dominates all physical law. For a complete treatise on Murphy's Law, see Appendix J, "The Contributions of Edsel Murphy to the Understanding of the Behavior of Inanimate Objects", by D.L. Klipstein. The law's consequences weigh heavily in high speed design. As such, a number of examples are given in the following discussion. The average number of phone calls we receive per month due to each "Murphy" example appears at the end of each figure caption.

Problems can start even before power is applied to the amplifier. Figure 4 shows severe ringing on the pulse edges at the output of an unterminated pulse generator cable. This is due to reflections and may be eliminated by terminating the cable. *Always terminate the source in its characteristic impedance when looking into cable or long PC traces. Any path over 1 inch long is suspect.*

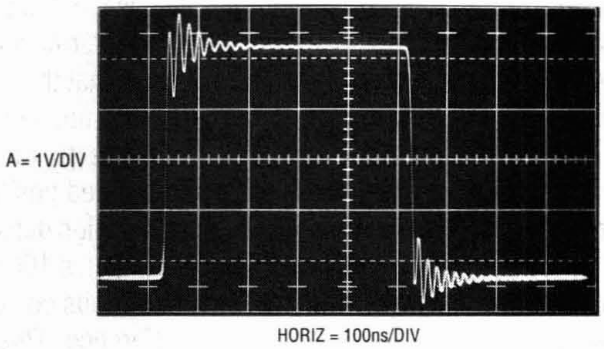

Figure 4. An Unterminated Pulse Generator Cable Produces Ringing Due to Reflections – 3 ☎

In Figure 5 the cable is terminated, but ripple and aberration are still noticeable following the high speed edge transitions. In this instance the terminating resistor's leads are lengthy (≈3/4"), preventing a high integrity wideband termination.

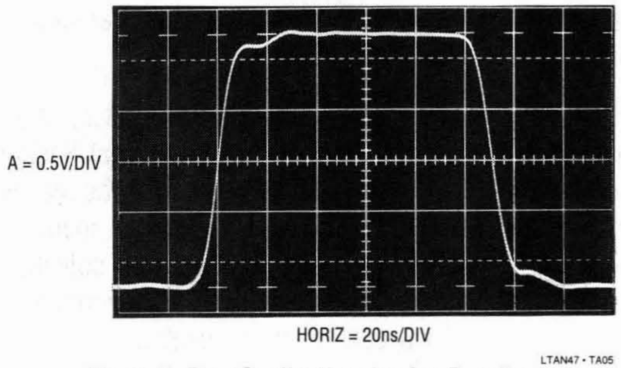

Figure 5. Poor Quality Termination Results in Pulse Corner Aberrations – 1 ☎

The best termination for 50Ω cable is the BNC coaxial type. These devices should not simply be resistors in an enclosure. Good grade 50Ω terminators maintain true coaxial form. They use a carefully designed 50Ω resistor with significant effort devoted to connections to the actual resistive element. In particular, the largest possible connection surface area is utilized to minimize high speed losses. While these type terminators are practical on the test bench, they are rarely used as board level components. In general, the best termination resistors for PC board use are carbon or metal film types with the shortest possible lead lengths. These resistor's end-cap connections provide better high speed characteristics than the rod-connected composition types. Wirewound resistors, because of their inherent and pronounced inductive characteristics, are completely unsuitable for high speed work. This includes so-called non-inductive types.

Another termination consideration is disposal of the current flowing through the terminator. The terminating resistor's grounded end should be placed so that the high speed currents flowing from it do not disrupt circuit operation. For example, it would be unwise to return terminator current to ground near the grounded positive input of an inverting op amp. The high speed, high density (5V pulses through a 50Ω termination generates 100mA current spikes) current flow could cause serious corruption of the desired zero volt op amp reference. This is another reason why, for bench testing, the coaxial BNC terminators are far preferable to discrete, breadboard mounted resistors. With BNC types in use the termination current returns directly to the source generator and never flows in the breadboard. (For more information see the Tutorial section.) *Select terminations carefully and evaluate the effects of their placement in the test set-up.*

Figure 6 shows an amplifier output which rings and distorts badly after rapid movement. In this case, the probe ground lead is too long. For general purpose work, most probes come with ground leads about 6 inches long. At low frequencies this is fine. At high speed, the long ground lead looks inductive, causing the ringing shown. High quality probes are always supplied with some short ground straps to deal with this problem. Some come with very short spring clips which fix directly to the probe tip to facilitate a low impedance ground connection. For fast work, the ground connection to the probe should not exceed 1 inch in length. (Probes are covered in the Tutorial section; also see Appendix A, "ABC's of Probes", guest written by the engineering staff of Tektronix, Inc.). *Keep the probe ground connection as short as possible. The ideal probe ground connection is purely coaxial. This is why probes mated directly to board mounted coaxial connectors give the best results.*

In Figure 7 the probe is properly grounded, but a new problem pops up. This photo shows an amplifier output

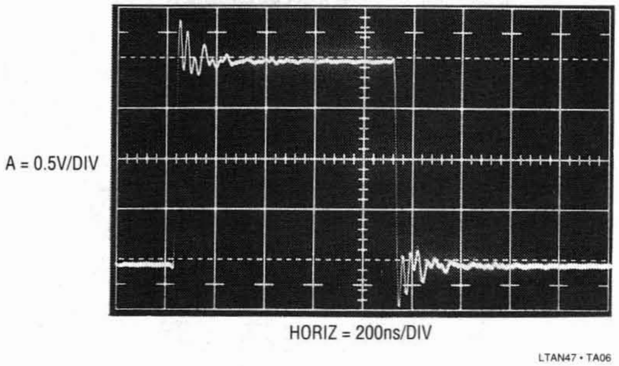

Figure 6. Poor Probe Grounding Badly Corrupts the Observed Waveform – 53 ☎

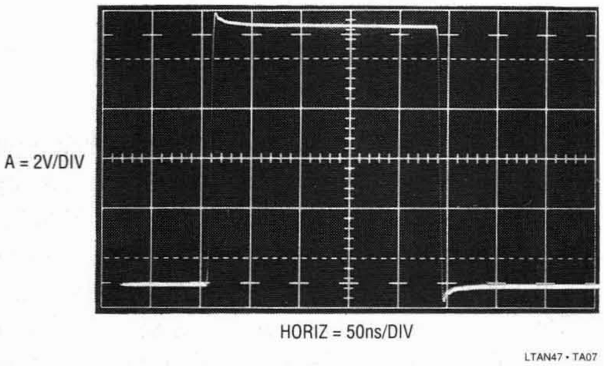

Figure 7. Improper Probe Compensation Causes Seemingly Unexplainable Amplitude Error – 12 ☎

excursion of 11V — quite a trick from an amplifier running from ±5V rails. This is a commonly reported problem in high speed circuits and can be quite confusing. It is not due to suspension of natural law, but is traceable to a grossly miscompensated or improperly selected oscilloscope probe. *Use probes which match your oscilloscope's input characteristics and compensate them properly.* (For discussions on probes, see Appendix A, "ABC's of Probes", guest written by the engineering staff of Tektronix, Inc. and the Tutorial section.) Figure 8 shows another probe-induced problem. Here the amplitude seems correct but the amplifier appears slow with pronounced edge rounding. In this case, the probe used is too heavily compensated or slow for the oscilloscope. Never use 1X or straight probes. Their bandwidth is 20MHz or less and capacitive loading is high. *Check probe bandwidth to ensure it is adequate for the measurement. Similarly, use an oscilloscope with adequate bandwidth.*

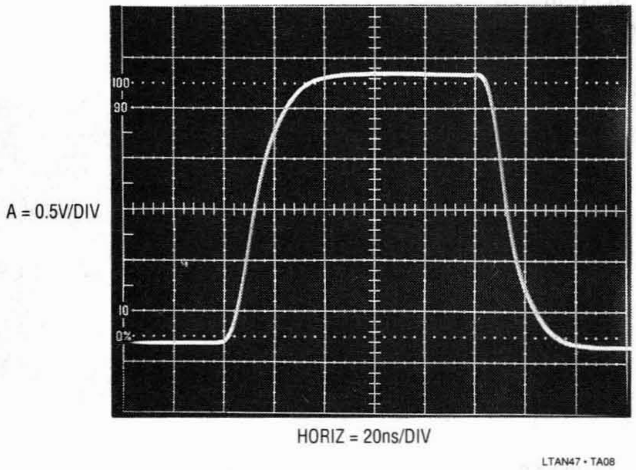

Figure 8. Overcompensated or Slow Probes Make Edges Look Too Slow – 2 ☎

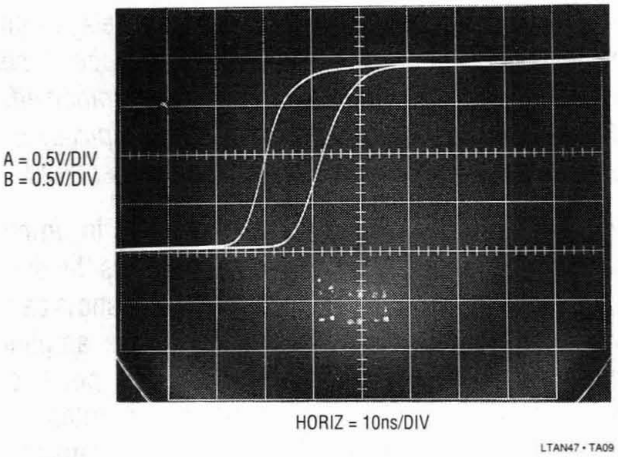

Figure 9. Probes with Mismatched Delays Produce Apparent Time Skewing in the Display – 4 ☎

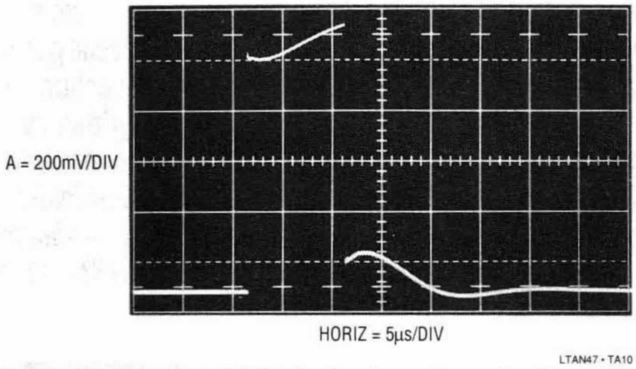

Figure 10. Overdriven FET Probe Produces Excessive Waveform Distortion and Tailing. Saturation Effects can Also Cause Delayed Response – 1 ☎

Mismatched probes account for the apparent excessive amplifier delay in Figure 9. Delay of almost 12ns (Trace A is the input, Trace B the output) is displayed for an amplifier specified at 6ns. Always keep in mind that various types of probes have different signal transit delay times. At high sweep speeds, this effect shows up in multi-trace displays as time skewing between individual channels. Using similar probes will eliminate this problem, but measurement requirements often dictate dissimilar probes. In such cases the differential delay should be measured and then mentally factored in to reduce error when interpreting the display. It is worth noting that active probes, such as FET and current probes, have signal transit times as long as 25ns. A fast 10X or 50Ω probe delay can be inside 3ns. *Account for probe delays in interpreting oscilloscope displays.*

The difficulty shown in Figure 10 is a wildly distorted amplifier output. The output slews quickly, but the pulse top and bottom recoveries have lengthy, tailing responses. Additionally, the amplifier output seems to clip well below its nominal rated output swing. A common oversight is responsible for these conditions. A FET probe monitors the amplifier output in this example. The probe's common-mode input range has been exceeded, causing it to overload, clip and distort badly. When the pulse rises, the probe is driven deeply into saturation, forcing internal circuitry away from normal operating points. Under these conditions the displayed pulse top is illegitimate. When the output falls, the probe's overload recovery is lengthy and uneven, causing the tailing. More subtle forms of FET probe overdrive may show up as extended delays with no obvious signal distortion. *Know your FET probe. Account for the delay of its active circuitry. Avoid saturation effects due to common-mode input limitations (typically ±1V). Use 10X and 100X attenuator heads when required.*

Figure 11's probe-caused problem results in amplifier output peaking and ringing. In other respects the display is acceptable. This output peaking characteristic is caused by a second 10X probe connected to the amplifier's summing junction. Because the summing point is so central to analyzing op amp operation, it is often monitored. At high speed the 10pF probe input capacitance causes a significant lag in feedback action, forcing the amplifier to overshoot and hunt as it seeks the null point. Minimizing this effect calls for the lowest possible probe input capacitance, mandating FET types or special passive probes. (Probes are covered in the Tutorial section; also see Appendix A, "ABC's of Probes", guest written by the engineering staff of Tektronix, Inc.). *Account for the effects of probe capacitance, which often dominates its impedance characteristics at high speeds. A standard 10pF 10X probe forms a 10ns lag with a 1KΩ source resistance.*

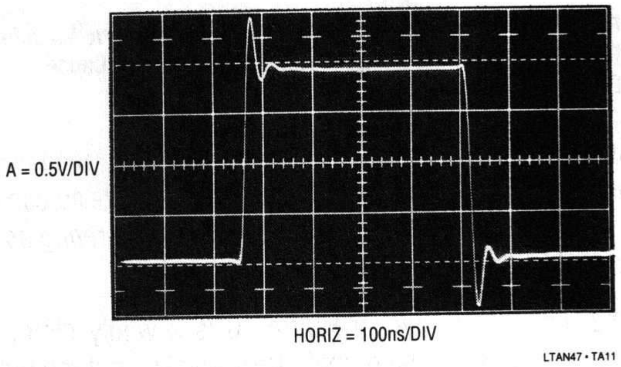

Figure 11. Effect of a 10X, 10pF 'Scope Probe at the Summing Point – 2 ☎

A peaked, tailing response is Figure 12's characteristic. The photo shows the final 40mV of a 2.5V amplifier excursion. Instead of a sharp corner which settles cleanly, peaking occurs, followed by a lengthy tailing decay. This waveform was recorded with an inexpensive off-brand 10X probe. Such probes are often poorly designed, and constructed from materials inappropriate for high speed work. The selection and integration of materials for wideband probes is a specialized and difficult art. Substantial design effort is required to get good fidelity at high speeds. *Never use probes unless they are fully specified for wideband operation. Obtain probes from a vendor you trust.*

Figure 13 shows the final movements of an amplifier output excursion. At only 1mV per division the objective is to view the settling residue to high resolution. This response is characterized by multiple time constants, nonlinear slew recovery and tailing. Note also the high speed event just before the waveform begins its negative going transition. What is actually being seen is the oscilloscope recovering from excessive overdrive. Any observation that requires off-screen positioning of parts of the waveform should be approached with the greatest caution. Oscilloscopes vary widely in their response to overdrive, bringing displayed results into question. Complete treatment of high resolution settling time measurements and oscilloscope overload characteristics is given in the Tutorial section, "About Oscilloscopes" and Appendix B "Measuring Amplifier Settling Time". *Approach all oscilloscope*

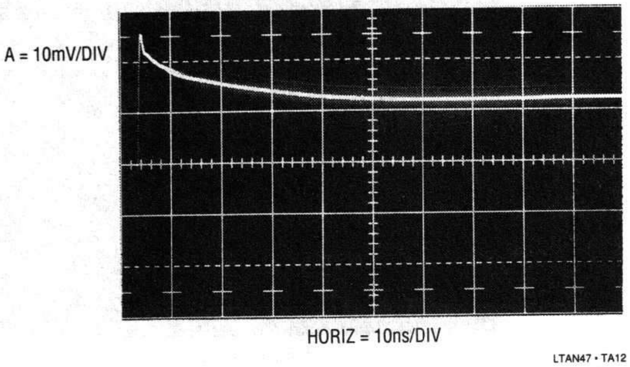

Figure 12. Poor Quality 10X Probe Introduces Tailing – 2 ☎

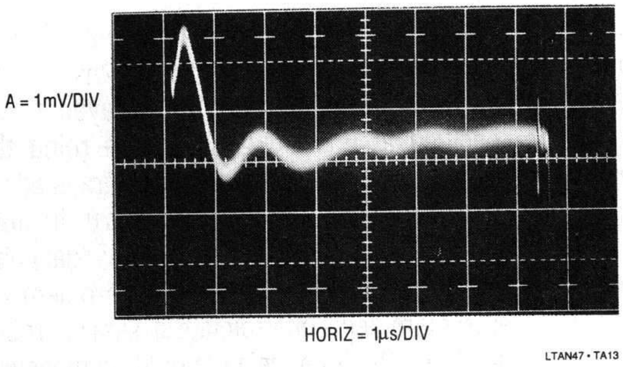

Figure 13. Overdriven Oscilloscope Display Says More About the Oscilloscope than the Circuit it's Connected to – 6 ☎

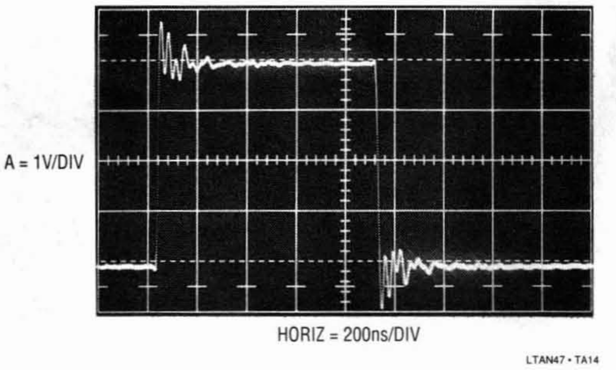

Figure 14. Instabilities Due to No Ground Plane Produce a Display Similar to a Poorly Grounded Probe – 62 ☎

measurements which require off-screen activity with caution. Know your instrument's capabilities and limitations.

Sharp eyed readers will observe that Figure 14 is a duplicate of Figure 6. Such lazy authorship is excusable because almost precisely the same waveform results when no ground plane is in use. A ground plane is formed by using a continuous conductive plane over the surface of the circuit board. (The theory behind ground planes is discussed in the Tutorial section). The only breaks in this plane are for the circuit's necessary current paths. The ground plane serves two functions. Because it is flat (AC currents travel along the surface of a conductor) and covers the entire area of the board, it provides a way to access a low inductance ground from anywhere on the board. Also, it minimizes the effects of stray capacitance in the circuit by referring them to ground. This breaks up potential unintended and harmful feedback paths. *Always use a ground plane with high speed circuitry.*

By far the most common error involves power supply bypassing. Bypassing is necessary to maintain low supply impedance. DC resistance and inductance in supply wires and PC traces can quickly build up to unacceptable levels. This allows the supply line to move as internal current levels of the devices connected to it change. This will almost always cause unruly operation. In addition, several devices connected to an unbypassed supply can "communicate" through the finite supply impedances, causing erratic modes. Bypass capacitors furnish a simple way to eliminate this problem by providing a local reservoir of energy at the device. The bypass capacitor acts as an electrical flywheel to keep supply impedance low at high frequencies. The choice of what type of capacitors to use for bypassing is a critical issue and should be approached carefully (see Tutorial, "About Bypass Capacitors"). An unbypassed amplifier with a 100Ω load is shown in Figure 15. The power supply the amplifier sees at its terminals has high impedance at high frequency. This impedance forms a voltage divider with the amplifier and its load, allowing the supply to move as internal conditions in the comparator change. This causes local feedback and oscillation occurs. *Always use bypass capacitors.*

In Figure 16 the 100Ω load is removed, and a pulse output is displayed. The unbypassed amplifier responds surprisingly well, but overshoot and ringing dominate. *Always use bypass capacitors.*

Figure 17's settling is noticeably better, but some ringing remains. This response is typical of lossy bypass capacitors, or good ones placed too far away from the amplifier. *Use good quality, low loss bypass capacitors, and place them as close to the amplifier as possible.*

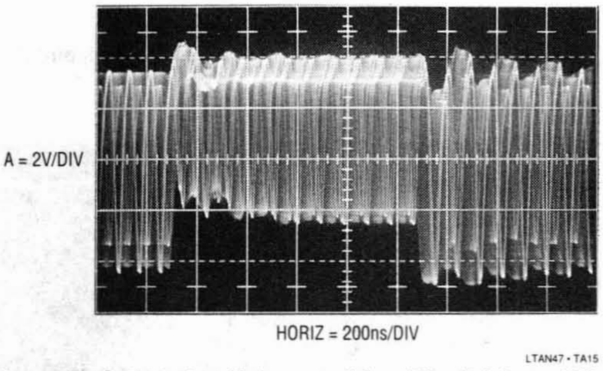

Figure 15. Output of an Unbypassed Amplifier Driving a 100Ω Load Without Bypass Capacitors – 58 ☎

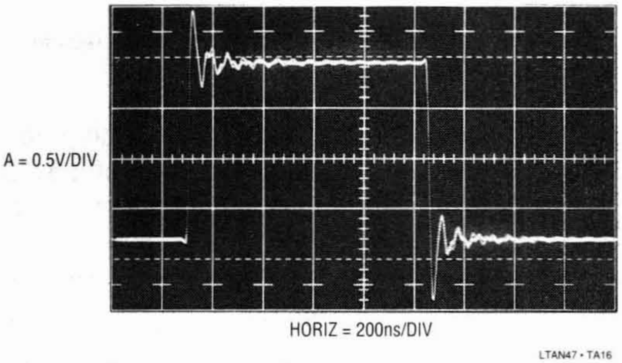

Figure 16. An Unbypassed Amplifier Driving No Load is Surprisingly Stable...at the Moment – 49 ☎

The multiple time constant ringing in Figure 18 often indicates poor grade paralleled bypassing capacitors or excessive trace length between the capacitors. While paralleling capacitors of different characteristics is a good way to get wideband bypassing, it should be carefully considered. Resonant interaction between the capacitors can cause a waveform like this after a step.

This type response is often aggravated by heavy amplifier loading. *When paralleling bypass capacitors, plan the layout and breadboard with the units you plan to use in production.*

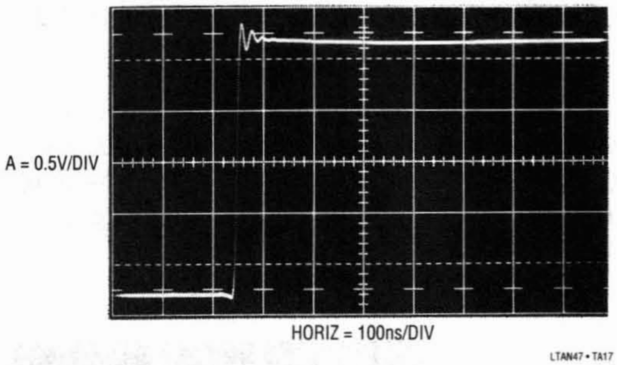

Figure 17. Poor Quality Bypass Capacitor Allows Some Ringing – 28 ☎

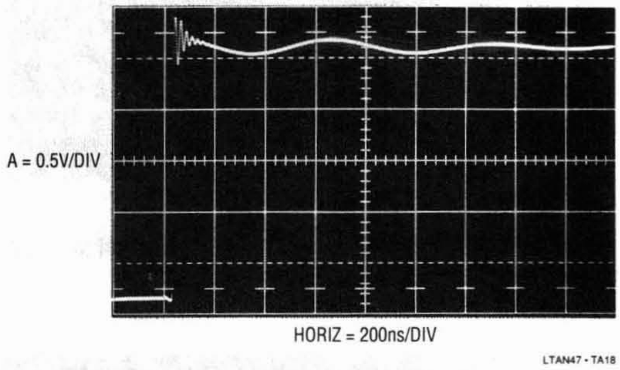

Figure 18. Paralleled Bypass Capacitors Form a Resonant Network and Ring – 2 ☎

Figure 19 addresses a more subtle bypassing problem. The trace shows the last 40mV excursion of a 5V step almost settling cleanly in 300ns. The slight overshoot is due to a loaded (500Ω) amplifier without quite enough bypassing. Increasing the total supply bypassing from 0.1µF to 1µF cured this problem. *Use large value paralleled bypass capacitors when very fast settling is required, particularly if the amplifier is heavily loaded or sees fast load steps.*

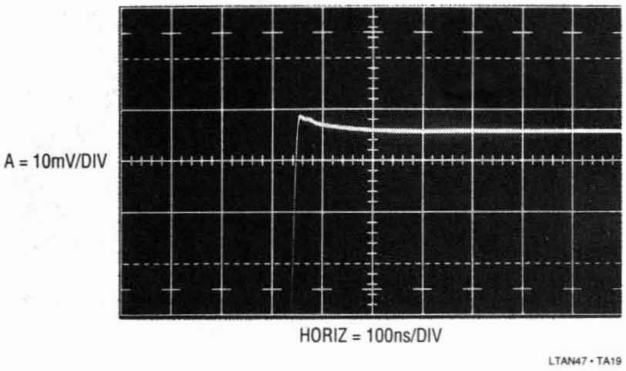

Figure 19. A More Subtle Bypassing Problem. Not-Quite-Good-Enough Bypassing Causes a Few Millivolts of Peaking – 1 ☎

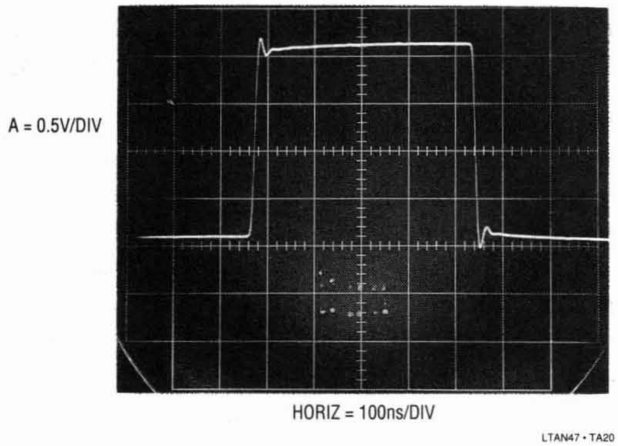

Figure 20. 2pF Stray Capacitance at the Summing Point Introduces Peaking – 4 ☎

The problem shown in Figure 20, peaking on the leading and trailing corners, is typical of poor layout practice (see Tutorial section on "Breadboarding Techniques"). This unity gain inverter suffers from excessive trace area at the summing point. Only 2pF of stray capacitance caused the peaking and ring shown. *Minimize trace area and stray capacitance at critical nodes. Consider layout as an integral part of the circuit and plan it accordingly.*

Figure 21's low level square wave output appears to suffer from some form of parasitic oscillation. In actuality, the disturbance is typical of that caused by fast digital clocking or switching regulator originated noise getting into critical circuit nodes. *Plan for parasitic radiative or conductive paths and eliminate them with appropriate layout and shielding.*

Figure 22 underscores the previous statement. This output was taken from a gain-of-ten inverter with 1kΩ input

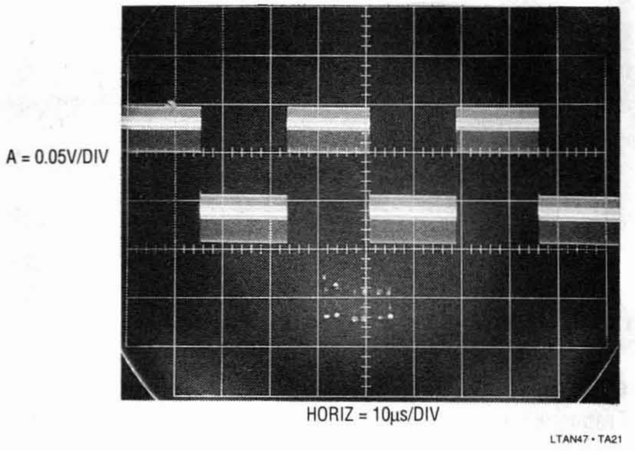

Figure 21. Clock or Switching Regulator Noise Corrupts Output Due to Poor Layout – 3 ☎

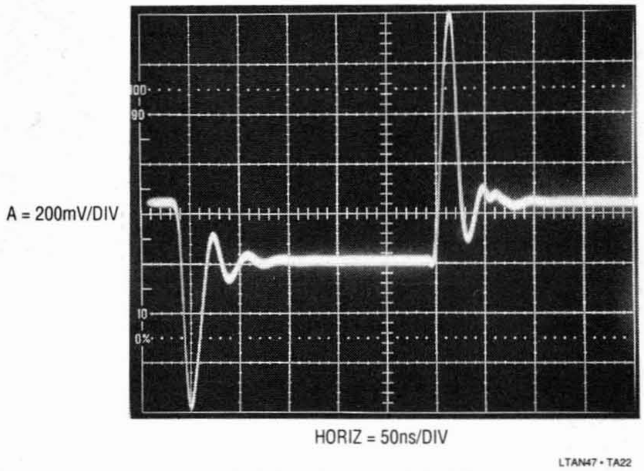

Figure 22. Output of an X10 Amplifier with 1pF Coupling from the Summing Point to the Input. Careful Shielding of the Input Resistor Will Eliminate the Peaked Edges and Ringing – 2 ☎

resistance. It shows severe peaking induced by *only 1pF* of parasitic capacitance across the 1k resistor. The 50Ω terminated input source provides only 20mV of drive via a divider, but that's more than enough to cause problems, even with only 1pF stray coupling. In this case the solution was a ground referred shield at a right angle to, and encircling, the 1kΩ resistor. *Plan for parasitic radiative paths and eliminate them with appropriate shielding.*

A decompensated amplifier running at too low a gain produced Figure 23's trace. The price for decompensated amplifiers' increased speed is restrictions on minimum allowable gain. Decompensated amplifiers are simply not stable below some (specified) minimum gain, and no amount of ignorance or wishing will change this. This is a common applications oversight with these devices, although the amplifier never fails to remind the user. *Observe gain restrictions when using decompensated amplifiers.*

Oscillation is also the problem in Figure 24, and it is due to excessive capacitive loading (see Tutorial section on "Oscillation"). Capacitive loading to ground introduces lag in the feedback signal's return to the input. If enough lag is introduced (e.g., a large capacitive load) the amplifier may oscillate. Even if a capacitively loaded amplifier doesn't oscillate, it's always a good idea to check its response with step testing. It's amazing how close to the edge of the cliff you can get without falling off, except when you build 10,000 production units. *Avoid capacitive loading. If such loading is necessary, check performance margins and isolate or buffer the load if necessary.*

Figure 25 appears to contain one cycle of oscillation. The output waveform initially responds, but abruptly reverses direction, overshoots and then heads positive again. Some

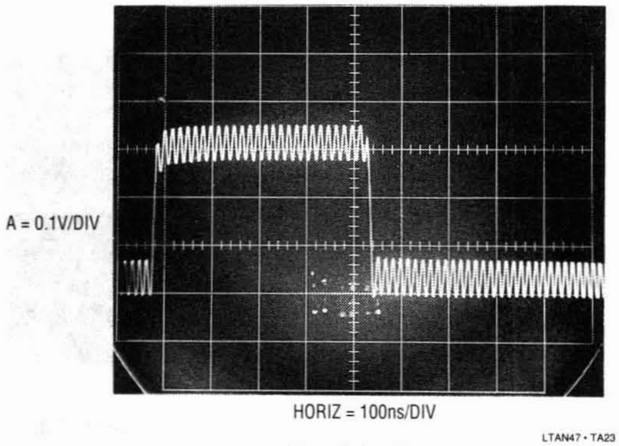

Figure 23. Decompensated Amplifier Running at Too Low a Gain – 22 ☎

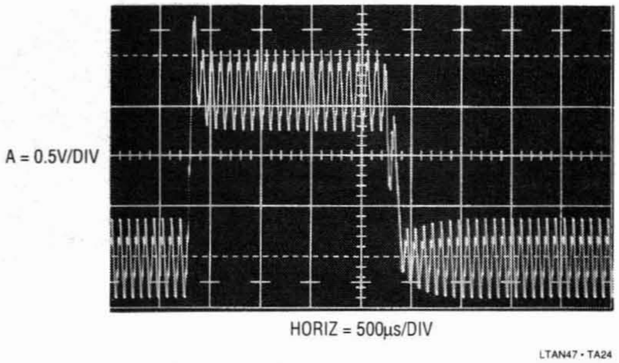

Figure 24. Excessive Capacitive Load Upsets the Amplifier – 165 ☎

overshoot again occurs, with a long tail and a small dip well before a non-linear slew returns the waveform to zero. Ugly overshoot and tailing completes the cycle. This is certainly strange behavior. What is going on here? The input pulse is responsible for all these anomalies. Its amplitude takes the amplifier outside its common-mode limits, inducing the bizarre effects shown. *Keep inputs inside specified common-mode limits at all times.*

Figure 26 shows an oscillation laden output (Trace B) trying to unity gain invert the input (Trace A). The input's form is distinguishable in the output, but corrupted with very high frequency oscillation and overshoot. In this case the amplifier includes a booster within its loop to provide increased output current. The disturbances noted are traceable to local instabilities within the booster circuit. (See Appendix C, "The Oscillation Problem — Frequency Compensation Without Tears"). *When using output booster stages, insure they are inherently stable before placing them inside an amplifier's feedback loop. Wideband booster stages are particularly prone to device level parasitic high frequency oscillation.*

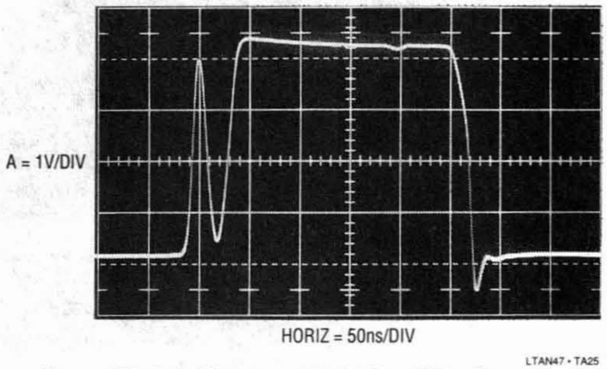

Figure 25. Input Common Mode Overdrive Generates Odd Outputs – 3 ☎

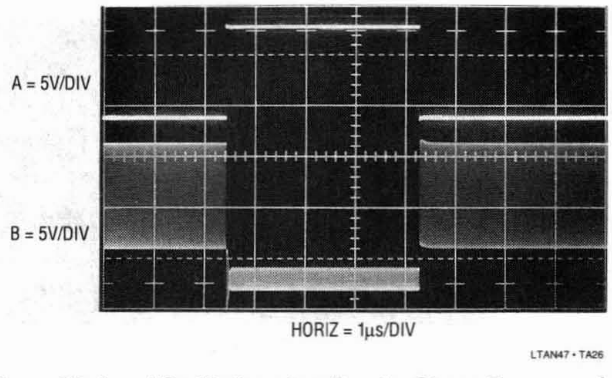

Figure 26. Local Oscillations in a Booster Stage. Frequency is Typically High – 12 ☎

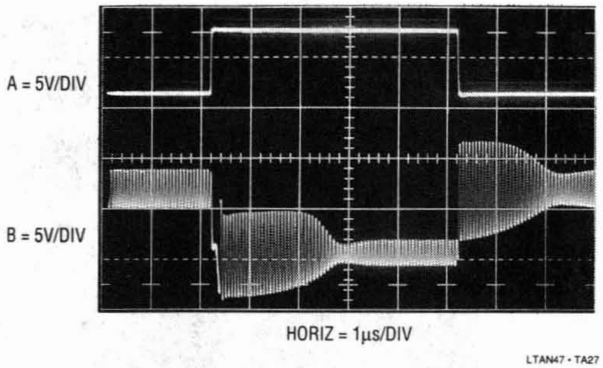

Figure 27. Loop Oscillations in a Booster Stage. Note Lower Frequency than Local Oscillations in Previous Example – 28 ☎

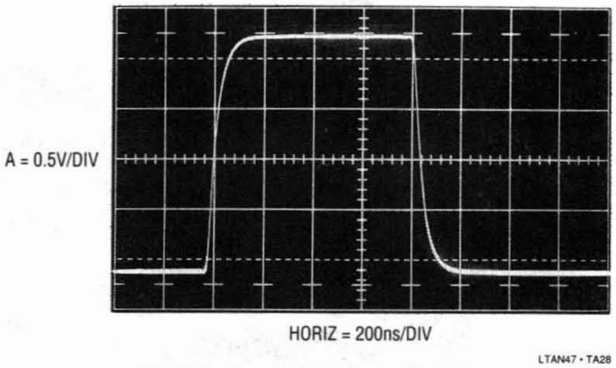

Figure 28. Excessive Source Impedance Gives Serene But Undesired Response – 6 ☎

Figure 27's booster augmented unity gain inverting op amp also oscillates, but at a much lower frequency. Additionally, overshoot and non-linear recovery dominate the waveform's envelope. Unlike the previous example, this behavior is not due to local oscillations within the booster stage. Instead, the booster is simply too slow to be included in the op amp's feedback loop. It introduces enough lag to force oscillation, even as it hopelessly tries to maintain loop closure. *Insure booster stages are fast enough to maintain stability when placed in the amplifier's feedback loop.*

The serene rise and fall of Figure 28's pulse is a welcome relief from the oscillatory screaming of the previous photos. Unfortunately, such tranquilized behavior is simply too slow. This waveform, reminiscent of Figure 8's bandlimited response, is due to excessive source impedance. The high source impedance combines with amplifier input capacitance to band limit the input and the output reflects this action. *Minimize source impedance to levels* *which maintain desired bandwidth. Keep stray capacitance at inputs down.*

TUTORIAL SECTION

An implied responsibility in raising the aforementioned issues is their solution or elimination. What good is all the rabble-rousing without suggestions for fixes? It is in this spirit that this tutorial section is presented. Theory, techniques, prejudice and just plain gossip are offered as tools which may help avoid or deal with difficulties. As previously mentioned, the tutorials appear in roughly the same order as the problems were presented.

About Cables, Connectors and Terminations

Routing of high speed signals to and from the circuit board should always be done with good quality coaxial cable. The cable should be driven and terminated in the system's characteristic impedance at the drive and load points. The driven end is usually an instrument (e.g., pulse or signal generator), presumably endowed with proper characteristics by its manufacturer. It is the cable and its termination, selected by the experimenter, that often cause problems.

All coaxial cable is not the same. Use cable appropriate to the system's characteristic impedance and of good quality. Poorly chosen cable materials or construction methods can introduce odd effects at very high speeds, resulting in observed waveform distortion. A poor cable choice can adversely effect 0.01% settling in the 100ns-200ns region. Similarly, poor cable can preclude maintenance of even the cleanest pulse generator's 1ns rise time or purity. Typically, inappropriate cable can introduce tailing, rise time degradation, aberrations following transitions, nonlinear impedance and other undesirable characteristics.

Termination choice is equally important. Good quality BNC coaxial type terminators are usually the best choice for breadboarding. Their impedance vs frequency is flat into the GHz range. Additionally, their construction insures that the (often substantial) drive current returns directly to the source, instead of being dumped into the breadboard's ground system. As previously discussed, BNC coaxial terminators are not simply resistors in a can. Special construction techniques insure optimum wideband response. Figures 29 and 30 demonstrate this nicely. In Figure 29 a 1ns pulse with 350ps rise and fall times[1] is monitored on a 1GHz sampling 'scope (Tektronix 556 with 1S1 sampling plug-in and P6032 probe). The waveform is clean, with only a slight hint of ring after the falling edge. This photo was taken with a high grade BNC coaxial type terminator in use. Figure 30 does not share these attributes. Here, the generator is terminated with a 50Ω carbon composition resistor with lead lengths of about 1/8 inch. The waveform rings and tails badly on turn-off before finally settling. Note that the sweep speed required a 2.5X reduction to capture these unwanted events.

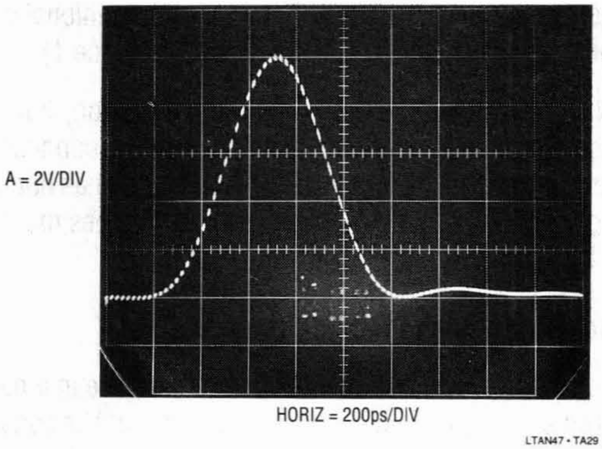

Figure 29. 350ps Rise and Fall Times are Preserved by a Good Quality Termination

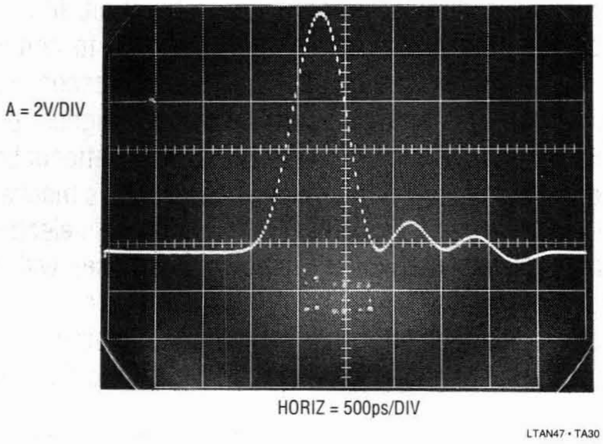

Figure 30. Poor Grade Termination Produces Pronounced Ringing and Tailing in the GHz Range

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[1] **Note 1:** The ability to generate such a pulse proves useful for a variety of tasks, including testing terminators, cables, probes and oscilloscopes for response. The requirements for this pulse generator are surprisingly convenient and inexpensive. For a discussion and construction details see Appendix D "Measuring Probe - Oscilloscope Response".

Connectors, such as BNC barrel extensions and tee-type adaptors, are convenient and frequently employed. Remember that these devices represent a discontinuity in the cable, and can introduce small but undesirable effects. In general it is best to employ them as close as possible to a terminated point in the system. Use in the middle of a cable run provides minimal absorption of their mismatch and reflections. The worst offenders among connectors are adapters. This is unfortunate, as these devices are necessitated by the lack of connection standardization in wideband instrumentation. The mismatch caused by a BNC-to-GR874 adaptor transition at the input of a wideband sampling 'scope is small, but clearly discernible in the display. Similarly, mismatches in almost all adaptors, and even in "identical" adaptors of different manufacture, are readily measured on a high-frequency network analyzer such as the Hewlett-Packard 4195A[2] (for additional wisdom and terror along these lines see Reference 1).

BNC connections are easily the most common, but not necessarily the most desirable, wideband connection mechanism. The ingenious GR874 connector has notably superior high frequency characteristics, as does the type N. Unfortunately, it's a BNC world out there.

About Probes and Probing Techniques

The choice of which oscilloscope probe to use in a measurement is absolutely crucial. The probe must be considered as an inherent part of the circuit under test. Rise time, bandwidth, resistive and capacitive loading, delay and other limitations must be kept in mind.

Sometimes, the best probe is no probe at all. In some circumstances it is possible and preferable to connect critical breadboard points *directly* to the oscilloscope (see Figure 31). This arrangement provides the highest possible grounding integrity, eliminates probe attenuation, and maintains bandwidth. In most cases this is mechanically inconvenient, and often the oscilloscope's electrical characteristics (particularly input capacitance) will not permit it. This is why oscilloscope probes were developed, and why so much effort has been put into their development (Reference 42 is excellent). In addition to the material presented here, an in-depth treatment of probes appears in Appendix A, "ABC's of Probes", guest written by the engineering staff of Tektronix, Inc.

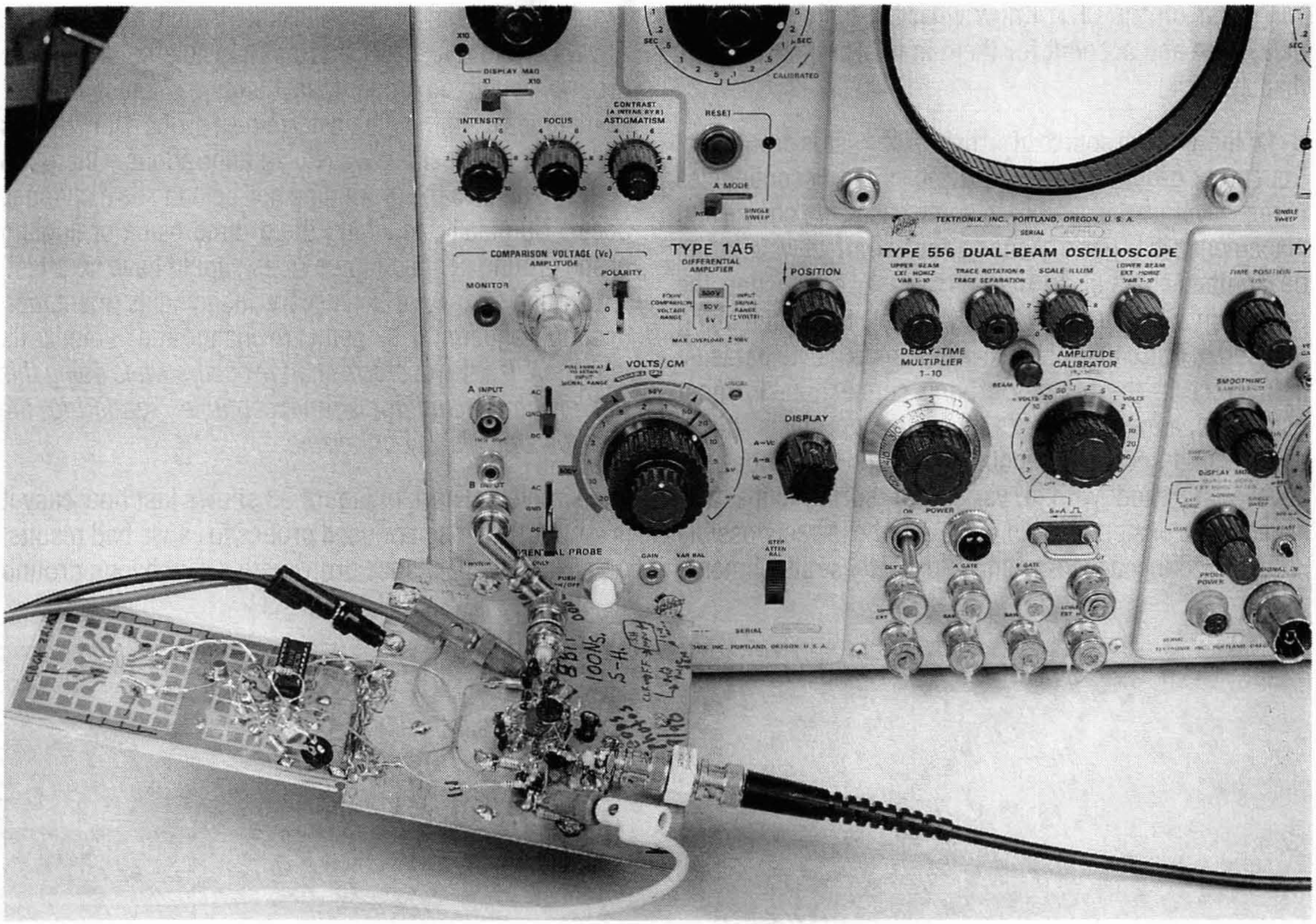
Probes are the most overlooked cause of oscilloscope mismeasurement. All probes have some effect on the point they are measuring. The most obvious is input resistance, but input capacitance usually dominates in a high speed measurement. Much time can be lost chasing circuit events which are actually due to improperly selected or applied probes. An 8pF probe looking at a 1kΩ source impedance forms an 8ns lag — substantially longer than a fast amplifier's delay time! Pay particular attention to the probe's input capacitance. Standard 10MΩ, 10X probes typically have 8pF-10pF of input capacitance, with 1X types being much higher. In general, 1X probes are not suitable for fast work because their bandwidth is limited to about 20MHz. Remember that all 10X probes cannot be used with all oscilloscopes; the probe's compensation range must match the oscilloscope's input capacitance. Low impedance probes (with 500Ω to 1kΩ resistance) designed for 50Ω inputs, usually have input capacitance of 1pF or 2pF. They are a very good choice if you can stand the low resistance. FET probes maintain high input resistance and keep capacitance at the 1pF level but have substantially more delay than passive probes. FET probes also have limitations on input common-mode range which must be adhered to or serious measurement errors will result. Contrary to popular belief, FET probes *do not* have extremely high input resistance — some types are as low as 100kΩ. It is possible to construct a wideband FET probe with very high input impedance, although input capacitance is somewhat higher than standard FET probes. For measurements requiring these characteristics, such a probe is useful. See Appendix E, "An Ultra Fast High Impedance Probe".

Regardless of which type probe is selected remember that they all have bandwidth and rise time restrictions. The displayed rise time on the oscilloscope is the vector sum of source, probe and 'scope rise times.

$$t_{RISE} = \sqrt{(t_{RISE}\ \text{Source})^2 + (t_{RISE}\ \text{Probe})^2 + (t_{RISE}\ \text{Oscilloscope})^2}$$

This equation warns that some rise time degradation must occur in a cascaded system. In particular, if probe and oscilloscope are rated at the same rise time, the system response will be slower than either.

Note 2: Almost no one believes any of this until they see it for themselves. I didn't. Photos of the network analyzer's display aren't included in the text because no one would believe them. I wouldn't.



LTAN47 • TA31

Figure 31. Sometimes the Best Probe is No Probe. Direct Connection to the Oscilloscope Eliminates a 10X Probe's Attenuation and Possible Grounding Problems in a Sample-Hold (Figure 124) Settling Time Measurement

Current probes are useful and convenient.[3] The passive transformer-based types are fast and have less delay than the Hall effect-based versions. The Hall types, however, respond at DC and low frequency and the transformer types typically roll off around 100Hz to 1kHz. Both types have saturation limitations which, when exceeded, cause odd results on the CRT which will confuse the unwary. The Tektronix type CT-1 current probe, although not nearly as versatile as the clip-on probes, bears mention. Although this is not a clip-on device, it may be the least electrically intrusive way of extracting wideband signal information. Rated at 1GHz bandwidth, it produces 5mV/mA output with only 0.6pF loading. Decay time constant of this AC current probe is ≈1%/50ns, resulting in a low frequency limit of 35kHz.

A very special probe is the differential probe. A differential probe may be thought of as two matched FET probes contained within a common probe housing. This probe literally brings the advantage of a differential input oscilloscope to the circuit board. The probes matched, active circuitry provides greatly improved high frequency common mode rejection over single ended probing or even matched passive probes used with a differential amplifier. The resultant ability to reject common-mode signals and ground noise at high frequency allows this probe to deliver exceptionally clean results when monitoring small, fast signals. Figure 32 shows a differential probe being used to verify the waveshape of a 2.5mV input to a wideband, high gain amplifier (Figure 76 of the Applications section).

When using different probes, remember that they all have different delay times, meaning that apparent timing errors will occur on the CRT. Know what the individual probe delays are and account for them in interpreting the CRT display.

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[3] **Note 3:** A more thorough discussion of current probes is given in LTC Application Note 35, "Step Down Switching Regulators". See Reference 2.

By far the greatest source of error in probe use is grounding. Poor probe grounding can cause ripples and discontinuities in the waveform observed. In some cases the choice and placement of a probe's ground strap will affect waveforms on another channel. In the worst case, connecting the probe's ground wire will virtually disable the circuit being measured. The cause of these problems is due to parasitic inductance in the probe's ground connection. In most oscilloscope measurements this is not a problem, but at nanosecond speeds it becomes critical. Fast probes are always supplied with a variety of spring clips and accessories designed to aid in making the lowest possible inductive connection to ground. Most of these attachments assume a ground plane is in use, which it should be. Always try to make the shortest possible connection to ground – anything longer than 1 inch may cause trouble. Sometimes it's difficult to determine if probe grounding is the cause of observed waveform aberrations. One good test is to disturb the grounding set-up and see if changes occur. Nominally, touching the ground plane or jiggling probe ground connectors or wires should have no effect. If a ground strap wire is in use try changing its orientation or simply squeezing it together to change and minimize its loop area. *If any waveform change occurs while doing this the probe grounding is unacceptable, rendering the oscilloscope display unreliable.*

The simple network of Figure 33 shows just how easy it is for poorly chosen or used probes to cause bad results. A 9pF input capacitance probe with a 4 inch long ground

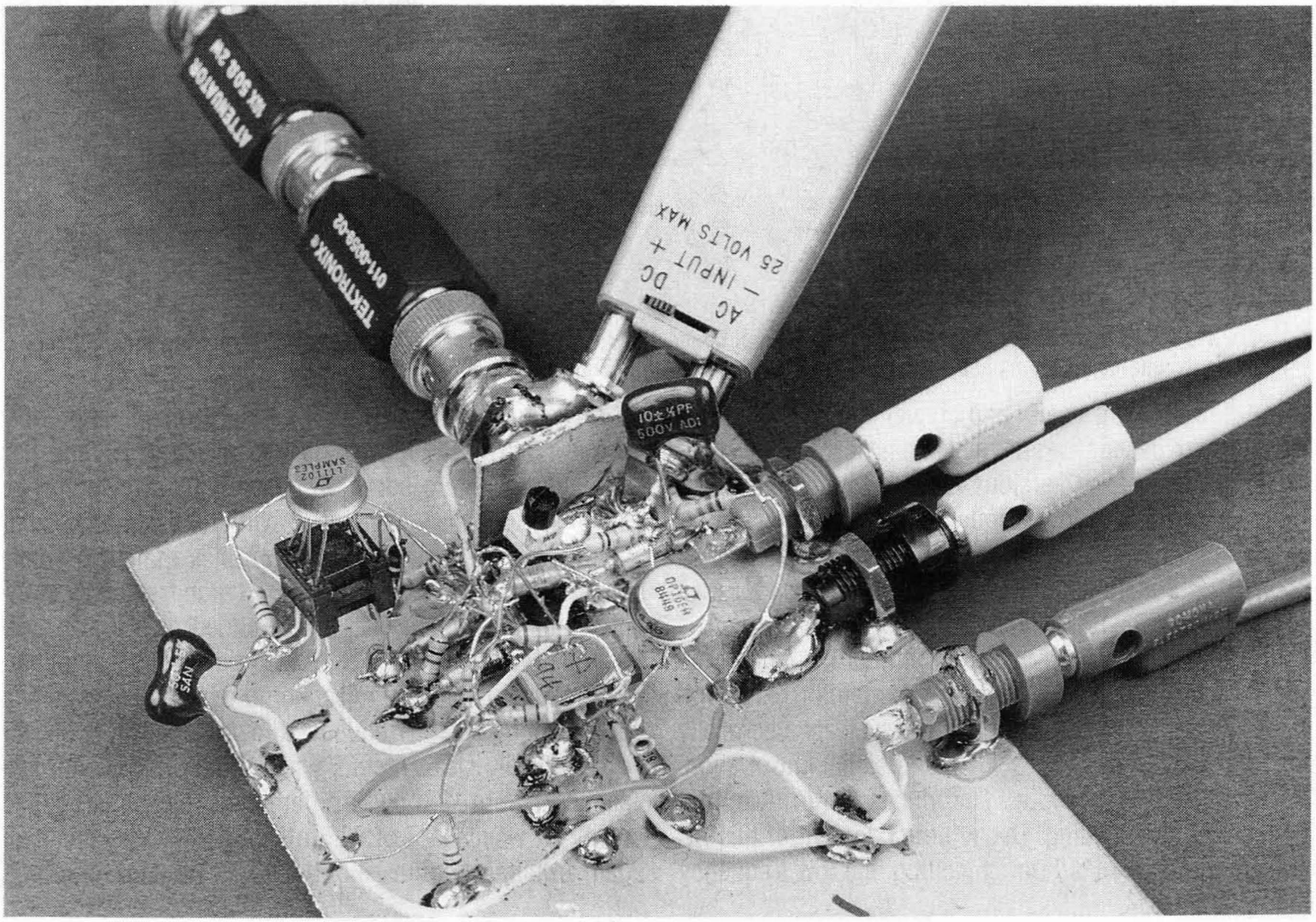

Figure 32. Using a Differential Probe to Verify the Integrity of a 2.5mV High Speed Input Pulse (Figure 76's X1000 Amplifier)

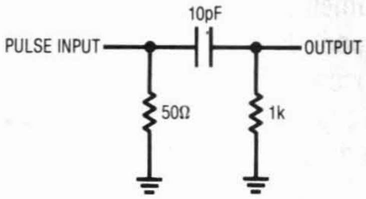

Figure 33. Probe Test Circuit

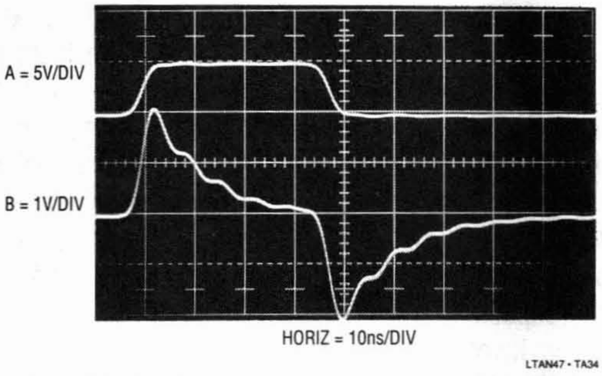

Figure 34. Test Circuit Output with 9pF Probe and 4 Inch Ground Strap

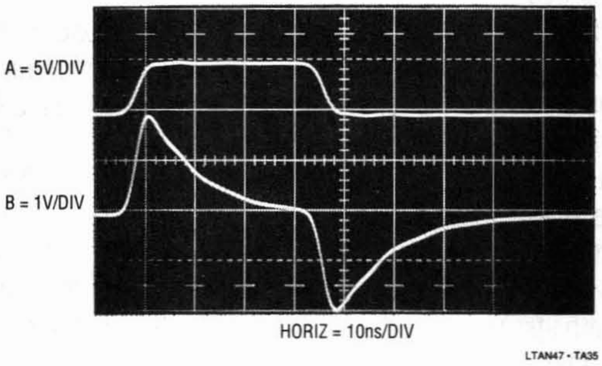

Figure 35. Test Circuit Output with 9pF Probe and 0.25 Inch Ground Strap

strap monitors the output (Trace B, Figure 34). Although the input (Trace A) is clean, the output contains ringing. Using the same probe with a 1/4 inch spring tip ground connection accessory seemingly cleans up everything (Figure 35). However, substituting a 1pf FET probe (Figure 36) reveals a 50% output amplitude error in Figure 35! The FET probe's low input capacitance allows a more accurate version of circuit action. The FET probe does, however, contribute its own form of error. Note that the probe's response is tardy by 5ns due to delay in its active circuitry. Hence, separate measurements with each probe are required to determine the output's amplitude and timing parameters.

A final form of probe is the human finger. Probing the circuit with a finger can accentuate desired or undesired effects, giving clues that may be useful. The finger can be used to introduce stray capacitance to a suspected circuit node while observing results on the CRT. Two fingers, lightly moistened, can be used to provide an experimental resistance path. Some high speed engineers are particularly adept at these techniques and can estimate the capacitive and resistive effects created with surprising accuracy.

Examples of some of the probes discussed, along with different forms of grounding implements, are shown in Figure 37. Probes A, B, E, and F are standard types equipped with various forms of low impedance grounding attachments. The conventional ground lead used on G is more convenient to work with but will cause ringing and

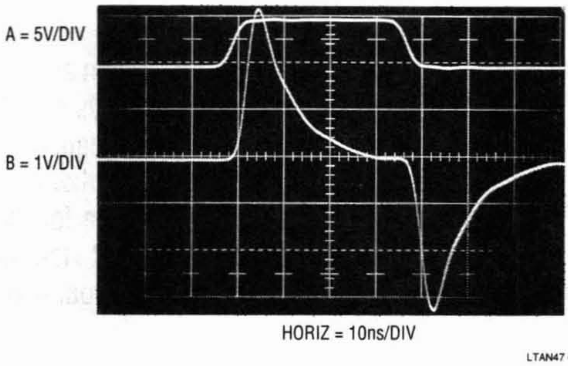

Figure 36. Test Circuit Output with FET Probe

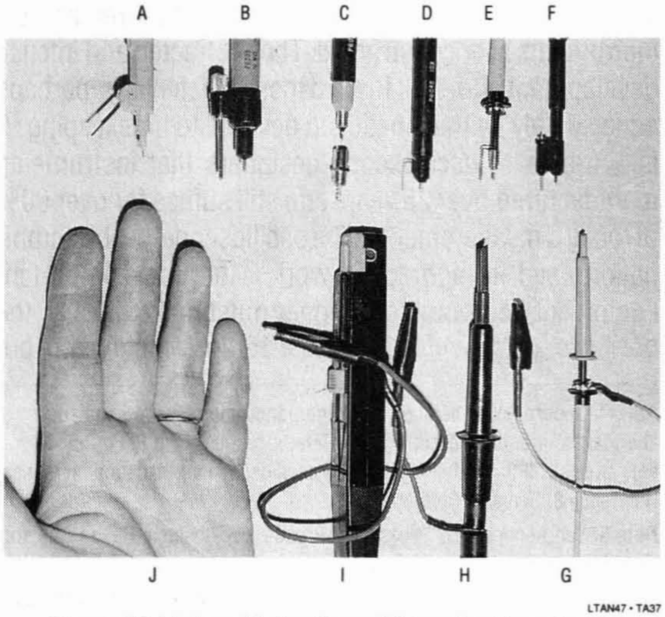

Figure 37. Various Probe-Ground Strap Configurations

other effects at high frequencies, rendering it useless. H has a very short ground lead. This is better, but can still cause trouble at high speeds. D is a FET probe. The active circuitry in the probe and a very short ground connector ensure low parasitic capacitance and inductance. C is a separated FET probe attenuator head. Such heads allow the probe to be used at higher voltage levels (e.g., ±10V or ±100V). The miniature coaxial connector shown can be mounted on the circuit board and the probe mated with it. This technique provides the lowest possible parasitic inductance in the ground path and is especially recommended. I is a current probe. A ground connection is not usually required. However, at high speeds the ground connection may result in a cleaner CRT presentation. Because no current flows in the ground lead of these probes, a long strap is usually permissible. J is typical of the finger probes described in the text. Note the ground strap on the third finger.

The low inductance ground connectors shown are available from probe manufacturers and are always supplied with good quality, high frequency probes. Because most oscilloscope measurements do not require them, they invariably become lost. There is no substitute for these devices when they are needed, so it is prudent to take care of them. This is especially applicable to the ground strap on the finger probe.

About Oscilloscopes

The modern oscilloscope is one of the most remarkable instruments ever constructed. The protracted and intense development effort put toward these machines is perhaps equaled only by the fanaticism devoted to timekeeping.[4] It is a tribute to oscilloscope designers that instruments manufactured over 25 years ago still suffice for over 90% of today's measurements. The oscilloscope-probe combination used in high speed work is the most important equipment decision the designer must make. Ideally, the oscilloscope should have at least 150MHz bandwidth, but slower instruments are acceptable if their limitations are well understood. Be certain of the characteristics of the probe-oscilloscope combination. Rise time, bandwidth, resistive and capacitive loading, delay, noise, channel-to-channel feedthrough, overdrive recovery, sweep nonlinearity, triggering, accuracy and other limitations must be kept in mind. High speed linear circuitry demands a great deal from test equipment and countless hours can be saved if the characteristics of the instruments used are well known. Obscene amounts of time have been lost pursuing "circuit problems" which in reality are caused by misunderstood, misapplied or out-of-spec equipment. Intimate familiarity with your oscilloscope is invaluable in getting the best possible results with it. In fact, it is possible to use seemingly inadequate equipment to get good results if the equipment's limitations are well known and respected. All of the circuits in the Applications section involve rise times and delays well above the 100MHz-200MHz region, but 90% of the development work was done with a 50MHz oscilloscope. Familiarity with equipment and thoughtful measurement technique permit useful measurements seemingly beyond instrument specifications. A 50MHz oscilloscope cannot track a 5ns rise time pulse, but it can measure a 2ns delay between two such events. Using such techniques, it is often possible to deduce the desired information. There are situations where no amount of cleverness will work and the right equipment (e.g., a faster oscilloscope) must be used. Sometimes, "sanity-checking" a limited bandwidth instrument with a higher bandwidth oscilloscope is all that is required. For high speed work, brute force bandwidth is indispensable when needed, and no amount of features or computational sophistication will substitute. Most high speed circuitry does not require more than two traces to get where you are going. Versatility and many channels are desirable, but if the budget is limited, spend for bandwidth!

Dramatic differences in displayed results are produced by probe-oscilloscope combinations of varying bandwidths. Figure 38 shows the output of a very fast pulse[5] monitored with a 1GHz sampling 'scope (Tektronix 556 with 1S1 sampling plug-in). At this bandwidth the 10V amplitude appears clean, with just a small hint of ringing after the falling edge. The rise and fall times of 350ps are suspicious, as the sampling oscilloscope's rise time is also specified at 350ps.[6]

Note 4: In particular, the marine chronometer received ferocious and abundant amounts of attention. See References 4, 5, and 6. For an enjoyable stroll through the history of oscilloscope vertical amplifiers, see Reference 3. See also Reference 41.

Note 5: See Appendix D, "Measuring Probe - Oscilloscope Response", for complete details on this pulse generator.

Note 6: This sequence of photos was shot in my home lab. I'm sorry, but 1GHz is the fastest 'scope in my house.

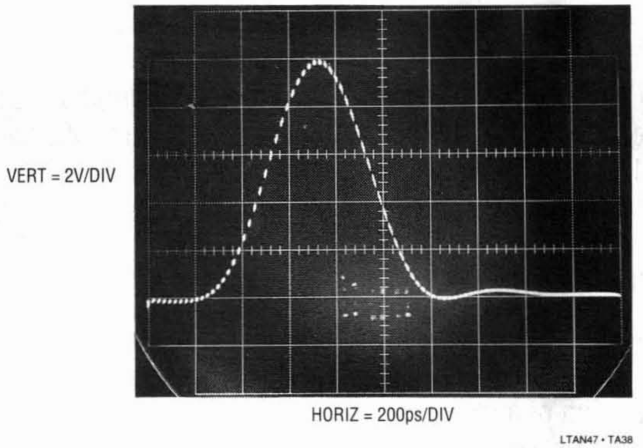

Figure 38. A 350ps Rise/Fall Time 10V Pulse Monitored on 1GHz Sampling Oscilloscope. Direct 50Ω Input Connection is Used

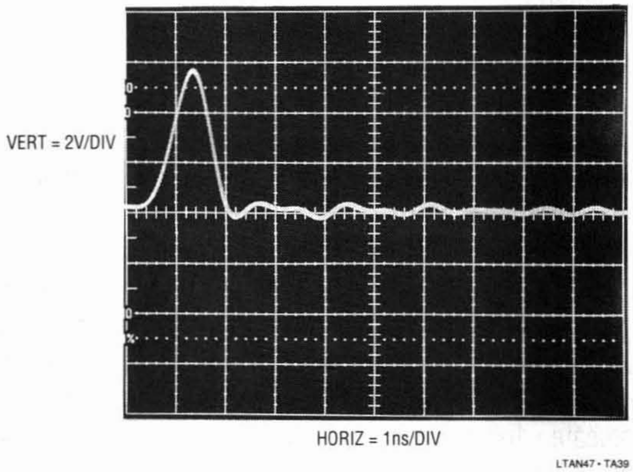

Figure 39. The Test Pulse Appears Smaller and Slower On a 350MHz Instrument (t_{RISE} = 1ns). Deliberate Poor Grounding Creates Rippling After the Pulse Falls. Direct 50Ω Connection is Used

Figure 39 shows the same pulse observed on a 350MHz instrument with a direct connection to the input (Tektronix 485/50Ω input). Indicated rise time balloons to 1ns, while displayed amplitude shrinks to 6V, reflecting this instrument's lesser bandwidth. To underscore earlier discussion, poor grounding technique (1 1/2" of ground lead to the ground plane) created the prolonged rippling after the pulse fall.

Figure 40 shows the same 350MHz (50Ω input) oscilloscope with a 3GHz 10X probe (Tektronix P6056). Displayed results are nearly identical, as the probe's high bandwidth contributes no degradation. Again, deliberate poor grounding causes overshoot and rippling on the pulse fall.

Figure 41 equips the same oscilloscope with a 10X probe specified at 290MHz bandwidth (Tektronix P6047). Additionally, the oscilloscope has been switched to its 1MΩ input mode, reducing bandwidth to a specified 250MHz. Amplitude degrades to less than 4V and edge times similarly increase. The deliberate poor grounding contributes the undershoot and underdamped recovery on pulse fall.

In Figure 42 a 100MHz 10X probe (Hewlett-Packard Model 10040A) has been substituted for the 290MHz unit. The oscilloscope and its set-up remain the same. Amplitude shrinks below 2V, with commensurate rise and fall times. Cleaned up grounding eliminates aberrations.

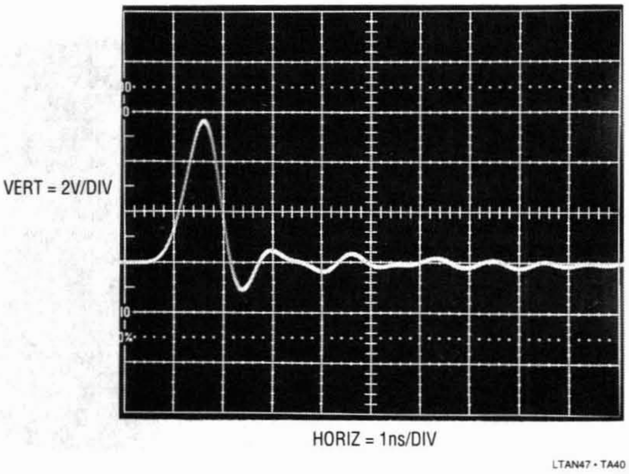

Figure 40. Test Pulse on the Same 350MHz Oscilloscope Using a 3GHz 10X Probe. Deliberate Poor Grounding Maintains Rippling Residue

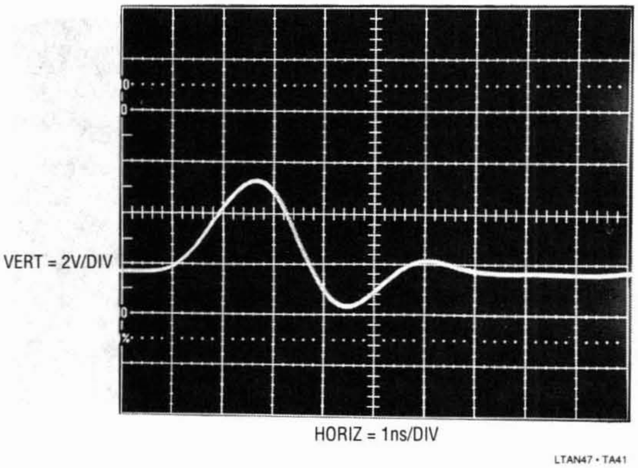

Figure 41. Test Pulse Measures Only 3V High on a 250MHz 'Scope with Significant Waveform Distortion. 250MHz 10X Probe Used

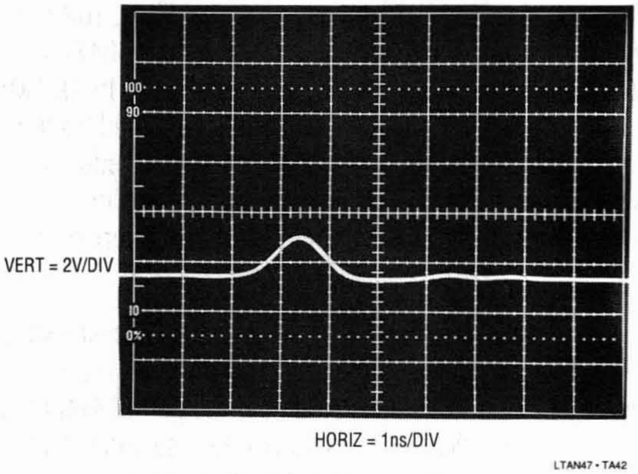

Figure 42. Test Pulse Measures Under 2V High Using 250MHz 'Scope and a 100MHz Probe

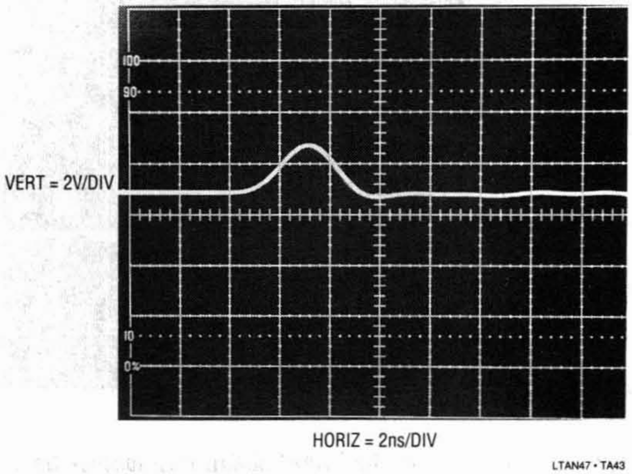

Figure 43. 150MHz Oscilloscope (t_{RISE} = 2.4ns) with Direct Connection Responds to the Test Pulse

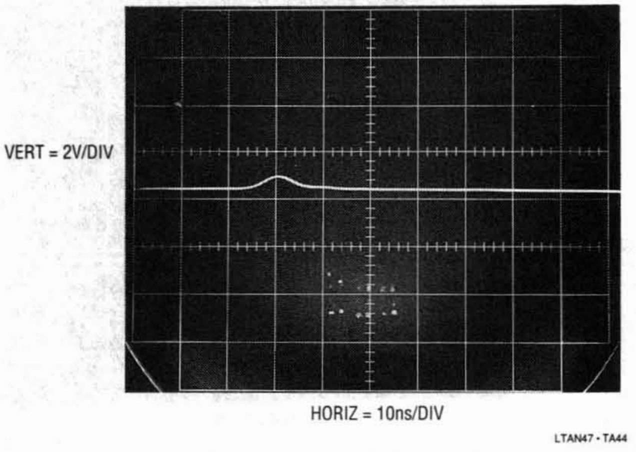

Figure 44. A 50MHz Instrument Barely Grunts. 10V, 350ps Test Pulse Measures Only 0.5V High with 7ns Rise and Fall Times!

A Tektronix 454A (150MHz) produced Figure 43's trace. The pulse generator was directly connected to the input. Displayed amplitude is about 2V, with appropriate 2ns edges. Finally, a 50MHz instrument (Tektronix 556 with 1A4 plug-in) just barely grunts in response to the pulse (Figure 44). Indicated amplitude is 0.5V, with edges reading about 7ns. That's a long way from the 10V and 350ps that's really there!

A final oscilloscope characteristic is overload performance. It is often desirable to view a small amplitude portion of a large waveform. In many cases the oscilloscope is required to supply an accurate waveform after the display has been driven off screen. How long must one wait after an overload before the display can be taken seriously? The answer to this question is quite complex. Factors involved include the degree of overload, its duty cycle, its magnitude in time and amplitude, and other considerations. Oscilloscope response to overload varies widely between types and markedly different behavior can be observed in any individual instrument. For example, the recovery time for a 100X overload at 0.005V/division may be very different than at 0.1V/division. The recovery characteristic may also vary with waveform shape, DC content and repetition rate. With so many variables, it is clear that measurements involving oscilloscope overload must be approached with caution. Nevertheless, a simple test can indicate when the oscilloscope is being deleteriously affected by overdrive.

The waveform to be expanded is placed on the screen at a vertical sensitivity which eliminates all off-screen activity. Figure 45 shows the display. The lower right hand portion is to be expanded. Increasing the vertical sensitivity by a factor of two (Figure 46) drives the waveform off-screen, but the remaining display appears reasonable. Amplitude has doubled and waveshape is consistent with the original display. Looking carefully, it is possible to see small amplitude information presented as a dip in the waveform at about the third vertical division. Some small disturbances are also visible. This observed expansion of the original waveform is believable. In Figure 47, gain has been further increased and all the features of Figure 46 are amplified accordingly. The basic waveshape appears clearer and the dip and small disturbances are also easier to see. No new waveform characteristics are observed. Figure 48 brings some unpleasant surprises. This increase in gain causes definite distortion. The initial negative-going peak, although larger, has a different shape. Its bottom appears less broad than in Figure 47. Additionally, the peak's positive recovery is shaped slightly differently. A new rippling disturbance is visible in the center of the screen. This kind of change indicates that the oscilloscope is having trouble. A further test can confirm that this waveform is being influenced by overloading. In Figure 49 the gain remains the same, but the vertical position knob has been used to reposition the display at the screen's bottom. This shifts the oscilloscope's DC operating point which, under normal circumstances, should not affect the displayed waveform. Instead, a marked shift in waveform amplitude and outline occurs. Repositioning the waveform to the screen's top produces a differently distorted waveform (Figure 50). It is obvious that for this particular waveform, accurate results cannot be obtained at this gain.

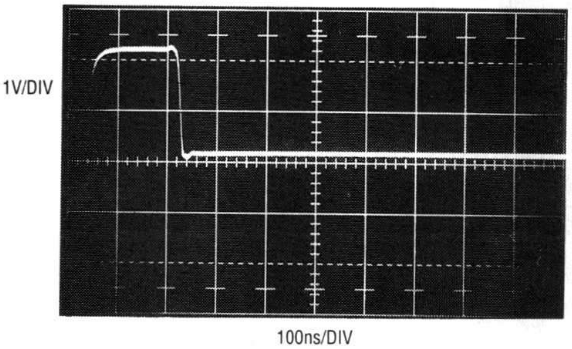

Figure 45

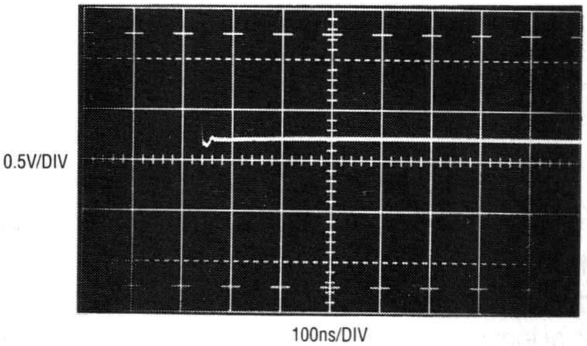

Figure 46

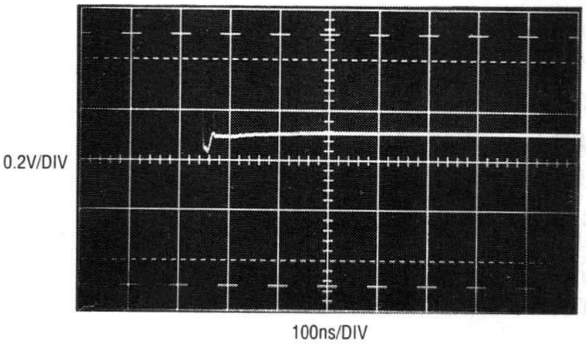

Figure 47

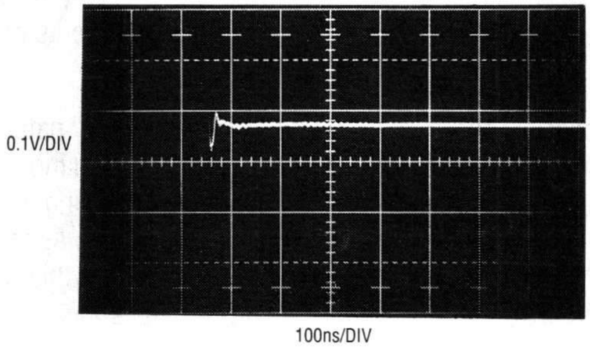

Figure 48

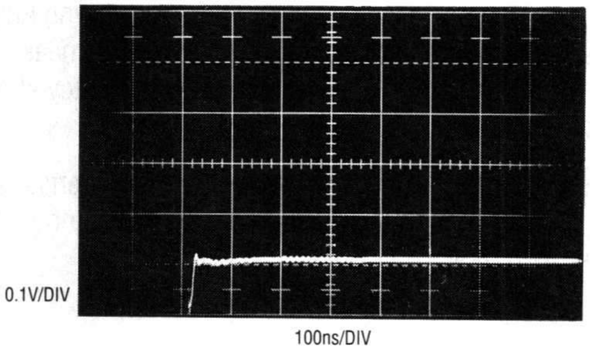

Figure 49

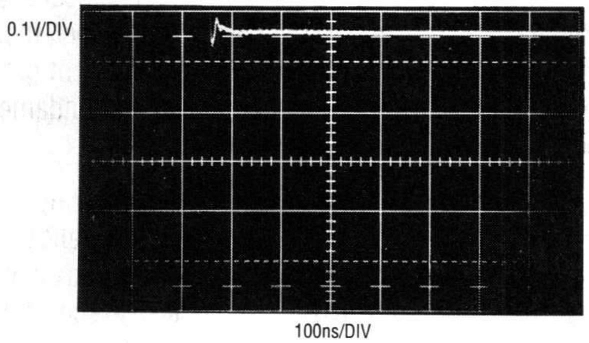

Figure 50

Figures 45-50. The Overdrive Limit is Determined by Progressively Increasing Oscilloscope Gain and Watching for Waveform Aberrations

Differential plug-ins can address some of the issues associated with excessive overdrive, although they cannot solve all problems. Two differential plug-in types merit special mention. At low level, a high sensitivity differential plug-in is indispensable. The Tektronix 1A7, 1A7A and 7A22 feature 10µV sensitivity, although bandwidth is limited to 1MHz. The units also have selectable high and low pass filters and good high frequency common-mode rejection. Tektronix type 1A5, W and 7A13 are differential comparators. They have calibrated DC nulling (slideback) sources, allowing observation of small, slowly moving events on top of common-mode DC or fast events riding on a waveform.

A special case is the sampling oscilloscope. By nature of its operation, a sampling 'scope in proper working order is inherently immune to input overload, providing essentially instantaneous recovery between samples. Appendix B, "Measuring Amplifier Settling Time", utilizes this capability. See Reference 8 for additional details.

The best approach to measuring small portions of large waveforms, however, is to eliminate the large signal swing seen by the oscilloscope. Appendix B, "Measuring Amplifier Settling Time" shows ways to do this when measuring DAC-amplifier settling time to very high accuracy at high speed.

In summary, while the oscilloscope provides remarkable capability, its limitations must be well understood when interpreting results.[7]

About Ground Planes

Many times in high frequency circuit layout, the term "ground plane" is used, most often as a mystical and ill-defined cure to spurious circuit operation. In fact, there is little mystery to the usefulness and operation of ground planes, and like many phenomena, their fundamental operating principle is surprisingly simple.

Ground planes are primarily useful for minimizing circuit inductance. They do this by utilizing basic magnetic theory. Current flowing in a wire produces an associated magnetic field. The field's strength is proportional to the current and inversely related to the distance from the conductor. Thus, we can visualize a wire carrying current (Figure 51) surrounded by radii of magnetic field. The unbounded field becomes smaller with distance. A wire's inductance is defined as the energy stored in the field set up by the wire's current. To compute the wire's inductance requires integrating the field over the wire's length and the total radial area of the field. This implies integrating on the radius from $R = R_W$ to infinity, a very large number. However, consider the case where we have two wires in space carrying the same current in either direction (Figure 52). The fields produced cancel.

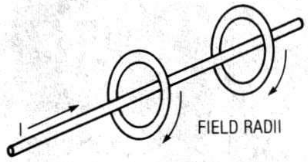

Figure 51. Single Wire Case

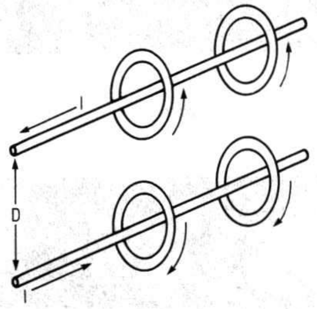

Figure 52. Two Wire Case

In this case, the inductance is much smaller than in the simple wire case and can be made arbitrarily smaller by reducing the distance between the two wires. This reduction of inductance between current carrying conductors is the underlying reason for ground planes. In a normal circuit, the current path from the signal source through its conductor and back to ground includes a large loop area. This produces a large inductance for this conductor which can cause ringing due to LRC effects. It is worth noting that 10nH at 100MHz has an impedance of 6Ω. At 10mA a 60mV drop results.

A ground plane provides a return path directly under the signal carrying conductor through which return current can flow. The conductor's small physical separation means the inductance is low. Return current has a direct path to ground, regardless of the number of branches associated with the conductor. Currents will always flow through the return path of lowest impedance. In a properly designed

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Note 7: Additional discourse on oscilloscopes will be found in References 1 and 7 through 11.

ground plane, this path is directly under the signal conductor. In a practical circuit, it is desirable to ground plane one whole side of the PC card (usually the component side for wave solder considerations) and run the signal conductors on the other side. This will give a low inductance path for all the return currents.

Aside from minimizing parasitic inductance, ground planes have additional benefits. Their flat surface minimizes resistive losses due to AC skin effect (AC currents travel along a conductor's surface). Additionally, they aid the circuit's high frequency stability by referring stray capacitances to ground.

Some practical hints for ground planes are:

1. Ground plane as much area as possible on the component side of the board, especially under traces that operate at high frequency.
2. Mount components that conduct substantial fast rise currents (termination resistors, ICs, transistors, decoupling capacitors) as close to the board as possible.
3. Where common ground potential is important (i.e., at comparator inputs), try to single point the critical components into the ground plane to avoid voltage drops.

   For example, in Figure 53's common A/D circuit, good practice would dictate that grounds 2, 3, 4 and 6 be as close to single point as possible. Fast, large currents must flow through R1, R2, D1 and D2 during the DAC settle time. Therefore, D1, D2, R1 and R2 should be mounted close to the ground plane to minimize their inductance. R3 and C1 don't carry any current, so their inductance is less important; they could be vertically inserted to save space and to allow point 4 to be single point common with 2, 3 and 6. In critical circuits, the designer must often trade off the beneficial effects of lowered inductance versus the loss of single point ground.
4. Keep trace length short. Inductance varies directly with length and no ground plane will achieve perfect cancellation.

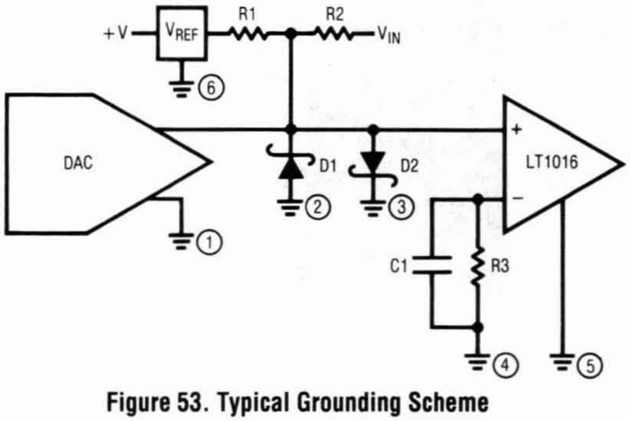

Figure 53. Typical Grounding Scheme

About Bypass Capacitors

Bypass capacitors are used to maintain low power supply impedance at the point of load. Parasitic resistance and inductance in supply lines mean that the power supply impedance can be quite high. As frequency goes up, the inductive parasitic becomes particularly troublesome. Even if these parasitic terms did not exist, or if local regulation is used, bypassing is still necessary because no power supply or regulator has zero output impedance at 100MHz. What type of bypass capacitor to use is determined by the application, frequency domain of the circuit, cost, board space and many other considerations. Some useful generalizations can be made.

All capacitors contain parasitic terms, some of which appear in Figure 54. In bypass applications, leakage and dielectric absorption are second order terms but series R and L are not. These latter terms limit the capacitor's ability to damp transients and maintain low supply impedance. Bypass capacitors must often be large values so they can absorb long transients, necessitating electrolytic types which have large series R and L.

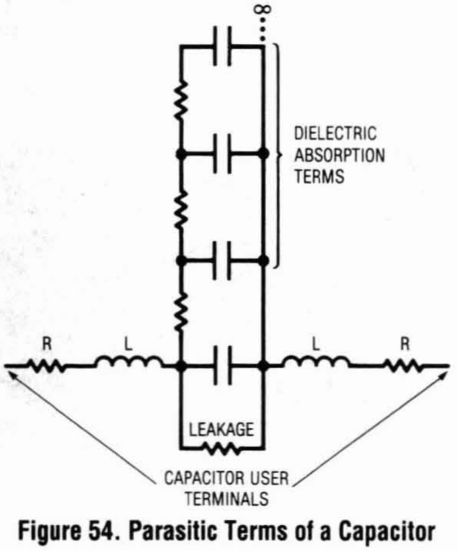

Figure 54. Parasitic Terms of a Capacitor

Different types of electrolytics and electrolytic-non-polar combinations have markedly different characteristics. Which type(s) to use is a matter of passionate debate in some circles and the test circuit (Figure 55) and accompanying photos are useful. The photos show the response of 5 bypassing methods to the transient generated by the test circuit. Figure 56 shows an unbypassed line which sags and ripples badly at large amplitudes. Figure 57 uses an aluminum 10µF electrolytic to considerably cut the disturbance, but there is still plenty of potential trouble. A tantalum 10µF unit offers cleaner response in Figure 58 and the 10µF aluminum combined with a 0.01µF ceramic type is even better in Figure 59. Combining electrolytics with non-polarized capacitors is a popular way to get good response but beware of picking the wrong duo. The right (wrong) combination of supply line parasitics and paralleled dissimilar capacitors can produce a resonant, ringing response, as in Figure 60. Caveat!

Breadboarding Techniques

The breadboard is both the designer's playground and proving ground. It is there that Reality resides, and paper (or computer) designs meet their ruler. More than anything else, breadboarding is an iterative procedure, an odd amalgam of experience guiding an innocent, ignorant,

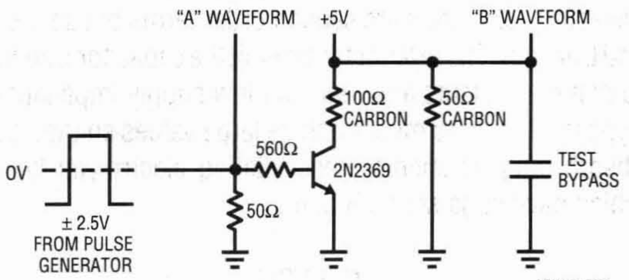

Figure 55. Bypass Capacitor Test Circuit

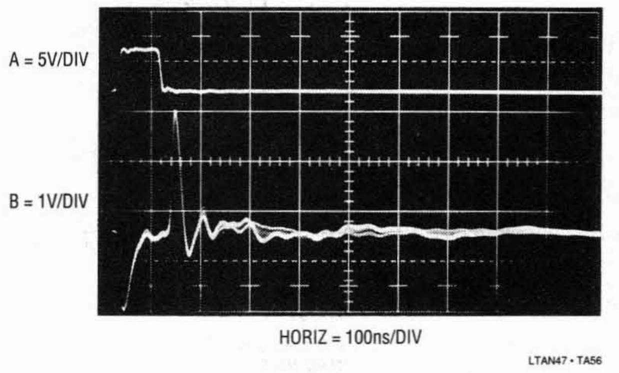

Figure 56. Response of Unbypassed Line

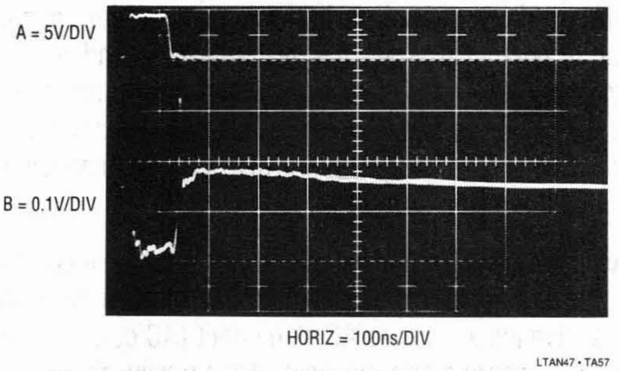

Figure 57. Response of 10µF Aluminum Capacitor

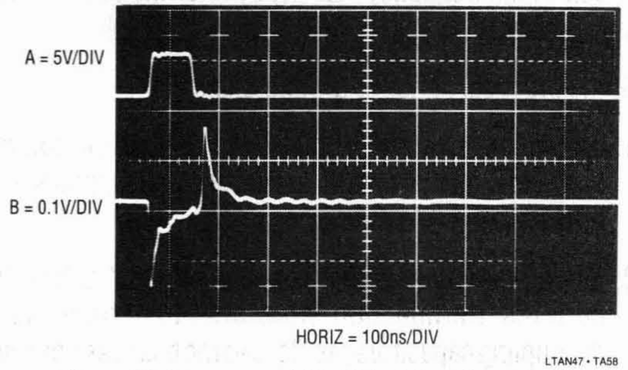

Figure 58. Response of 10µF Tantalum Capacitor

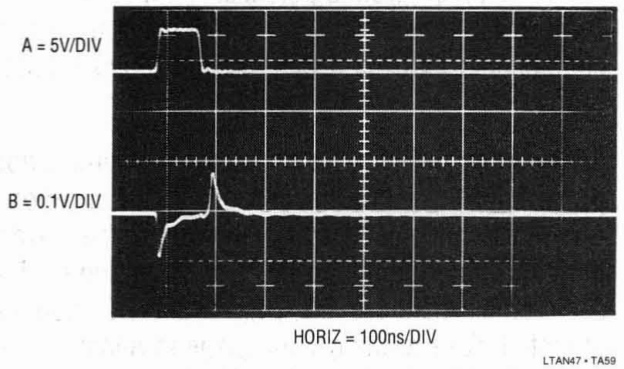

Figure 59. Response of 10µF Aluminum Paralleled by 0.01µF Ceramic

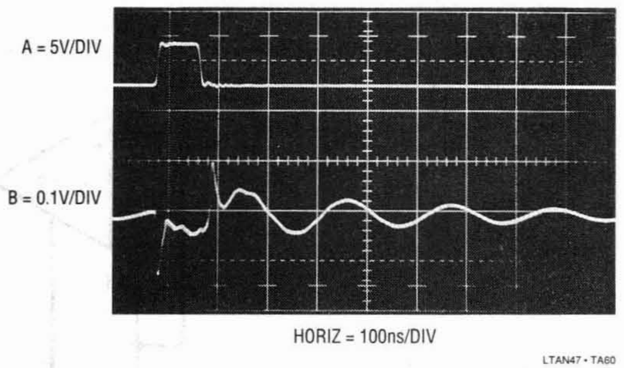

Figure 60. Some Paralleled Combinations can Ring. Try before Specifying!

explorative spirit. A key is to be willing to try things out, sometimes for not very good reasons. Invent problems and solutions, guess carefully and wildly, throw rocks and see what comes loose. Invent and design experiments, and follow them wherever they lead. Reticence to try things is probably the number one cause of breadboards that "don't work".[8] Implementing the above approach to life begins with the physical construction methods used to build the breadboard.

A high speed breadboard must start with a ground plane. Additionally, bypassing, component layout and connections should be consistent with high speed operations. Because of these considerations there is a common misconception that breadboarding high speed circuits is time consuming and difficult. This is simply not true. For high speed circuits of moderate complexity a complete and electrically correct breadboard can be assembled in 10 minutes if all necessary components are on hand. The key to rapid breadboarding is to identify critical circuit nodes and design the layout to suit them. This permits most of the breadboard's construction to be fairly sloppy, saving time and effort. Additionally, use all degrees of freedom in making connections and mounting components. Don't be bashful about bending I.C. pins to suit desired low capacitance connections, or air wiring components to achieve rapid or electrically optimum layout. Save time by using components, such as bypass capacitors, as mechanical supports for other components, such as amplifiers. It is true that eventual printed circuit construction is required, but when initially breadboarding forget about PC and production constraints. Later, when the circuit works, and is well understood, PC adaptations can be taken care of.

Figure 61's amplifier circuit is a good working example. This circuit, excerpted from the Applications section (where its electrical operation is more fully explained) is a high impedance, wideband amplifier with low input capacitance. Q1 and A1 form the high frequency path, with the 900Ω-100Ω feedback divider setting gain. A2 and Q2 close a DC stabilization loop, minimizing DC offset between the circuit's input and output. Critical nodes in this circuit include Q1's gate (because of the desired low input capacitance) and A1's input related connections (because of their high speed operation). Note that the connections associated with A2 serve at DC and are much less sensitive to layout. These determinations dominate the breadboard's construction.

Figure 62 shows initial breadboard construction. The copper clad board is equipped with banana type connectors. The connector's mounting nuts are simply soldered to the clad board, securing the connectors. Figure 63 adds A1 and the bypass capacitors. Observe that A1's leads have been bent out, permitting the amplifier to sit down on the ground plane, minimizing parasitic capacitance. Also, the bypass capacitors are soldered to the amplifier power pins right at the capacitor's body. The capacitor's lead lengths are returned to the banana power jacks. This connection method provides good amplifier bypassing

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Note 8: A much more eloquently stated version of this approach is found in Reference 12.

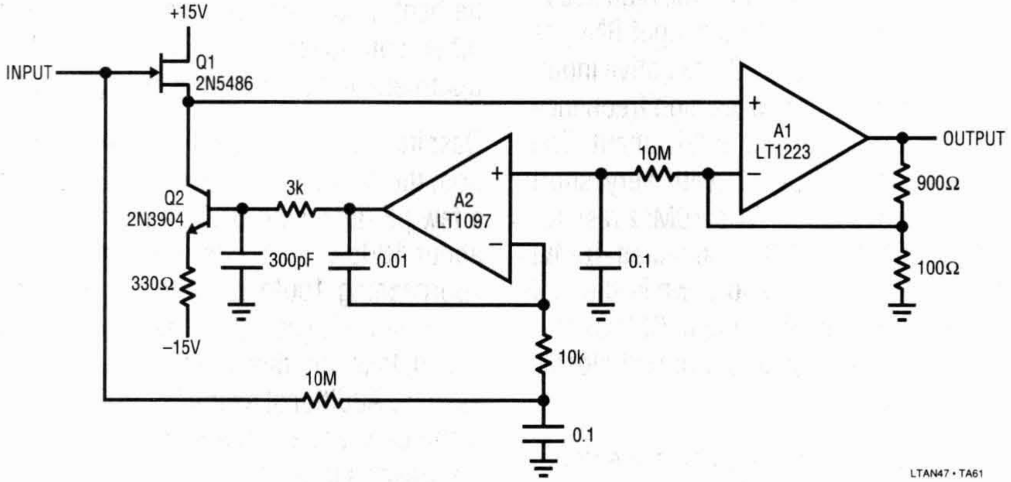

Figure 61. The Stabilized FET Input Amplifier (Applications Figure 73) to be Breadboarded

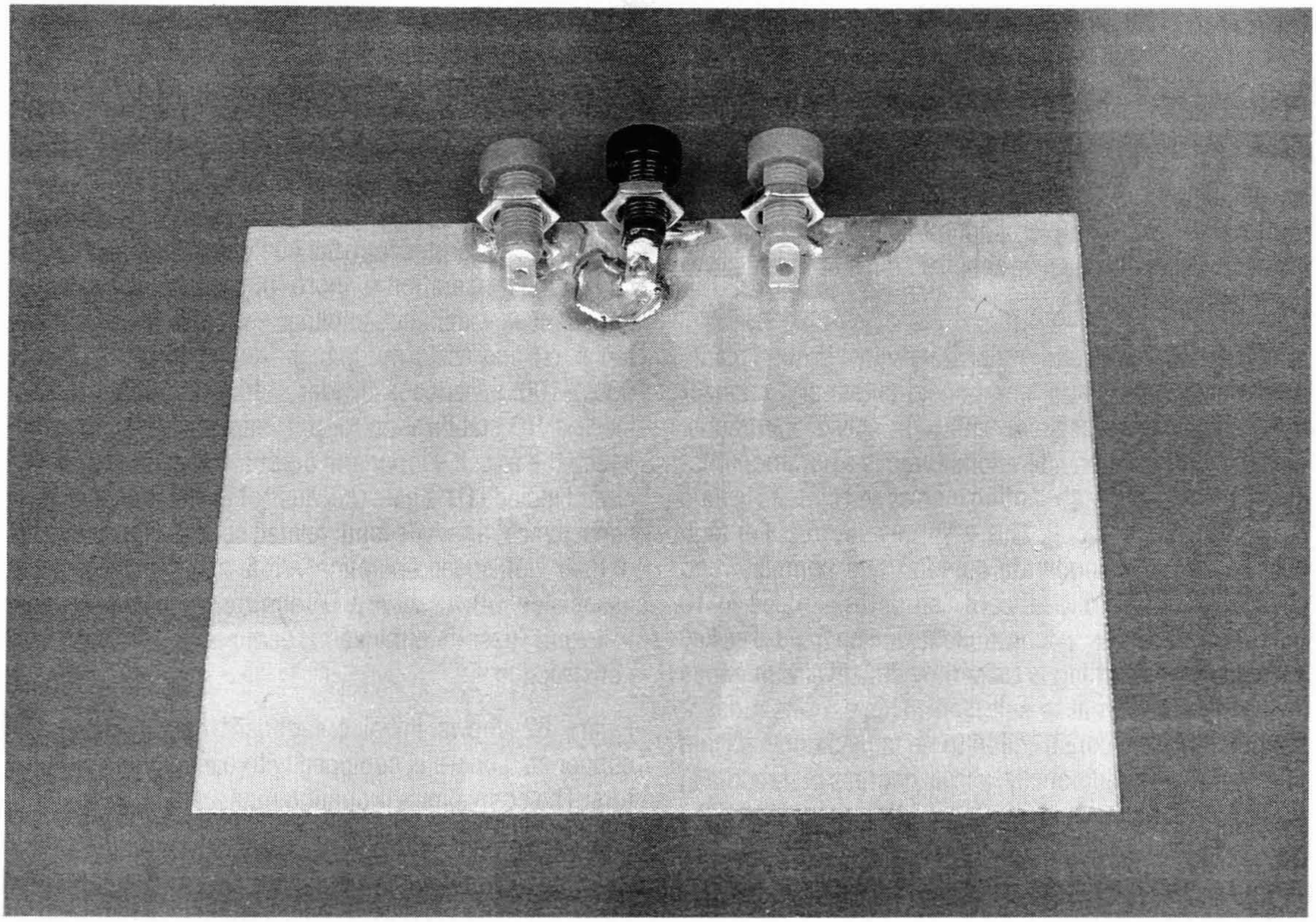

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Figure 62. The Banana Jacks are Soldered to the Copper Clad Board

while mechanically supporting the amplifier. It also eliminates separate wire runs to the power pins.

Figure 64 adds the discrete components in the high speed path. A1's gate is connected directly to the input BNC, as is the 10MΩ resistor associated with A2's negative input. Note that the end of this resistor that sees high frequency is cut very short, while the other end is left uncut. The 900Ω-100Ω divider is installed at A1, with very short connections to A1's negative input. A1's 10MΩ resistor receives similar treatment to the BNC connected 10MΩ unit; the high frequency end is cut short, while the end destined for connection to A2 remains uncut. Q2's collector and Q1's source, high speed points, are tied closely together with A1's positive input.

Finally, DC amplifier A2 and its associated components are air wired into the breadboard (Figure 65). Their DC operation permits this, while the construction technique makes connections to the previously wired nodes easy. The previously uncommitted ends of the 10MΩ resistors may be bent in any way necessary to make connections. All other components associated with A2 receive similar treatment and the circuit is ready for experimentation.

Despite the breadboard's seemingly haphazard construction, the circuit worked well. Input capacitance measured a few pF (including BNC connector) with bias current of about 100pA. Slew rate was 1000V/µs, with bandwidth approaching 100MHz. Output, even with 50mA loading, was clean, with no sign of oscillation or other instabilities. Full details on this circuit appear in the Applications section. Additional examples of breadboard construction techniques appear in Appendix F, "Additional Comments on Breadboarding".

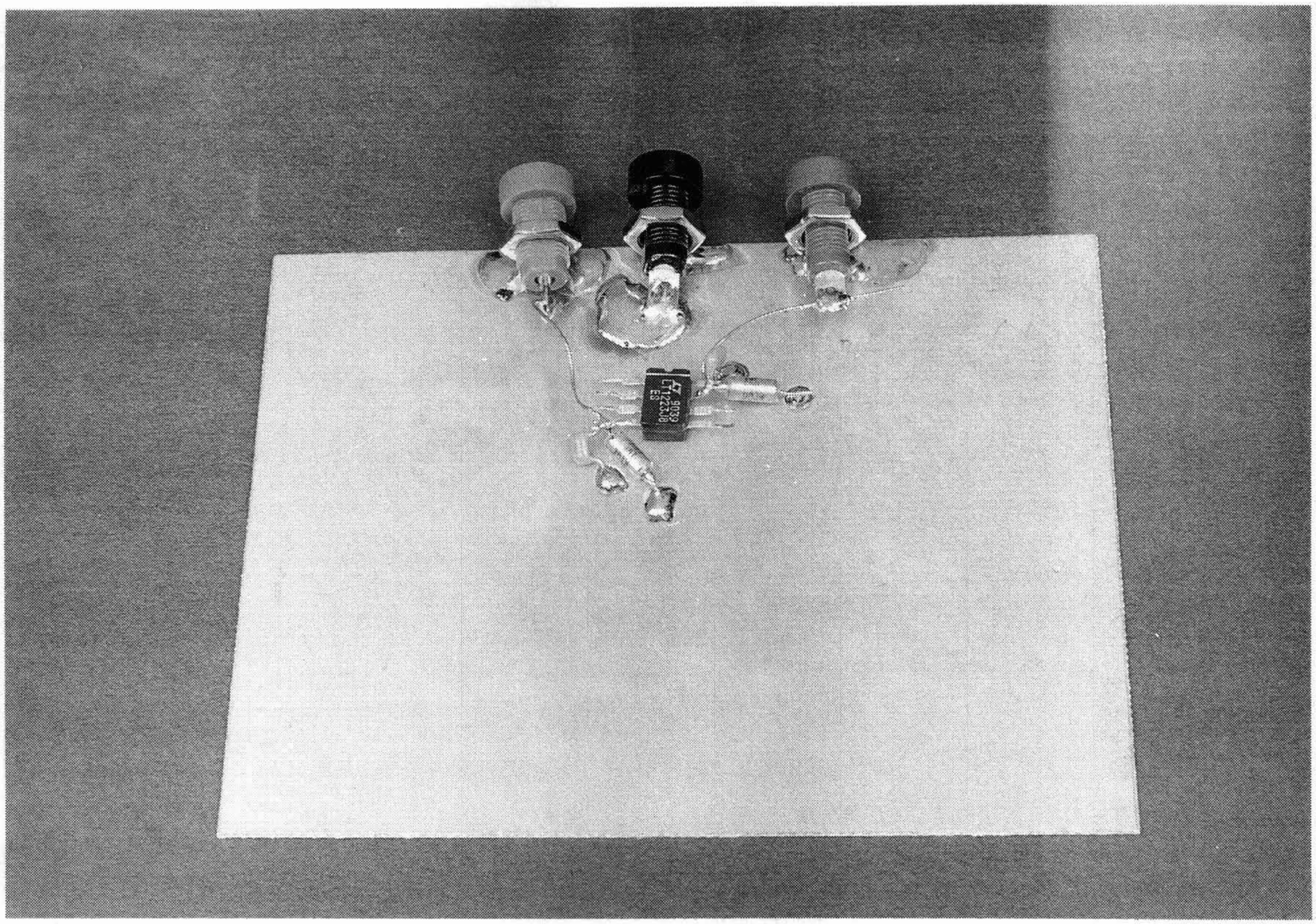

Figure 63. High Speed Amplifier A1 is Connected to Power. Bypass Capacitors Provide Support. Bending Amplifier Pins Eases Connections and Minimizes Distance to the Ground Plane

Once the breadboard seems to work, it's useful to begin thinking about PC layout and component choice for production. Experiment with the existing layout to determine just how sensitive nominally critical points are. Add controlled parasitic terms (e.g., resistors, capacitors and physical layout changes) to test for sensitivity. Gentle touching of suspect points with a finger can yield preliminary indication of sensitivity, giving clues that can be quite valuable.

In conclusion, when breadboarding, design the breadboard to be quick and easy to build, work with and modify. Observe the circuit and listen to what it is telling you before trying to get it to some desired state. Finally, don't hesitate to try just about anything; that's what the breadboard is for. Almost anything you do will cause some result — whether it's good or bad is almost irrelevant. Anything you do that enhances your ability to correlate events occurring on the breadboard can only be beneficial.

Oscillation

The forte of the operational amplifier is negative feedback. It is feedback which stabilizes the operating point and fixes the gain. However, positive feedback or delayed negative feedback can cause oscillation. Thus, a properly functioning amplifier constantly lives in the shadow of oscillation.

When oscillation occurs, several major candidates for blame are present. Power supply impedance must be low. If the supply is unbypassed, the impedance the amplifier sees at its power terminals is high, particularly at high

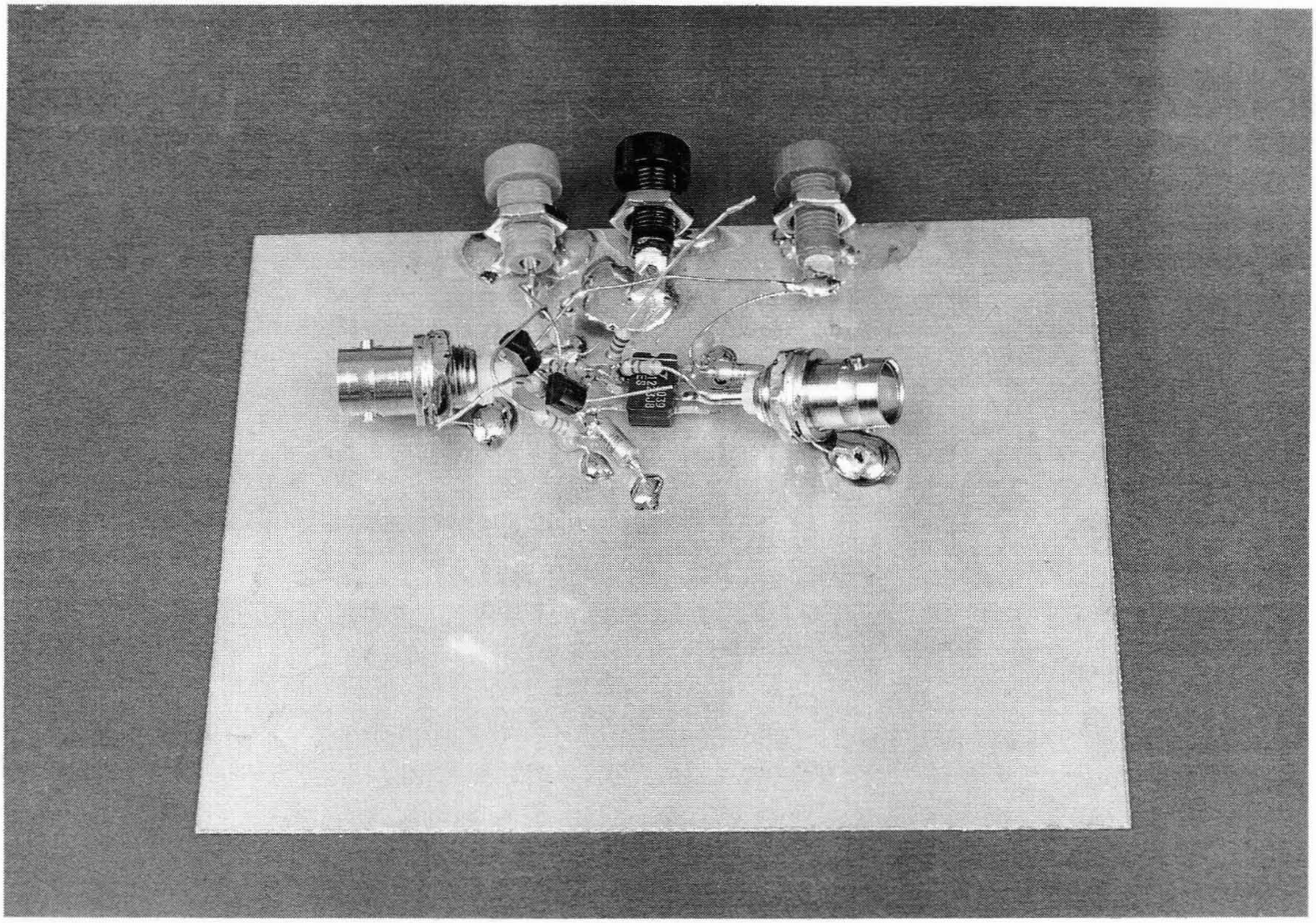

Figure 64. Additional High Speed Discrete Components and Connectors are Added. Note Short Connections at Amplifier Input Pins (Left Side of Package). 10M Resistors Uncommitted Ends are Just Visible

frequency. This impedance forms a voltage divider with the amplifier, allowing the supply to move as internal conditions in the amplifier change. This can cause local feedback and oscillation occurs. The obvious cure is to bypass the amplifier.

A second common cause of oscillation is positive feedback. In most amplifier circuits feedback is negative, although controlled amounts of positive feedback may be used. In a circuit that nominally has only negative feedback unintended positive feedback may occur with poor layout. Check for possible parasitic feedback paths and unwanted or overlooked feedback action. Always minimize (to the extent possible) impedances seen by amplifier inputs. This helps attenuate the effects of parasitic feedback paths to the inputs. Similarly, minimize exposed input trace area. Route amplifier outputs and other signals well away from sensitive nodes. Sometimes no amount of layout finesse will work and shielding is required. Use shielding only when required — extensive shielding is a sloppy substitute for good layout practice.

A final cause of oscillation is negative feedback arriving well delayed in time. Under these conditions the amplifier hopelessly tries to servo a feedback signal which consistently arrives too late. The servo action takes the form of an electronic tail chase, with oscillation centered around the ideal servo point. The most common causes of this problem are reactive loading of the amplifier (most notably capacitive loads such as cable) and circuitry, such as power amplifiers, placed within the amplifier's feedback path. Reactive loads should be isolated from the amplifier's output (and feedback path) with a resistor or power amplifier. Sometimes rolling off the amplifier's frequency

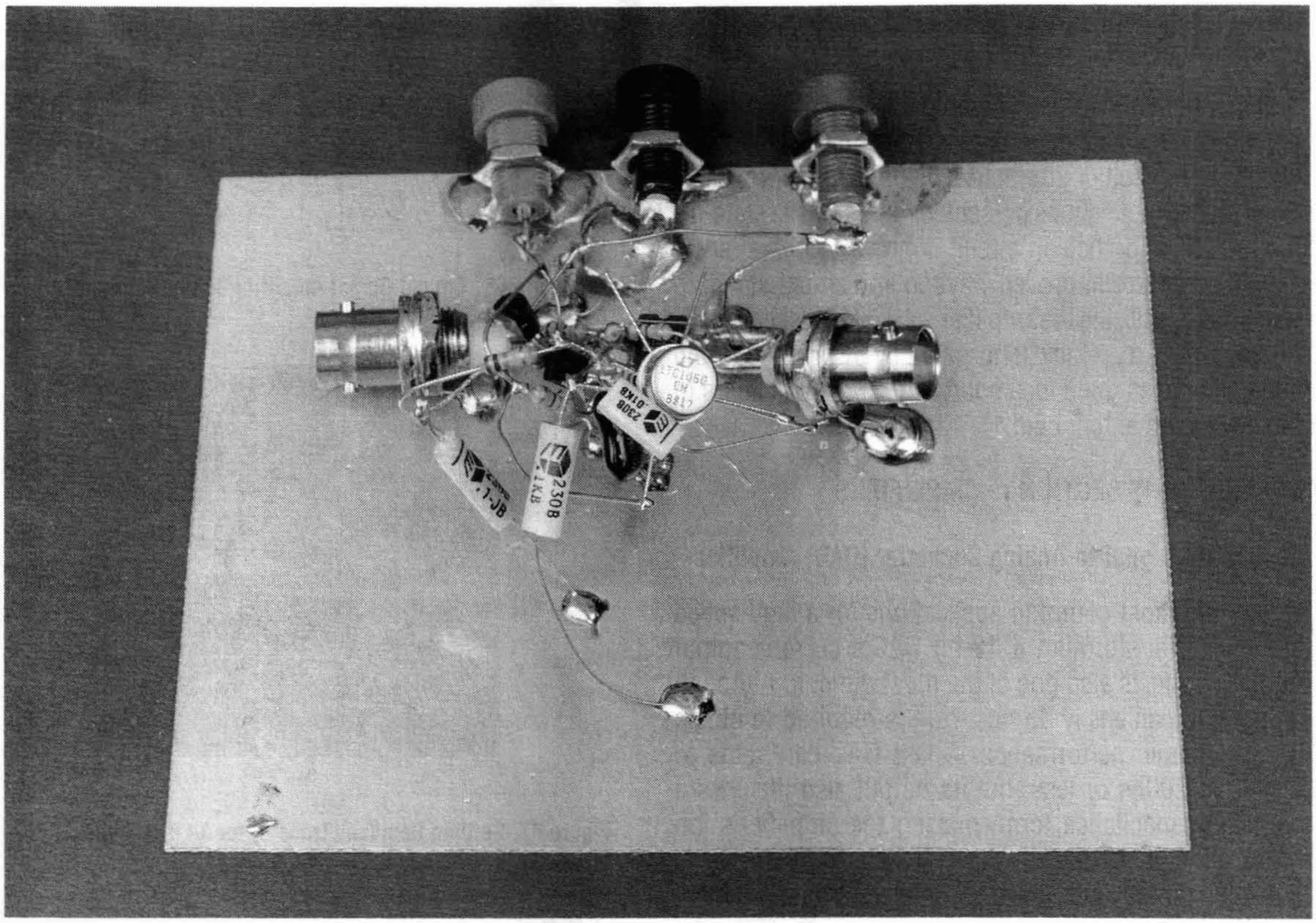

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Figure 65. DC Servo Amplifier is Wired In and Connections to 10M Resistors Completed. This Part of the Circuit is Not Layout Sensitive

response will fix the problem, but in high speed circuits this may not be an option.

Placing power gain or other type stages within the amplifier's feedback path adds time delay to the stabilizing feedback. If the delay is significant, oscillation commences. Stages operating within the amplifier's loop must contribute minimum time lag compared to the amplifier's speed capability. At lower speeds this is not too difficult, but something destined for operation within a 100MHz amplifier's loop must be *fast.* As mentioned before, rolling off the amplifier's frequency response eases the job, but is usually undesirable in a wideband circuit. Every effort should be expended to maximize the added stages bandwidth before resorting to roll-off of the amplifier. In this way the fastest overall bandwidth is achieved while maintaining stability. Appendix C, "The Oscillation Problem – Frequency Compensation Without Tears", discusses considerations surrounding operating power gain and other type stages within amplifier loops.

This completes the tutorial section. Hopefully, several notions have been imparted. First, in any measurement situation, test equipment characteristics are an integral part of the circuit. At high speed and high precision this is particularly the case. As such, it is imperative to know your equipment and how it works. There is no substitute for intimate familiarity with your tool's capabilities and limitations.[9]

In general, use equipment you trust and measurement techniques you understand. Keep asking questions and

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Note 9: Further exposition and *kvetching* on this point is given in Reference 13.

don't be satisfied until everything you see on the oscilloscope is accounted for and makes sense.

Fast monolithic amplifiers, combined with the precautionary notes listed above, permit fast linear circuit functions which are difficult or impractical using other approaches. Some of the applications presented represent the state-of-the-art for a particular circuit function. Others show simplified and/or improved ways to implement standard functions by utilizing the amplifier's easily accessed speed. All have been carefully (and painfully) worked out and should serve as good idea sources for potential users of the device. Have fun. I did.

APPLICATIONS SECTION I - AMPLIFIERS

Fast 12-Bit Digital-to-Analog Converter (DAC) Amplifier

One of the most common applications for a high speed amplifier, transforming a 12-bit DAC's current output into a voltage, is also one of the most difficult. Although an op amp can easily do this, care is required to obtain good dynamic performance. A fast DAC can settle to 0.01% in 200ns or less, but its output also includes a parasitic capacitance term, making the amplifier's job more difficult. Normally, the DAC's current output is unloaded directly into the amplifier's summing junction, placing the parasitic capacitance from ground to the amplifier's input. The capacitance introduces feedback phase shift at high frequencies, forcing the amplifier to hunt and ring about the final value before settling. Different DACs have different values of output capacitance. CMOS DACs have the highest output capacitance, in the 100pF-150pF range, and it varies with code. Bipolar DACs typically have 20pF-30pF of capacitance, stable over all codes. As such, bipolar DACs are almost always used where high speed is required. Figure 66 shows the popular AD565A 12-bit DAC with an LT1220 output op amp. Figure 67 shows clean 0.01% settling in 280ns (Trace B) to an all-bits-on input step (Trace A). The requirements for obtaining Trace B's display are not trivial, and are fully detailed in Appendix B, "Measuring Amplifier Settling Time".

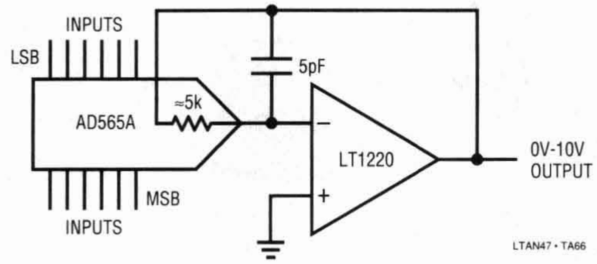

Figure 66. Typical Output Amplifier Configuration for a 12-Bit D-to-A Converter

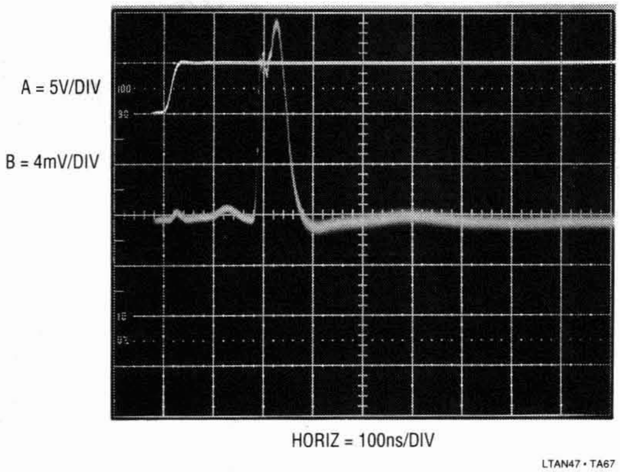

Figure 67. Settling Residue (Trace B) for All Bits Switched On (Trace A). Output is Fully Settled in 280ns

2-Channel Video Amplifier

Figure 68 shows a simple way to multiplex two video amplifiers onto a single 75Ω cable. The appropriate amplifier is activated in accordance with the truth table in the figure[10]. Amplifier performance includes 0.02% differential gain error and 0.1° differential phase error. The 75Ω back termination looking into the cable means the amplifiers must swing 2Vp-p to produce 1Vp-p at the cable output, but this is easily handled.

Simple Video Amplifier

Figure 69 is a simpler version of Figure 68. This is a single channel video amplifier, arranged (in this case) for a gain of ten. The double cable termination is retained and the circuit delivers a bandwidth of 55MHz.

Loop Through Cable Receivers

Figure 70 is another cable related circuit. Here, the LT1193 differential amplifier simply hangs across a distribution cable, extracting the signal. The amplifier's true differential inputs reject common-mode signals. As in the previous

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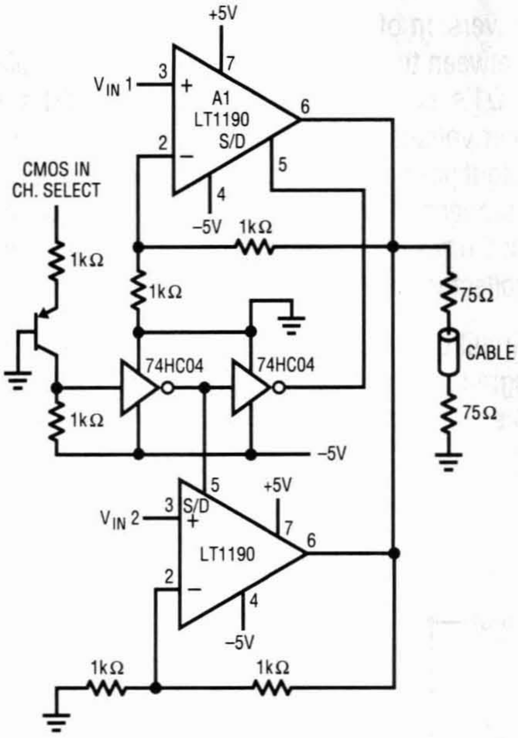
Note 10: A truth table in an op amp circuit! *Et tu*, LTC!!


+5V
V_{IN} 1
3
+
A1
LT1190
S/D
7
6
2
−
5
4
CMOS IN
CH. SELECT
−5V
1kΩ
1kΩ
1kΩ
75Ω
74HC04
74HC04
CABLE
1kΩ
75Ω
−5V
5
+5V
V_{IN} 2
3
S/D
+
LT1190
7
6
2
−
4
−5V
1kΩ
1kΩ

TRUTH TABLE

INPUT SELECT	A1 OUTPUT	A2 OUTPUT
5V	ACTIVE	INACTIVE
0V	INACTIVE	ACTIVE

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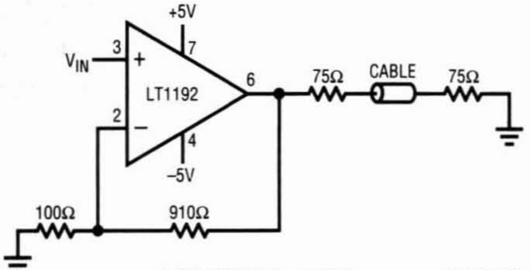
Figure 68. 2-Channel Multiplexed Video Amplifier

circuit, differential gain and phase errors measure 0.02% and 0.1°, respectively. A separate input permits DC level adjustment.

DC Stabilization – Summing Point Technique

Often it is desirable to obtain the precision offset of a DC amplifier with the bandwidth of a fast device. There are a variety of techniques for doing this. Which method is best is heavily application dependent, so several configurations are presented.

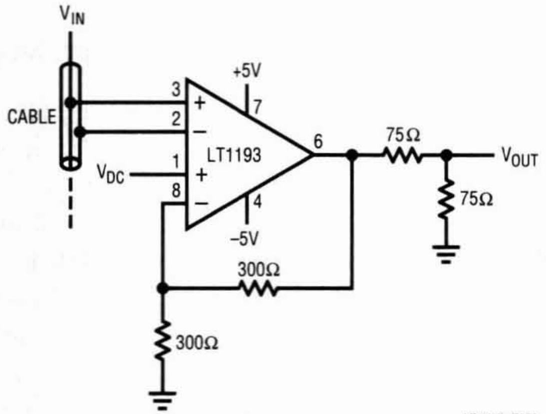
Figure 71 shows a composite made up of an LT1097 low drift device and an LT1191 high speed amplifier. The overall circuit is a unity gain inverter with the summing node located at the junction of the two 1k resistors. The LT1097 monitors this summing node, compares it to ground and drives the LT1191's positive input, completing a DC stabilizing loop around the LT1191. The 100kΩ-0.01µF time constant at the LT1097 limits its response to low frequency signals. The LT1191 handles high frequency inputs while the LT1097 stabilizes the DC operating point. The 4.7k-220Ω divider at the LT1191 prevents excessive input overdrive during start-up. This circuit combines the LT1097's 35µV offset and 1.5V/°C drift with the LT1191's 450V/µs slew rate and 90MHz bandwidth. Bias current, dominated by the LT1191, is about 500nA.


+5V
V_{IN}
3
+
7
LT1192
6
75Ω
CABLE
75Ω
2
−
4
−5V
100Ω
910Ω

−3dB BANDWIDTH = 55MHz

LTAN47 • TA69

Figure 69. Double Terminated Cable Driver


V_{IN}
+5V
CABLE
3
+
7
2
−
1
LT1193
6
75Ω
V_{OUT}
V_{DC}
+
8
−
4
75Ω
−5V
300Ω
300Ω

LTAN47 • TA70

Figure 70. Cable Sense Amplifier for Loop Through Connections with DC Adjust

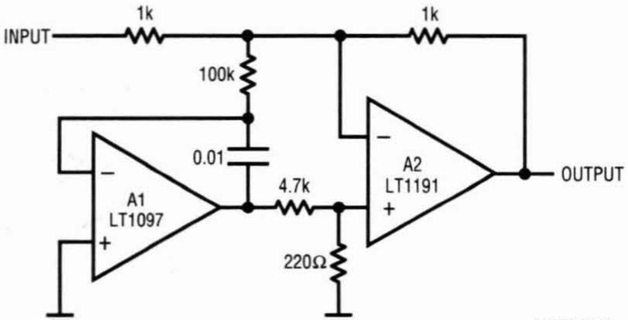

INPUT
1k
1k
100k
0.01
−
A1
LT1097
+
4.7k
−
A2
LT1191
+
OUTPUT
220Ω

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Figure 71. A1 DC Stabilizes A2 by Forcing the Summing Point to Zero

DC Stabilization – Differentially Sensed Technique

Figure 72 is similar to Figure 71, except that the sensing is done differentially, preserving access to both fast amplifier inputs. The LT1097 measures the DC error at the LT1220's input terminals and biases its offset pins to force offset within 50µV. The offset pin biasing at the LT1220 is arranged so the LT1097 will always be able to find the servo point. The 0.01µF capacitor rolls off the LT1097 at low frequency and the LT1220 handles high frequency signals. The combined characteristics of these amplifiers yield the following performance:

Offset Voltage	50µV
Offset Drift	1µV/°C
Slew Rate	250V/µs
Gain-Bandwidth	45MHz

DC Stabilization – Servo Controlled FET Input Stage

Figure 73 shows a wideband, highly stable gain-of-ten with high input impedance. Input capacitance is about 3pF. Q1 and Q2 constitute a simple, high speed FET input buffer. Q1 functions as a source follower, with the Q2 current source load setting the drain-source channel current. The LT1223 provides a 100MHz bandwidth gain of ten. Normally, this open loop configuration would be quite drifty because there is no DC feedback. The LT1097 contributes this function to stabilize the circuit. It does this by comparing the filtered circuit output to a similarly filtered version of the input signal. The amplified difference between these signals is used to set Q2's bias, and hence Q1's channel current. This forces Q1's V_{GS} to whatever voltage is required to match the circuit's input and output potentials. The capacitor at A1 provides stable loop compensation. The RC network in A1's output prevents it from seeing high speed edges coupled through Q2's collector-base junction.

This circuit constitutes an extremely wideband (Q1 does not degrade A2's 100MHz performance), high input impedance amplifier. With an input capacitance of 3pF and

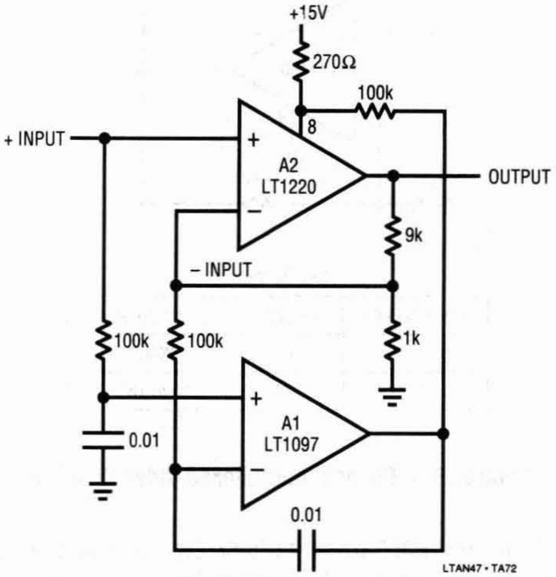

Figure 72. A1 DC Stabilizes A2 by Forcing the Offset Pins to Produce a 0V Difference at A2's Inputs

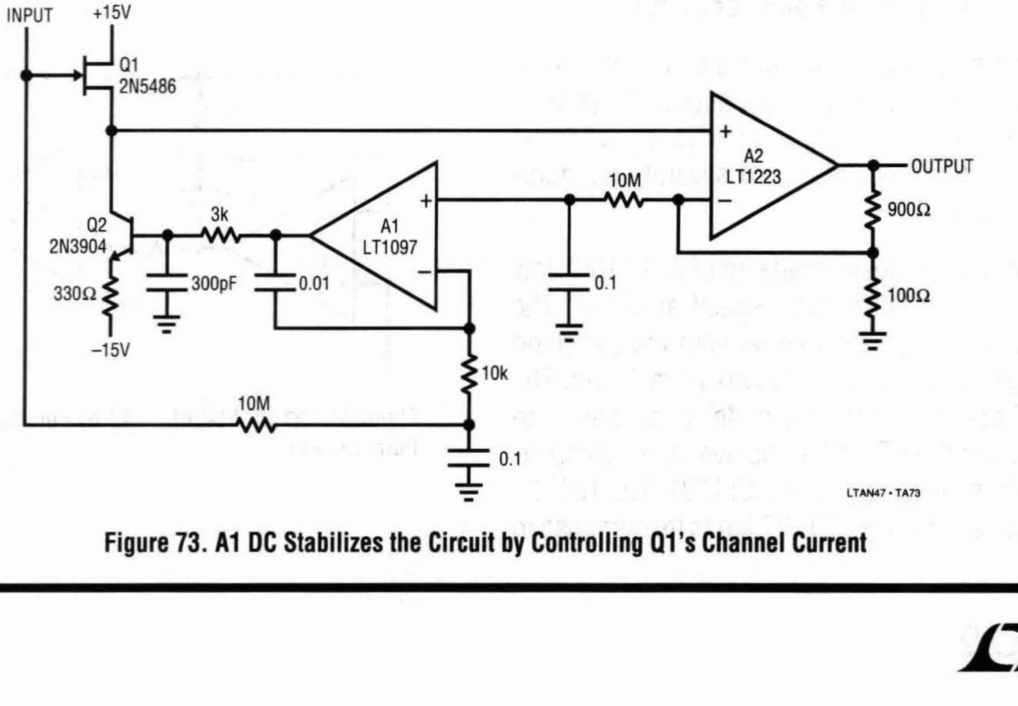

Figure 73. A1 DC Stabilizes the Circuit by Controlling Q1's Channel Current

bias current of 100pA, it is well suited for probing or as an ATE pin amplifier. As shown, gain is ten, but other gains are possible by varying the feedback ratio.

DC Stabilization – Full Differential Inputs with Parallel Paths

Figure 74 shows a way to get full differential inputs with DC stabilized operation. This circuit combines the output of two differential input amplifiers for overall DC corrected wideband operation. A1 and A2 both differentially sense the input at gains of ten. Wideband A1 feeds output amplifier A3 via a highpass network, while the slower A2 contributes DC and low frequency information to A3. A2 does not see high frequency inputs, because they are filtered by the 2k-200pF lowpass networks at its inputs. If the gain and bandwidth of the high and low frequency paths complement each other, A3's output should be an undistorted, amplified version (in this case × 10) of the input. Figure 75 shows this to be the case. Trace A is one side of a differential input applied to the circuit. Trace B is A1's output taken at the 500Ω potentiometer - 0.001µF junction. Trace C is A2's output. With the AC gain and DC gain match trims properly adjusted, the two paths' contributions match up and Trace D is singularly clean, with no residue. The adjustments are optimized by trimming the AC gain for the squarest corners and the DC gain match for a flat top. Bandwidth for this circuit exceeds 35MHz, slew rate is 450V/µs and DC offset about 200µV.

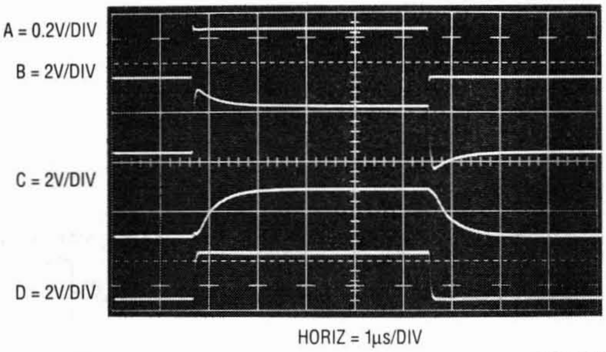

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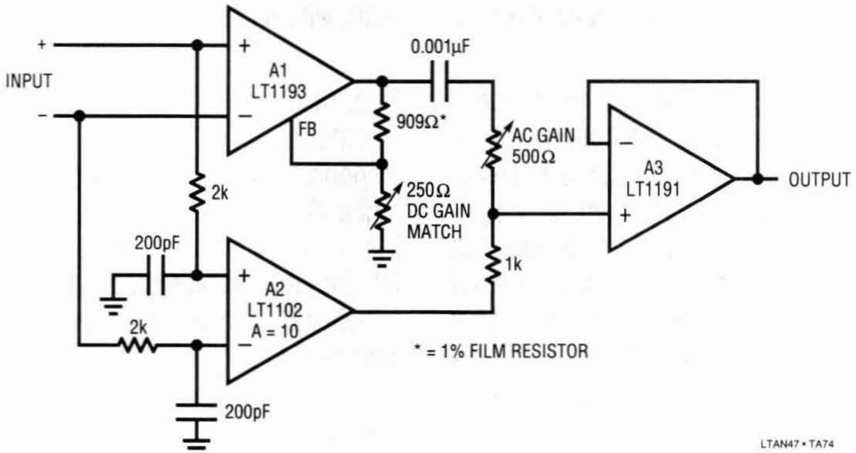
Figure 75. Waveforms for the Parallel Path Differential Amplifier. Trace A is the Input; B, C and D are the High Pass, Low Pass and Output Nodes, Respectively

DC Stabilization – Full Differential Inputs, Gain-of-1000 with Parallel Paths

Figure 76 is a very powerful extension of the previous circuit. Operation is similar, but gain is increased to 1000. Bandwidth is about 35MHz, rise time equals 7ns and delay is inside 7.5ns. Full power response is available to 10MHz, with input noise about 15µV broadband. This kind of speed, coupled with full differential inputs, the gain of 1000, DC stability, and low cost make the circuit broadly applicable in wideband instrumentation. As before, two differential amplifiers, A1 and A2, simultaneously sense the inputs. In this case A1 is the popular and economical 592-733 type, operating at a gain of 100.[11] A1's differential outputs feed output amplifier A3 via 1µF-1kΩ high pass networks which strip off A1's DC content. A2, a precision DC differential type, operates in similar fashion to the previous circuit, supplying DC and low frequency



LTAN47 • TA74

Figure 74. A Parallel Path DC Stabilized Differential Amplifier. High Frequency Signals Go through A1, while A2 Handles DC and Low Frequency. A3 Sums Both Paths

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[11] **Note 11:** For assistance in following circuit signal flow, the schematic of this device is included in the figure.

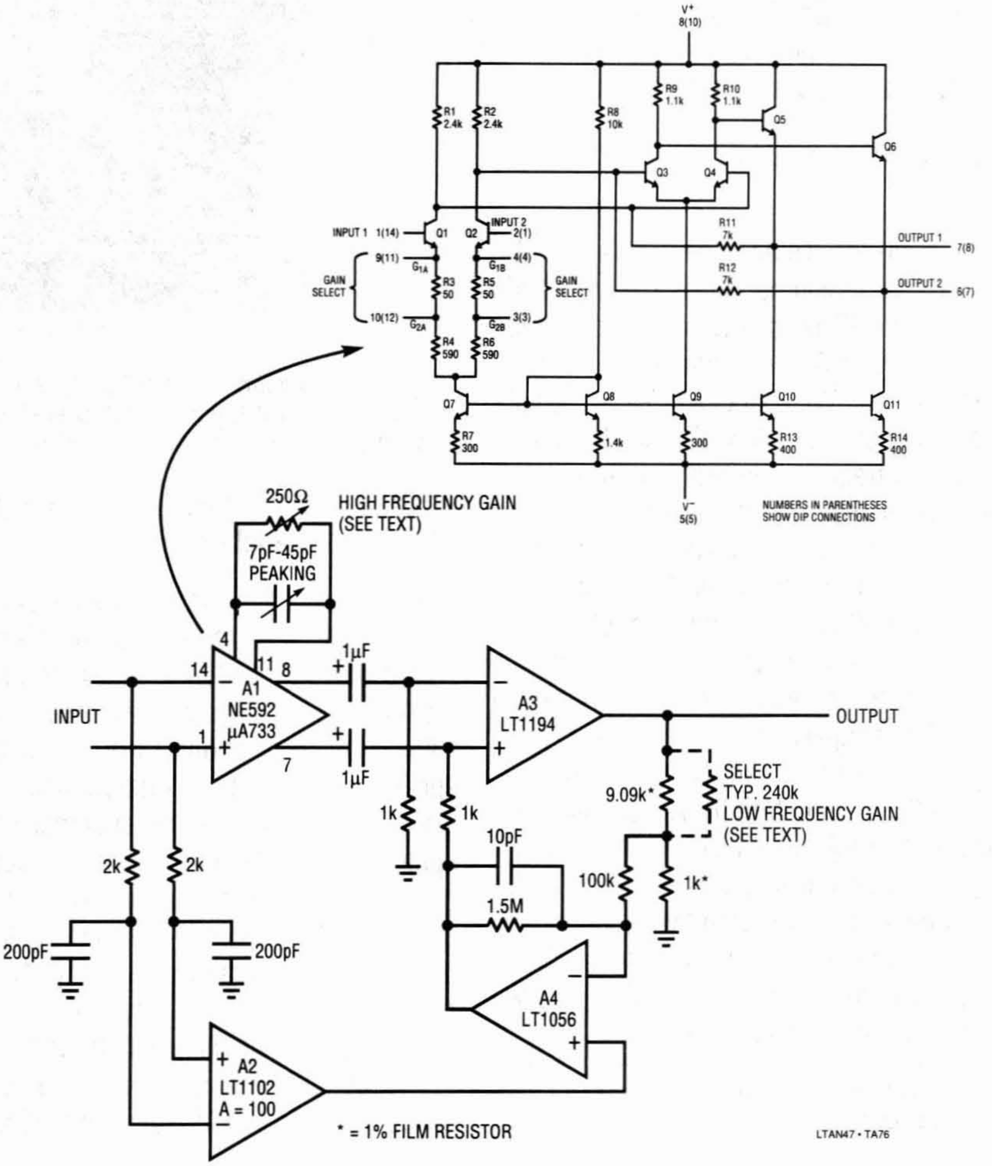

V+
8(10)
R1 2.4k
R2 2.4k
R8 10k
R9 1.1k
R10 1.1k
Q5
Q6
Q3
Q4
INPUT 1 1(14)
Q1
Q2
INPUT 2 2(1)
9(11)
G_{1A}
G_{1B}
4(4)
GAIN SELECT
R3 50
R5 50
GAIN SELECT
10(12)
G_{2A}
G_{2B}
3(3)
R4 590
R6 590
R11 7k
OUTPUT 1 7(8)
R12 7k
OUTPUT 2 6(7)
Q7
Q8
Q9
Q10
Q11
R7 300
1.4k
300
R13 400
R14 400
V−
5(5)
NUMBERS IN PARENTHESES SHOW DIP CONNECTIONS
250Ω
HIGH FREQUENCY GAIN (SEE TEXT)
7pF-45pF PEAKING
4
14
11
8
1µF
1µF
A1
NE592
µA733
1
7
INPUT
A3
LT1194
OUTPUT
SELECT TYP. 240k LOW FREQUENCY GAIN (SEE TEXT)
9.09k*
1k
1k
10pF
1.5M
100k
1k*
2k
2k
200pF
200pF
A4
LT1056
A2
LT1102
A = 100
* = 1% FILM RESISTOR
LTAN47 • TA76

Figure 76. A Full Differential, Parallel Path Amplifier. Gain is 1000, with 38MHz Bandwidth. Delay is Inside 7.5ns and Rise Time Under 7ns

information to A3 at a trimmed gain of 100. In this case output amplifier A3 is a differential gain block with a nominal committed gain of 10. This change is necessitated by A1's differential output, which must be single-ended to obtain the circuit's output. As such A2 does not directly apply its low frequency information to A3 as it did before. Instead, A4 measures the difference between A2's output and a divided down portion of A3's output. A4's output, biasing A3's positive input via the 1kΩ resistor, closes a loop around the circuit's DC-low frequency path. The divider feeding A4's negative input is adjusted so that the circuit's DC gain is known and equal to its AC gain.

Figure 77 shows the circuit's response to a 60ns, 2.5mV amplitude pulse (Trace A). The X1000 output (Trace B) responds cleanly, with delay and rise time in the 5ns-7ns range. Some small amount of peaking is evident, although it may be trimmed with the peaking adjustment at A1. Figure 78 plots the circuit's gain vs frequency. Gain is flat within 1/2dB to 20MHz, with the –3dB point at 38MHz. Figure 77's edge peaking shows up here as a very slight gain increase starting around 1MHz and continuing out to about 15MHz. The peaking trim will eliminate this effect.

To use this circuit, put in a low frequency or DC signal of known amplitude and adjust the low frequency gain for a

X1000 output after the output has settled. Next, adjust the high frequency gain so that the signal's front and rear corners have amplitudes identical to the settled portion. Finally, trim the peaking adjustment for best settling of the output pulse's front and rear corners.

Figure 79 shows input (Trace A) and output (Trace B) waveforms with all adjustments properly set. Fidelity is excellent, with no aberrations or other artifacts of the parallel path operation evident. Figure 80 shows the effects of too much AC gain; excessive peaking on the edges with proper amplitude indicated only after the AC channel transitions through its highpass cut off. Similarly, excessive DC gain produces Figure 81's traces. The AC gain path provides proper initial response, but too much DC gain forces a long, tailing response to an incorrect amplitude.

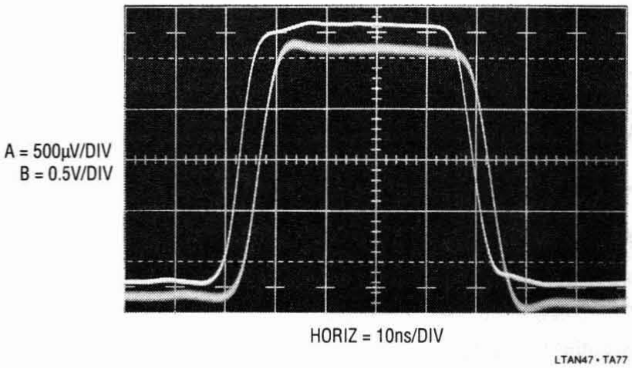
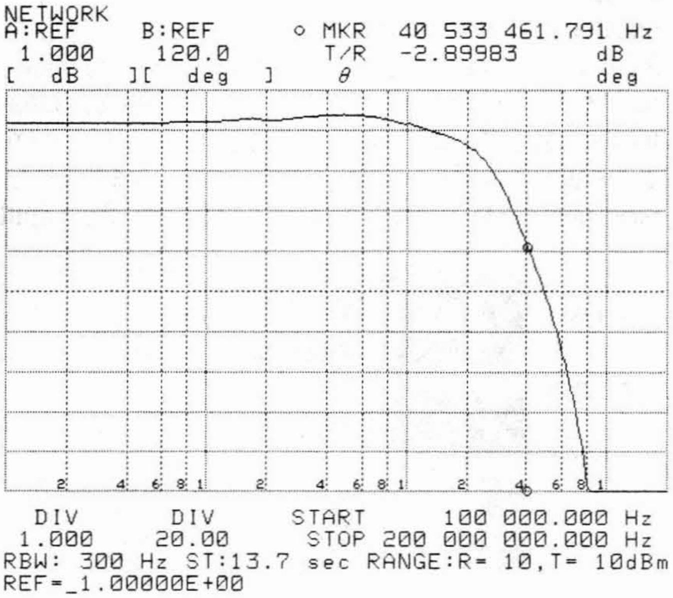


Figure 77. Pulse Response for the X1000 Differential Amplifier. Fidelity is Quite Good, with Only Slight Output Peaking (Trace B)



```
NETWORK
A:REF      B:REF        ○ MKR   40 533 461.791 Hz
 1.000      120.0          T/R   -2.89983         dB
[  dB    ][  deg   ]        θ                     deg

     DIV        DIV       START        100 000.000 Hz
 1.000      20.00        STOP 200 000 000.000 Hz
RBW:  300 Hz ST:13.7 sec RANGE:R= 10,T= 10dBm
REF=_1.00000E+00
```

Figure 78. Gain vs Bandwidth for the X1000 Differential Amplifier. Peaking Noted in Figure 77 Shows up as 0.25dB Peak at 5MHz, Which Could be Trimmed Out

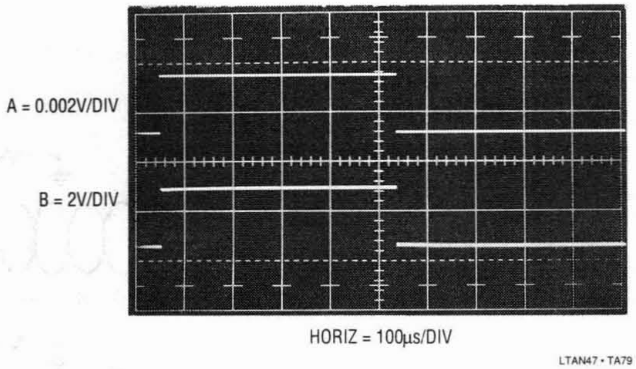


Figure 79. Response of X1000 Amplifier with Bandwidth Crossover Points Properly Adjusted. A = Input; B = Output

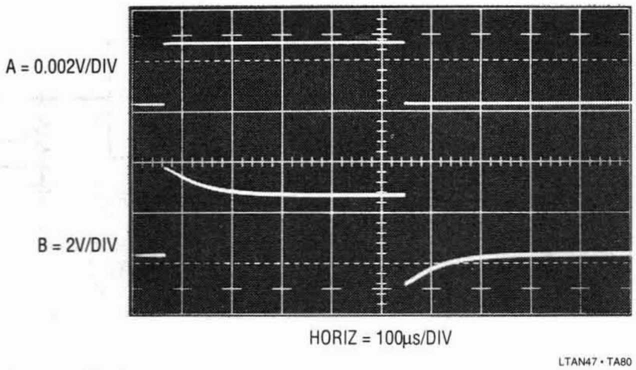


Figure 80. Response of X1000 Amplifier with Excessive AC Gain. A = Input; B = Output

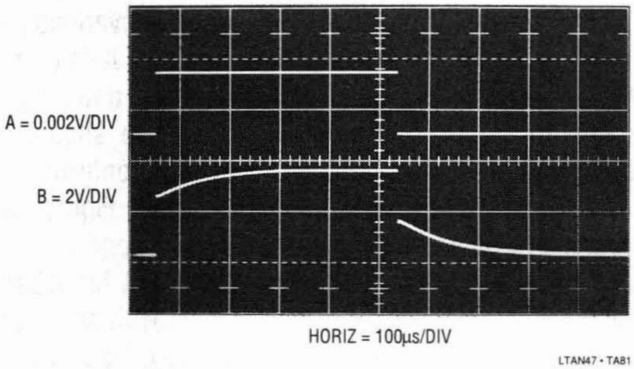


Figure 81. Response of X1000 Amplifier with Too Much DC Gain. A = Input; B = Output

High Speed Differential Line Receiver

High speed analog signals transmitted on a line often pick up substantial common-mode noise. Figure 82 shows a simple, fast differential line receiver using the LT1194

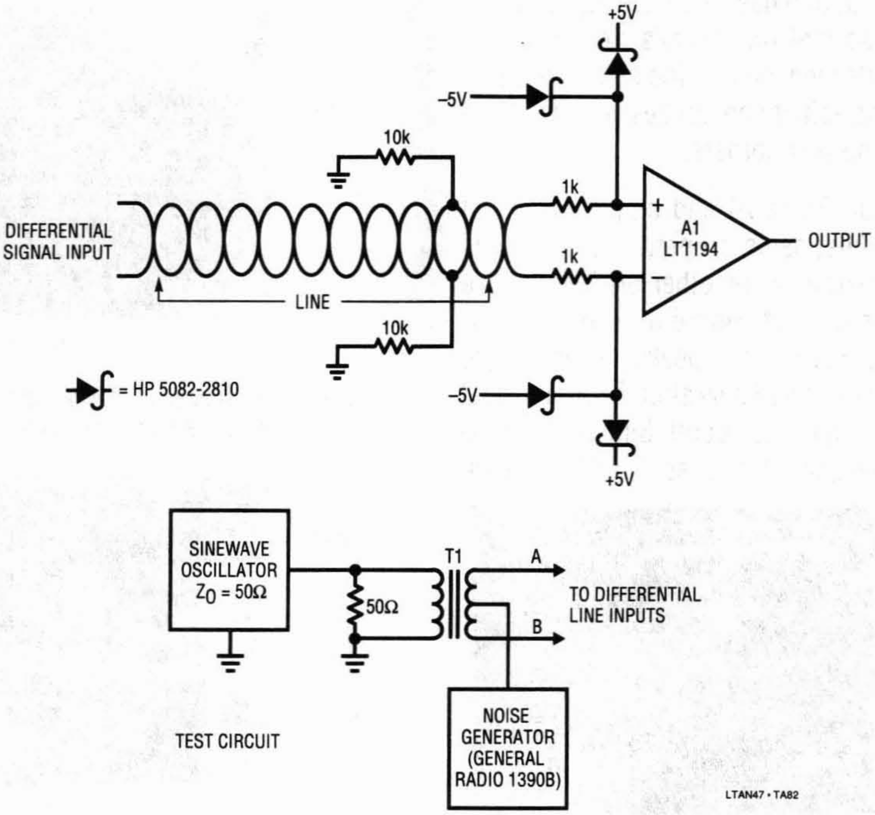

+5V
–5V
10k
1k
DIFFERENTIAL SIGNAL INPUT
A1
LT1194
OUTPUT
1k
LINE
10k
= HP 5082-2810
–5V
+5V
SINEWAVE OSCILLATOR
Z_O = 50Ω
50Ω
T1
A
TO DIFFERENTIAL LINE INPUTS
B
NOISE GENERATOR (GENERAL RADIO 1390B)
TEST CIRCUIT
LTAN47 • TA82

Figure 82. Simple, Full Differential Line Receiver

gain-of-ten differential amplifier. The differential line is fed to A1. The resistor-diode networks prevent overload and insure input bias for A1 under all conditions. A1's output represents the difference of the two line input times a gain of ten. In theory, all common-mode noise should be rejected. The test circuit shown in the figure confirms this. The sinewave oscillator drives T1 (Trace A, Figure 83), producing a differential line output at its secondary. T1's secondary is returned to ground through a broadband noise generator, flooding the line inputs with common-mode noise (traces B and C are A1's inputs). Trace D, A1's X10 version of the differential signal at its inputs, is clean with no visible noise or disturbances. This circuit will easily provide a clean output with DC-5MHz noise dominating signal by a 100:1 ratio.

Transformer Coupled Amplifier

Figure 84 shows another way to achieve high common-mode rejection. Additionally, this circuit has the advantage of true 3 port isolation. The input, gain stage, and output are all galvanically isolated from each other. As such, this configuration is useful where large common-mode differences are encountered or where ground integrity is uncertain. A1 is set up in a simple gain of 11. T1 feeds its input, and the output is taken from T2. Figure 85 shows results for a 4MHz input, with all "•" designated transformer leads referred to ground. The input (Trace A, Figure 85) is applied to T1, whose output (Trace B) feeds A1. A1 takes gain, and its output (Trace C) feeds T2. T2's output

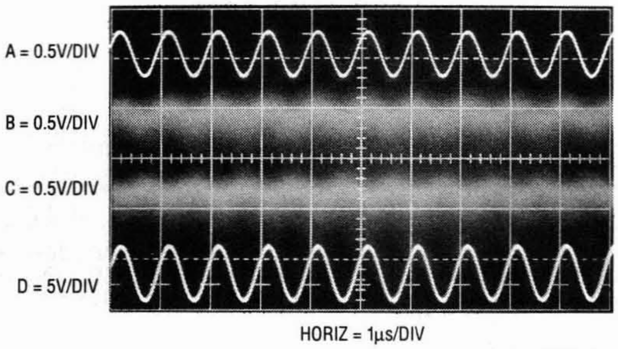


Figure 83. Differential Line Receiver Easily Pulls Out a Signal Buried in Common-Mode Noise. Output is Clean, Despite 100:1 Noise-to-Signal Ratio

(Trace D) is the circuit's output. Phase shift is evident, although tolerable. T1 and T2 are very wideband devices, with low phase shift. Note the negligible phase difference between the A-B and C-D trace pairs. A1 contributes essentially the entire phase error. Using the transformers specified, the circuit's low frequency cut-off is about 10kHz.

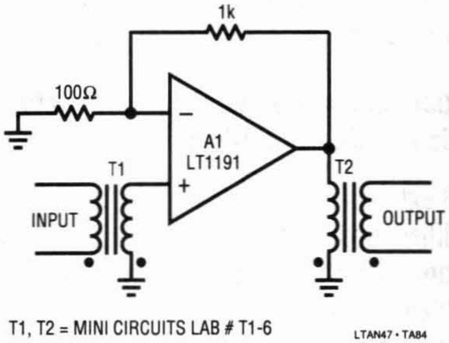


Figure 84. Transformer Coupled Amplifier. Note That A1 is Galvanically Isolated From Input and Output Nodes

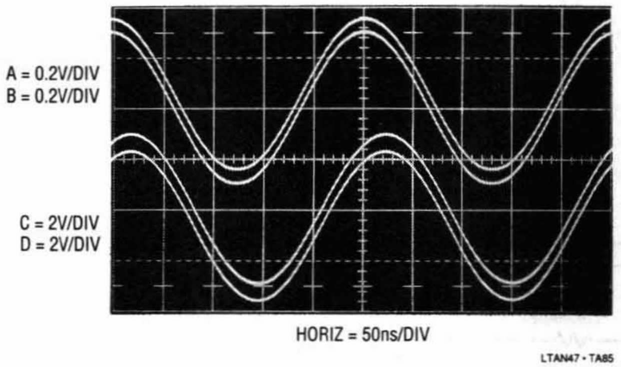


Figure 85. Transformer Coupled Amplifier Responds to an Input (Trace A) with A Slightly Phase Shifted Output (Trace D). Traces B and C are T1 Secondary and T2 Primary, Respectively

Differential Comparator Amplifier with Adjustable Offset

It is often desirable to examine or amplify one particular portion of a signal while rejecting all other portions. At high speed this can be difficult, because the amplifier may see fast, large common-mode swings. Recovery from such activity usually is dominated by saturation effects, making the amplifier's output questionable. The LT1193's differential amplifier's fast overload recovery permits this function, maintaining output fidelity to the input signal. Additionally, the input level amplitude at which amplification begins is settable, allowing any amplitude defined point to be selected. In Figure 86, A1, the LT1019 reference and associated components form an adjustable, bipolar voltage source which is coupled to differential amplifier A2's negative input. The input signal biases A2's positive input with A2's gain set by R1 and R2, in accordance with the equation given.

Input signals below A2's negative input levels maintain A2's output in saturation, and no signal is seen at the output. When the positive input rises above the negative input's bias point A2 becomes active, providing an amplified version of the instantaneous difference between its inputs. Figure 87 shows what happens when the output of a triangle wave generator (Trace A) is applied to the circuit. Setting the bias level just below the triangle peak permits high gain, detailed operation of the turnaround at the peak. Switching residue in the generator's output is clearly observable in Trace B. Appropriate variations in the voltage source setting would permit more of the triangle

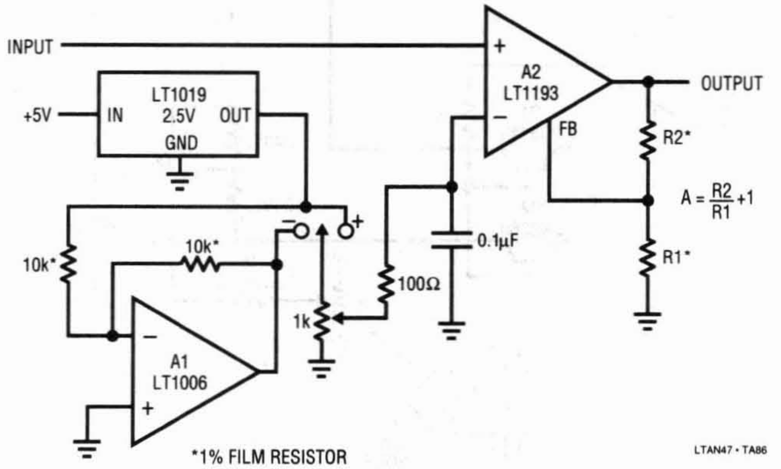


Figure 86. Fast Differential Comparator Amplifier with Settable Offset

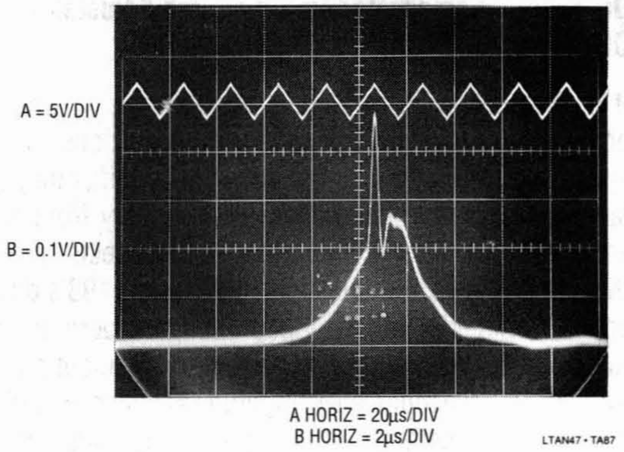


Figure 87. The Differential Comparator Amplifier Extracting Signal Detail From a Triangle Waveform's Peak. Triangle Generator's Switching Artifacts are Clearly Evident

slopes to be observed, with attendant loss of resolution due to oscilloscope overload limitations. Similarly, increasing A2's gain allows more amplitude detail while placing restrictions on how much of the waveform can be displayed. It is worth noting that this circuit performs the same function as differential plug-in units for oscilloscopes. This circuit's output is accurate and settled to 0.1% 100ns after it enters its linear region.

Differential Comparator Amplifier with Settable Automatic Limiting and Offset

Figure 88 extends the previous circuit's operation, allowing amplified observation of information between two settable, amplitude defined points. The amplitude setpoints are settable in both magnitude and sign. In this circuit the polarity of the offset applied to A2's negative input is

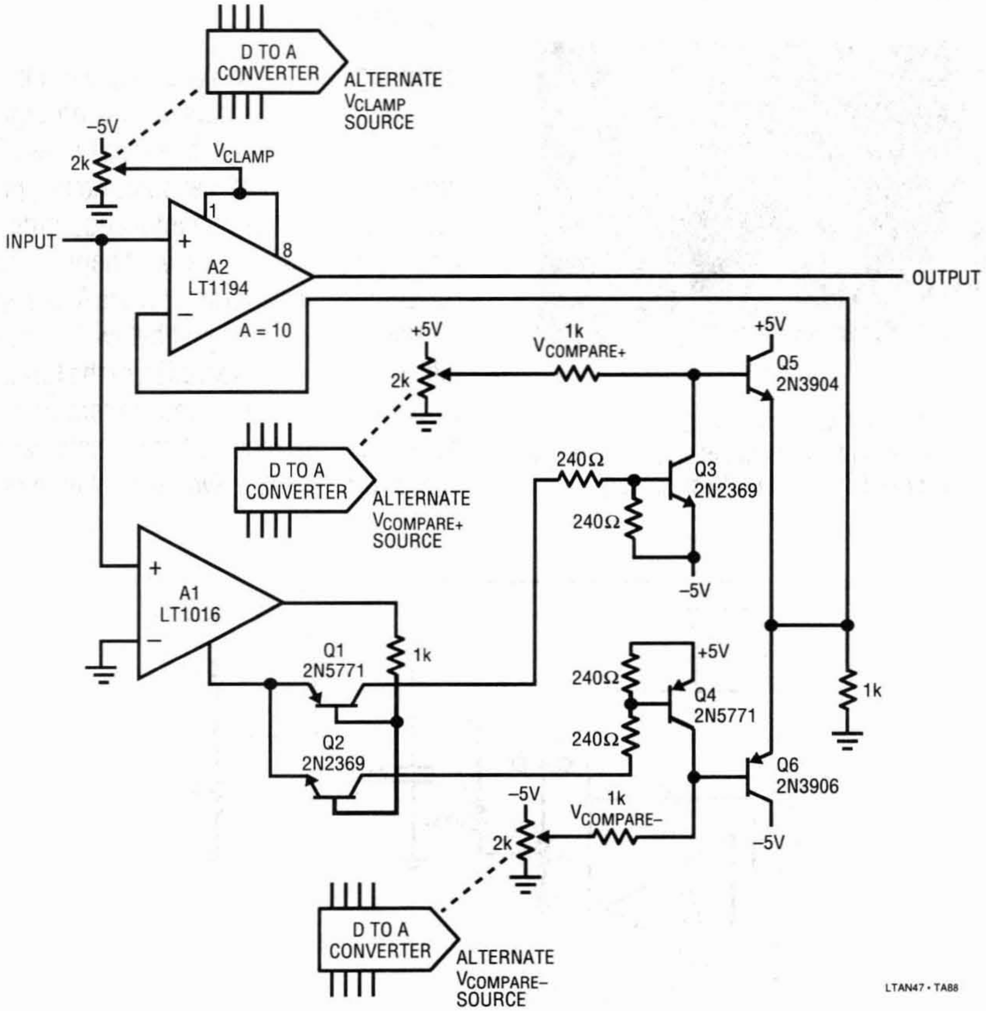
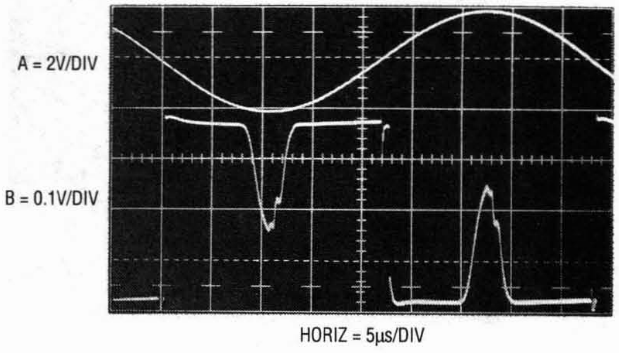

D TO A CONVERTER
ALTERNATE V_{CLAMP} SOURCE
–5V
2k
V_{CLAMP}
1
8
INPUT
+
A2
LT1194
–
A = 10
OUTPUT
+5V
2k
1k
$V_{COMPARE+}$
+5V
Q5
2N3904
D TO A CONVERTER
ALTERNATE $V_{COMPARE+}$ SOURCE
240Ω
240Ω
Q3
2N2369
–5V
+
A1
LT1016
–
Q1
2N5771
1k
240Ω
240Ω
+5V
Q4
2N5771
1k
Q2
2N2369
Q6
2N3906
–5V
1k
$V_{COMPARE–}$
2k
–5V
D TO A CONVERTER
ALTERNATE $V_{COMPARE–}$ SOURCE
LTAN47 • TA88

Figure 88. Differential Comparator Amplifier with Settable Automatic Limiting and Offset

determined by comparator A1's output state. A1 compares the circuit's input to ground, generating polarity information at its outputs. Level shifters Q1-Q3 and Q2-Q4 bias followers Q5 and Q6. Positive circuit inputs result in Q5 supplying the "$V_{COMPARE+}$" potential to A2, while negative inputs route "$V_{COMPARE-}$" to A2. This eliminates the previous circuit's manual polarity switch, permitting automatic selection of the differencing polarity and amplitude. Additionally, this circuit takes advantage of A2's input clamp feature. This feature (See LT1194 Data Sheet) limits the dynamic range of the input, clamping the amplifier's input operating range. Signals inside the clamp limit are processed normally, while signals outside the limit are precluded from influencing the amplifier. This combination of circuit controls allows very tightly defined windows on a waveform to be selected for accurate amplification without overload restrictions.

Figure 89 shows the circuit output for a sine input (Trace A) from the same function generator used to test the previous circuit. The V^+ and V^- compare voltages are set just below the sinewave peaks, with "V_{clamp}" programmed to restrict amplification to the peak's excursion. Trace B, the circuit's output, simultaneously shows amplitude detail of *both* sine peaks. The observed distortion is directly traceable to this generator's imperfect internal triangle waveform (see Figure 87), as well as its sine shaper characteristics.



LTAN47 • TA89

Figure 89. The Automatic Differential Comparator Amplifier Finds Triangle Wave and Switching Residuals (Trace B) in Trace A's Peaks

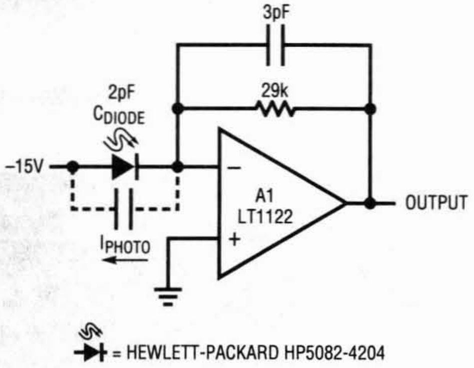
Photodiode Amplifier

Amplification of fast photodiode signals over a wide range of intensity is a common requirement. Figure 90's fast FET amplifier serves well, giving wideband operation with 5 decades of photocurrent. The photodiode is set up in the conventional manner. Photocurrent is fed directly to A1's summing point, causing A1's output to move to the level required to maintain virtual ground at the negative input. The –15V diode bias aids diode response. The table in the figure details circuit operating characteristics with the diode specified.

Some care in frequency compensating this configuration is required. The diode has about 2pF of parasitic capacitance, forming a significant lag at A1's summing point. If no feedback capacitor is used, high speed dynamics are poor. Figure 91 shows circuit response to a photo input (Trace A) with the indicated 3pF feedback capacitor removed. A1's output overshoots and saturates before finally ringing down to final value. In contrast, replacing the 3pf capacitor provides Figure 92's results. The same input pulse (Trace A, Figure 92) produces a cleanly damped output (Trace B). The capacitor imposes a 50% speed penalty (note faster horizontal scale for Figure 92). This is unavoidable because suppressing the parasitic ringing's relatively low frequency mandates significant roll-off.

Fast Photo Integrator

A related circuit to the photodiode amplifier is Figure 93's photo integrator. Here, the output represents the integral of the diode's photocurrent over some period of time. This



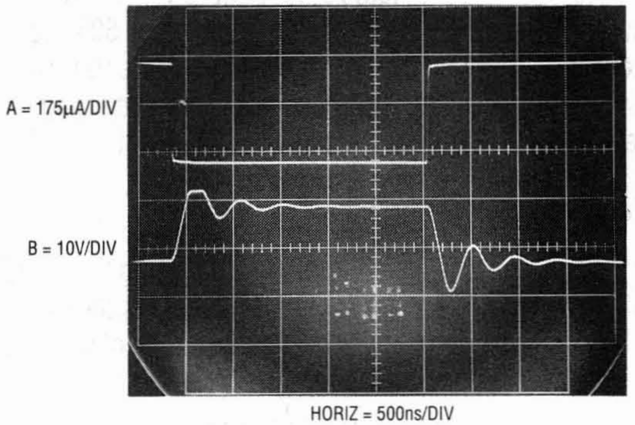
RESPONSE DATA

LIGHT (900nM)	DIODE CURRENT	CIRCUIT OUTPUT
1mW	350μA	10.0V
100μW	35μA	1V
10μW	3.5μA	0.1V
1μW	350nA	0.01V
100nW	35nA	0.001V

LTAN47 • TA90

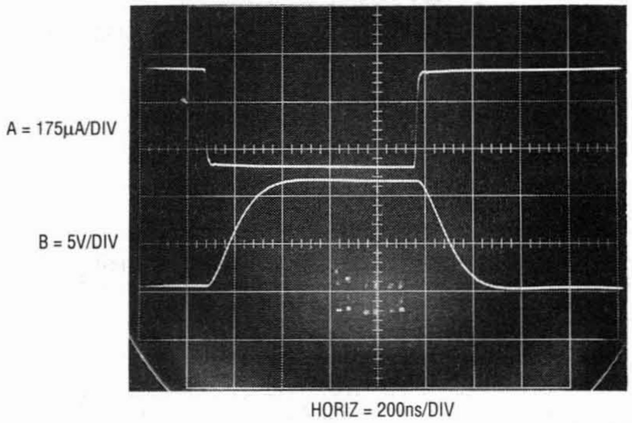
Figure 90. A Simple Photodiode Amplifier

circuit is particularly applicable in situations where the total energy in a light pulse (or pulses) must be measured. The circuit is a very fast integrator, with S1 used as a reset switch. S2, switched simultaneously with S1, compensates S1's charge injection error. With the control input (Trace A, Figure 94) low and no photocurrent, S1 is closed and A1 looks like a grounded follower. Under these conditions A1's output (Trace C) sits at 0V. When the control input goes high, A1 becomes an integrator as soon as S1 opens. Due to switch delay, this occurs about 150ns after the control input goes high. When S1 opens it delivers some parasitic charge to A1's summing point. S2 provides a compensatory charge based pulse at A1's positive terminal to cancel the effects of S1's charge error. This action shows up as a fast, small amplitude event in A1's output which settles rapidly back to 0V.



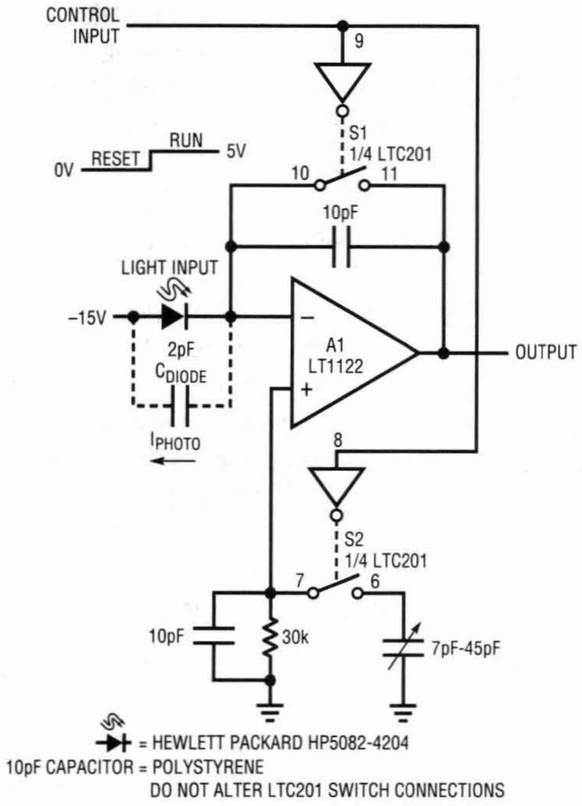
LTAN47 • TA91

Figure 91. Response of Figure 90 Without a Feedback Capacitor



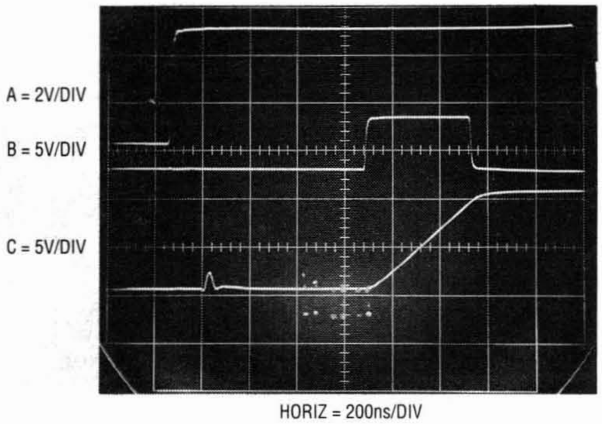
LTAN47 • TA92

Figure 92. Figure 90 Responding with a Feedback Capacitor


CONTROL INPUT
9
S1
1/4 LTC201
RUN
RESET
0V
5V
10
11
10pF
LIGHT INPUT
–15V
2pF
C_{DIODE}
I_{PHOTO}
A1
LT1122
OUTPUT
8
S2
1/4 LTC201
7
6
10pF
30k
7pF-45pF
= HEWLETT PACKARD HP5082-4204
10pF CAPACITOR = POLYSTYRENE
DO NOT ALTER LTC201 SWITCH CONNECTIONS

LTAN47 • TA93

Figure 93. A Very Fast Photo Integrator. S2 Compensates Reset Switch S1's Small Charge Injection



LTAN47 • TA94

Figure 94. The Photo Integrator Acquires (Trace C) an Input Light Pulse (Trace B) with the Control Line (Trace A) in the Run Mode. Charge Cancellation Action is Evident at Trace C's 400ns Point

At this point in time the integrator is ready to receive and record a photo pulse. When light falls on the photodiode (Trace B triggers a light pulse seen by the photodiode) A1 responds by integrating. In this case A1's output integrates rapidly until the light pulse ceases. A1's voltage after the light event is over is related to the total energy seen by the diode during the event. A monitoring A-D converter can acquire A1's output. In typical operation the control line returns low, resetting A1 until the next event is to be integrated.

With only 10pF of integration capacitor, the circuit has an output droop rate of about 0.2V/µs. This can be increased, although integration speed will suffer accordingly. Integration times of nanoseconds to milliseconds and photocurrents ranging from nanoamperes to hundreds of microamperes are accommodated by the circuit as shown. Thus, light intensities spanning microwatts to milliwatts over wide ranges of duration are practical inputs. The primary accuracy restrictions are A1's 75pA bias current, its 12V output swing and the effectiveness of the charge cancellation network. Typically, full-scale accuracy of several percent is achievable if the charge cancellation network is trimmed. To do this, assure that the diode sees no light while repetitively pulsing the control line. Adjust the trimmer capacitor for 0V output at A1 immediately after the disturbance associated with the S1-S2 switching settles.

Fiber Optic Receiver

A simple high speed fiber optic receiver appears in Figure 95. A1, a photocurrent-to-voltage converter similar to Figure 90, feeds comparator A2. A2 compares A1's output to a DC level established by the threshold adjust setting, producing a logic compatible output. Figure 96 shows typical waveforms. Trace A is a pulse associated with a photo input. Trace B is A1's response and Trace C is A2's output. The phase shift between the photo input and A2's output is due to A1's delay in reaching the threshold level. Reducing the threshold level will help, but moves operation closer to the noise floor. Additionally, the fixed threshold level cannot account for response changes in the emitter and detector diodes and fiber optic line over time and temperature.

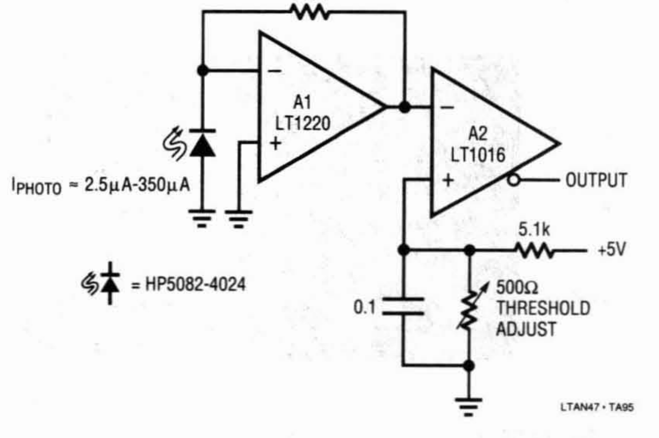


Figure 95. A Simple Fiber Optic Receiver

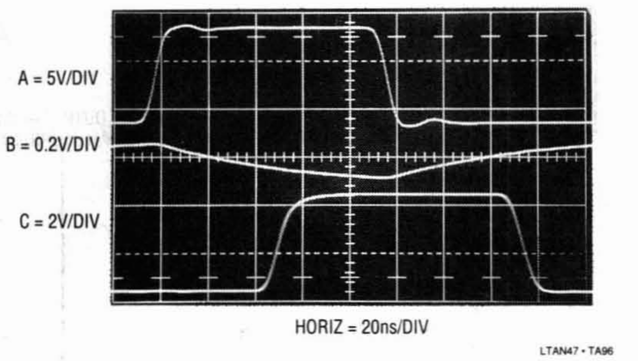


Figure 96. Waveforms for the Simple Fiber Optic Receiver. A1 (Trace B) Lags the Input (Trace A), but Output (Trace C) is Clean

40MHz Fiber Optic Receiver with Adaptive Trigger

Receiving high speed fiber optic data with wide input amplitude variations is not easy. The high speed data and uncertain intensity of the light level can cause erroneous results unless the receiver is carefully designed. Figure 97 addresses the previous circuit's limitations, offering significant performance advantages. This receiver will reliably condition fiber optic inputs of up to 40MHz with input amplitude varying by >40dB. Its digital output features an adaptive threshold trigger which accommodates varying signal intensities due to component aging and other causes. An analog output is also available to monitor the detector output. The optical signal is detected by the PIN photodiode and amplified by A1. A second stage, A2, gives further amplification. The output of this stage biases a 2-way peak detector (Q1-Q4). The maximum peak is stored in Q2's emitter capacitor, while the minimum excursion is retained in Q4's emitter capacitor. The DC value of A2's output signal's mid-point appears at the junction of the 500pF capacitor and the 22MΩ units. This point will always sit midway between the signal's excursions, re-

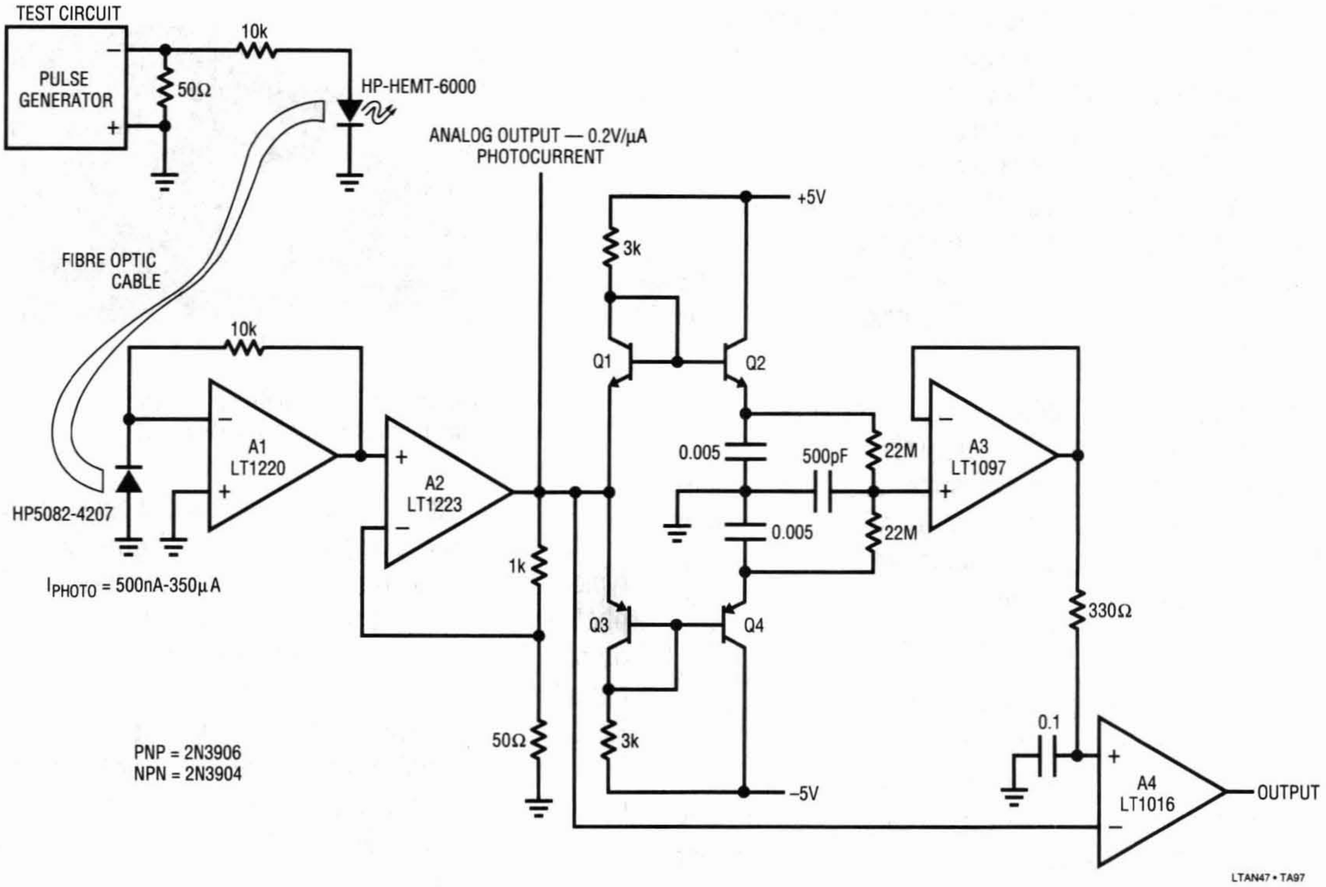

TEST CIRCUIT
PULSE GENERATOR
10k
50Ω
HP-HEMT-6000
ANALOG OUTPUT — 0.2V/μA PHOTOCURRENT
+5V
3k
FIBRE OPTIC CABLE
10k
Q1
Q2
A1 LT1220
A2 LT1223
0.005
500pF
22M
A3 LT1097
HP5082-4207
0.005
22M
1k
I_{PHOTO} = 500nA-350μA
Q3
Q4
330Ω
PNP = 2N3906
NPN = 2N3904
50Ω
3k
0.1
–5V
A4 LT1016
OUTPUT
LTAN47 • TA97

Figure 97. Adaptively Triggered 40MHz Fiber Optic Receiver is Immune to Shifts in Operating Point

gardless of absolute amplitude. This signal-adaptive voltage is buffered by the low bias LT1097 to set the trigger voltage at the LT1016's positive input. The LT1016's negative input is biased directly from A2's output. Figure 98 shows the results using the test circuit indicated in Figure 97. The pulse generator's output is Trace A, while A2's output (analog output monitor) appears in Trace B. The LT1016 output is Trace C. The waveforms were recorded with a 5μA photocurrent at about 20MHz. Note that A4's output transitions correspond with the midpoint of A2's output (plus A4's 10ns propagation delay) in accordance with the adaptive trigger's operation.

50MHz High Accuracy Analog Multiplier

Although highly accurate, very wideband analog multipliers are available, their output takes a differential form. These differential outputs, which have substantial common mode content, are frequently inconvenient to work with. RF transformers can be used to single end the outputs, but DC and low frequency information is lost. Figure 99 uses the LT1193 differential amplifier to accomplish the differential-to-single ended transition. The AD834 is set up in the recommended configuration (see Analog Devices AD834 Data Sheet, Reference 26). The LT1193 takes the differential signal from the AD834's 50Ω terminated output and provides a single ended output. The gain of two yields a ±1V output at full-scale.

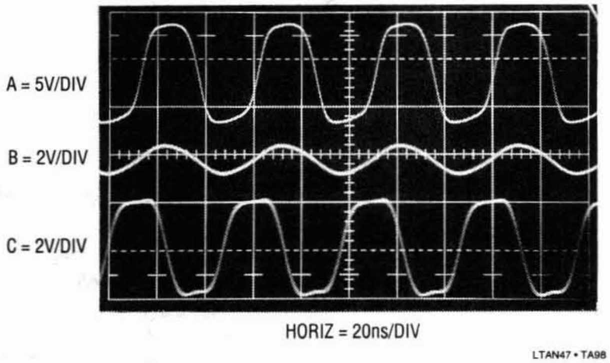


Figure 98. Adaptively Triggered Fiber Optic Receiver's Waveforms at 20MHz with 5μA Diode Current

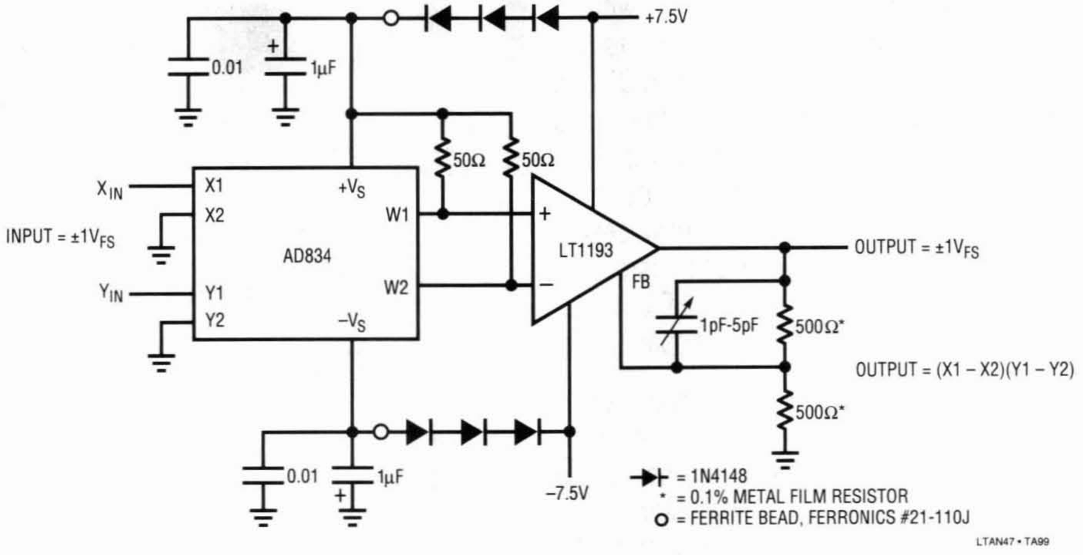


Figure 99. Analog Multiplier with 2% Accuracy Over DC to 50MHz Has a Single Ended Output

The AD834 outputs come out riding on a common-mode level very close to the devices positive supply. This common-mode level falls outside the LT1193's input common-mode range. The diodes in the 7.5V supply rails drop the supply at the AD834, biasing its outputs within the LT1193's input range. This scheme avoids the attenuation and matching problems presented by placing a level shift between the multiplier and amplifier. The ferrite beads combine with the diode's impedance to ensure adequate bypassing for the multiplier, a very wideband device.

Performance for this circuit is quite impressive. Error remains within 2% over DC-50MHz, with feedthrough below –50dB. Trimming the circuit involves adjusting the variable capacitor at the amplifier for minimal output square wave peaking. Figure 100 shows performance when a 20MHz sine input is multiplied by Trace A's waveform. The output (Trace B) is a singularly clean instantaneous representation of the X•Y input products, with strict fidelity to their components.

Power Booster Stage

Occasionally, it is necessary to supply larger output currents than an amplifier is capable of delivering. The power gain stage, sometimes called a booster, is usually placed within the monolithic amplifier's feedback loop, preserving the IC's low drift and stable gain characteristics. Because the output stage resides in the amplifier's feedback path, loop stability is a concern. This is particularly the case with high speed amplifiers. The output stage's gain and AC characteristics must be considered if good dynamic performance is to be achieved. Overall circuit phase shift, frequency response and dynamic load handling capabilities are issues that cannot be ignored when designing a power gain stage for a monolithic amplifier. The output stage's added gain and phase shift can cause poor AC response or outright oscillation. Judicious application of frequency compensation methods is needed for good results (see Appendix C, "The Oscillation Problem – Frequency Compensation Without Tears", for discussion and details on compensation methods).

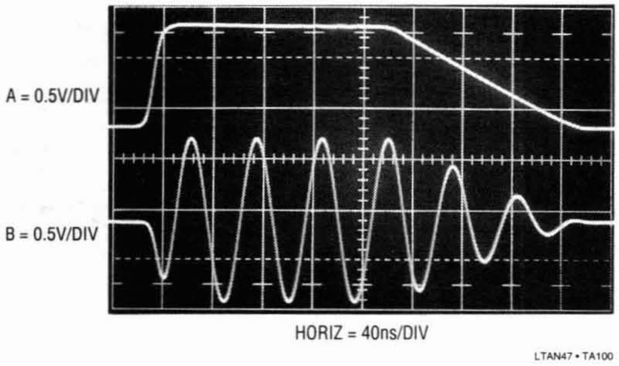


Figure 100. The Multiplier Produces a Modulated Sine Output (Trace B) in Accordance with Trace A's Envelope

Figure 101 shows a 200mA power booster used with an LT1220 amplifier. Complementary emitter followers Q1-Q5 provide current gain for positive signals, with Q2 and Q6 handling negative excursions. Q3 and Q4 are V_{BE} based current limits, coming on and robbing drive from the appropriate output transistor when current exceeds about 300mA. The diodes prevent Q1 and Q2 from seeing reverse V_{BE} during current limit. The 100Ω resistor and ferrite beads prevent the low impedance amplifier output from causing oscillation in Q1 and Q2 (see Appendix C).

To be effective, the booster must be exceptionally fast. A slow design will obviate the AC performance of the amplifier controlling it, or in the worst case, cause oscillation (again, see Appendix C). Figure 102 shows booster performance with the LT1220 removed from the circuit. The input pulse (Trace A) is applied to the booster input, with the output (Trace B) taken at the indicated spot. Evaluation of the photograph shows that booster rise and fall times are limited by the input pulse generator. Additionally, delay is in the 1ns range. This kind of speed makes the circuit a good candidate for acceptable AC performance within a fast amplifier's loop.

Figure 103 shows pulse response with the LT1220 installed in the circuit with a 50Ω load. The booster's high speed contributes negligible delay and overall response is clean and predictable. The local 3pF roll-off at the LT1220 optimizes response, but is not absolutely necessary in this circuit. The input (Trace A) produces a nicely shaped LT1220 slew-limited output (Trace B).

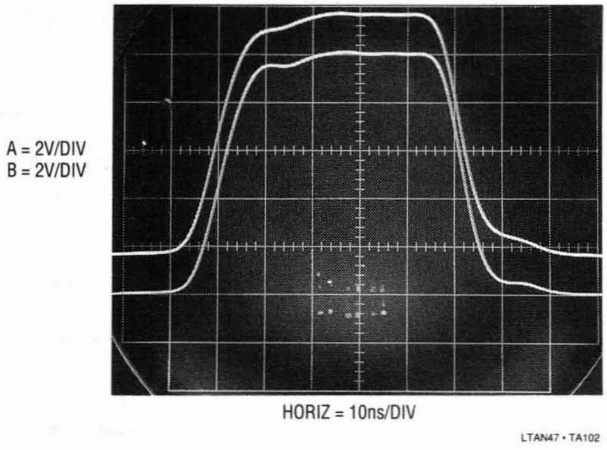


Figure 102. Response of Figure 101's Booster Stage

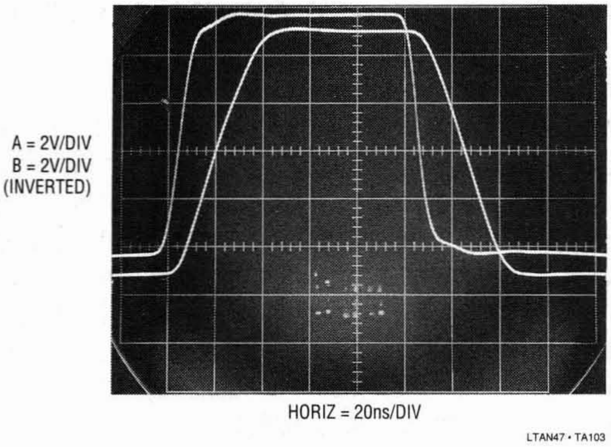


Figure 103. The Booster's Response When Inside an Amplifier's Loop

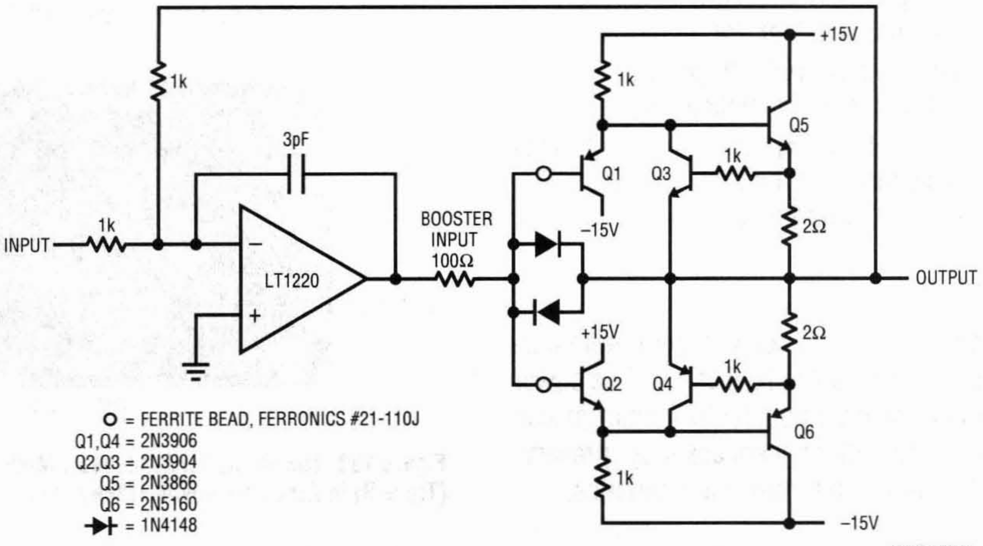


Figure 101. A 200mA Output Wideband Booster Stage

High Power Booster Stage

In theory, higher power booster stages should be achievable by utilizing bigger devices. This is partly the case, but lack of availability of wideband PNP power transistors is an issue. Figure 104 shows a way around this problem.

The circuit is essentially a 1A output version of Figure 101, with several differences. In the positive signal path output transistor Q4 is an RF power type, driven by Darlington connected Q3. The diode in Q1's emitter compensates the additional V_{BE} introduced by Q3, preventing crossover distortion.

The negative signal path substitutes the Q5-Q6 connection to simulate a fast PNP power transistor. Although this configuration acts like a fast PNP follower, it has voltage gain and tends to oscillate. The local 2pF feedback capacitor suppresses these parasitic oscillations and the composite transistor is stable.

This circuit also includes a feedback capacitor trim to optimize AC response. This difference from the previous circuit is necessitated by this circuit's slightly slower characteristics and much heavier loading. Current limit operation and other characteristics are similar to the lower power circuit.

Figure 105 shows waveforms for a 10V negative input step (Trace A) with a 10Ω load. The amplifier responds (Trace B), driving the booster to the voltage required to close the loop. For this positive step, the amplifier provides about 1.5V overdrive to overcome Q3 and Q4's V_{BE} drops. The booster output, lagging by a few nanoseconds (Trace C), drives the load cleanly, with only minor peaking. This peaking may be minimized with the feedback capacitance trimmer.

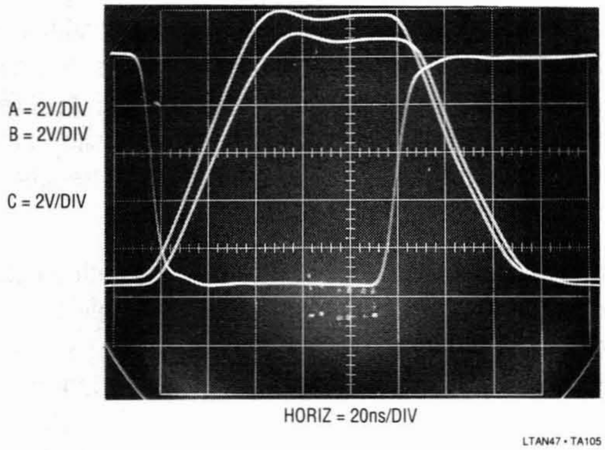


Figure 105. The Boosted Op Amp Drives a 1A Load to 10V in 50ns

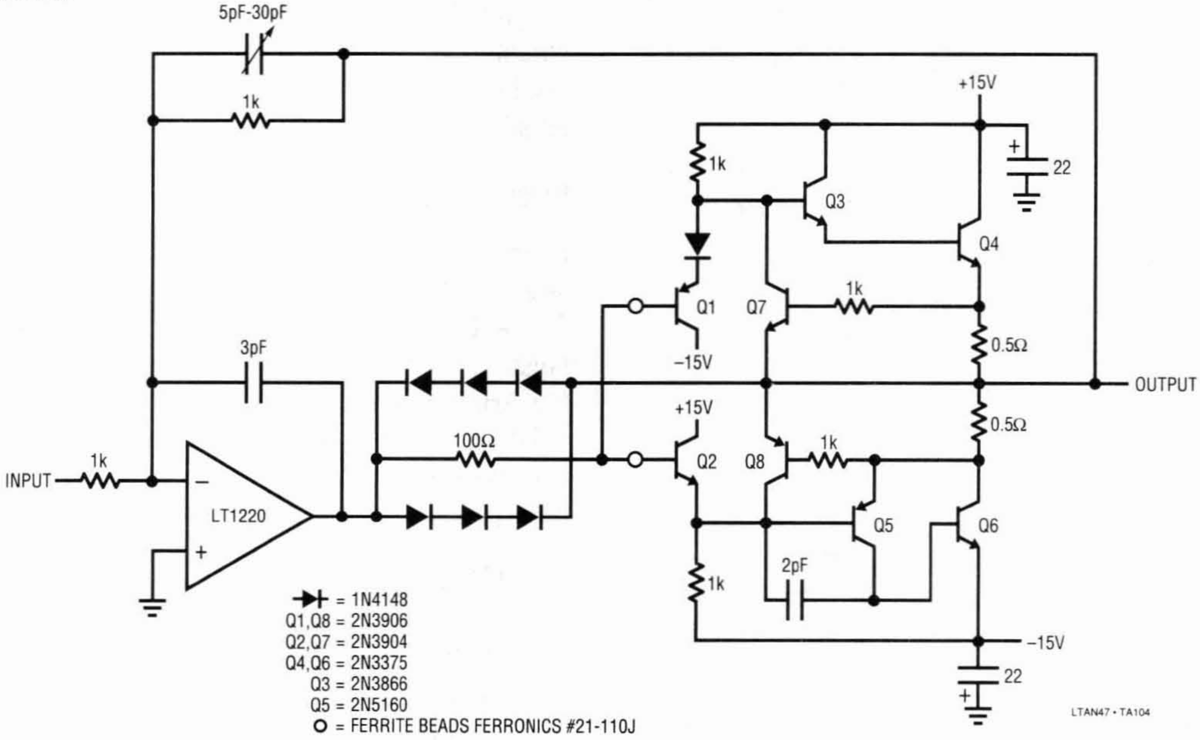
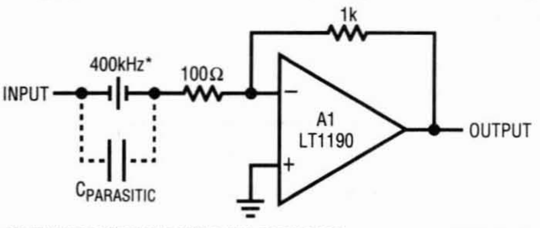

5pF-30pF
1k
+15V
22
1k
Q3
Q4
Q1
Q7
1k
0.5Ω
–15V
3pF
OUTPUT
+15V
100Ω
Q2
Q8
1k
0.5Ω
INPUT
1k
LT1220
Q5
Q6
2pF
1k
–15V
22
= 1N4148
Q1,Q8 = 2N3906
Q2,Q7 = 2N3904
Q4,Q6 = 2N3375
Q3 = 2N3866
Q5 = 2N5160
○ = FERRITE BEADS FERRONICS #21-110J
LTAN47 • TA104

Figure 104. Fast, 1A Booster Stage

Ceramic Bandpass Filters

Figure 106 is a highly selective bandpass filter using a resonant ceramic element and a single amplifier. The ceramic element nominally looks like a high impedance off its resonant frequency, in this case 400kHz. For off resonance inputs, A1 acts like a grounded follower, producing no output. At resonance, the ceramic element has a low impedance and A1 responds as an inverter with gain. The 100Ω resistor isolates the ceramic element's capacitance from A1's summing point. This capacitance is quite substantial and limits the circuits out of band rejection capability. Figure 107 shows this. This plot shows very steep rejection, with A1's output down almost 20dB at 300kHz and 40dB at 425kHz. The device's stray parasitic capacitance causes the gentle rise in output at higher frequencies and also sets the –20dB floor at 300kHz.

Figure 108 partially corrects this problem with a nulling technique. This circuit is similar to the previous one, except that a portion of the input is fed to A1's positive input. The RC network at this input is scaled to look like the ceramic resonator's off null impedance. As such, A1's inputs see similar signals for out of band components, resulting in attenuation via A1's common-mode rejection. At resonance, the added RC network appears as a much higher impedance than the ceramic element and filter response is similar to Figure 106's circuit. Figure 107 shows that this circuit has much better out of band rejection than Figure 106. The high frequency roll-off is smooth, and over 20dB deeper than Figure 106 at 475kHz. The low frequency side of resonance has similar characteristics at 375kHz and below.



*CERAMIC RESONATOR MURATA-ERIE CORP

Figure 106. A Piezo-Ceramic Based Filter

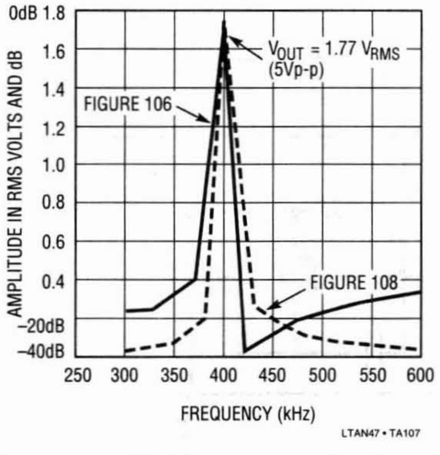
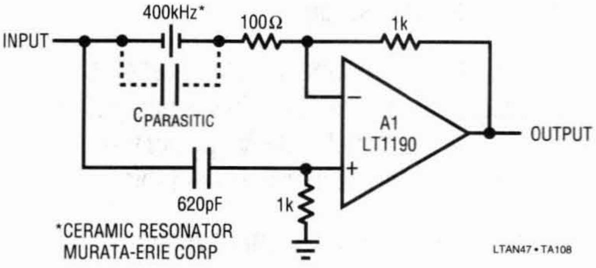


Figure 107. Response of Both Piezo-Ceramic Filters. Differential Network's Activity is Evident in Figure 108's Performance



*CERAMIC RESONATOR MURATA-ERIE CORP

Figure 108. Differential Network Nulls Parasitic Capacitance of Ceramic Element

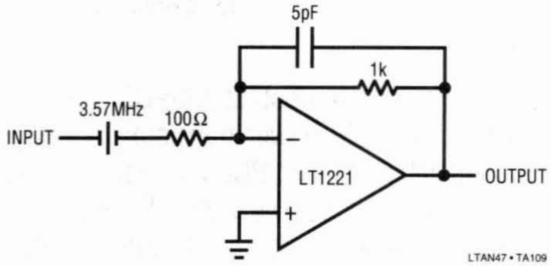


Figure 109. Crystal Filter

Crystal Filter

Quartz crystals can also be used to make even higher selectivity filters at higher frequencies. Figure 109 replaces Figure 106's ceramic element with a 3.57MHz quartz crystal. Figure 110 shows almost 30dB attenuation only a few kHz on either side of resonance! The differential nulling technique used with the ceramic elements is less effective with quartz crystals. Crystals have significantly lower parasitic terms, making the cancellation less effective.

APPLICATIONS SECTION II - OSCILLATORS

Sine Wave Output Quartz Stabilized Oscillator

Figure 111 places a crystal within the amplifier's feedback path, creating an oscillator. With the crystal removed, the

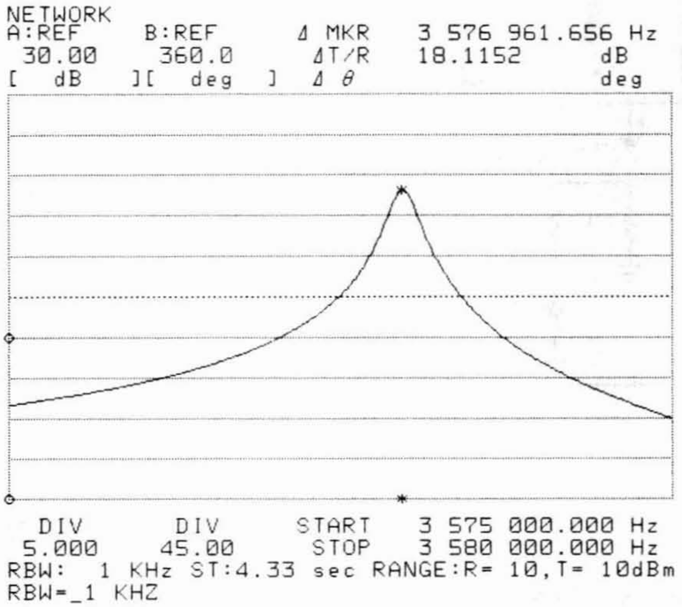


Figure 110. The Crystal Filter's Response

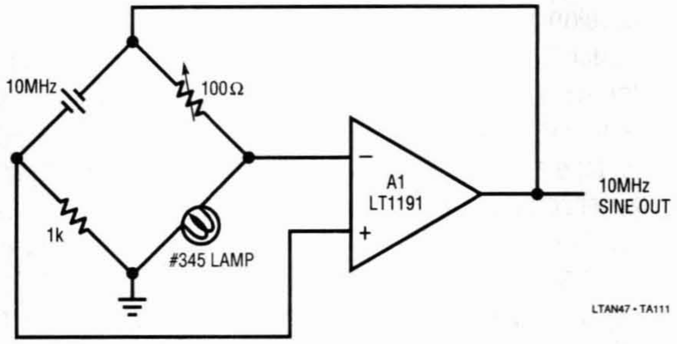


Figure 111. 10MHz Quartz Stabilized Sine Wave Oscillator

circuit is a familiar non-inverting amplifier with a grounded input. Gain is set by the impedance ratio of the elements associated with A1's negative input. Inserting the crystal closes a positive feedback path at the crystal's resonant frequency and oscillations commence.

In any oscillator it is necessary to control the gain as well as the phase shift at the frequency of interest. If gain is too low, oscillation will not occur. Conversely, too much gain produces saturation limiting. Here, gain control comes from the positive temperature coefficient of the lamp at A1's negative input. When power is applied, the lamp is at a low resistance value, gain is high and oscillation amplitude builds. As amplitude builds, lamp current increases, heating occurs, and the lamp's resistance goes up. This causes a reduction in amplifier gain and the circuit finds a stable operating point. This circuit's sine wave output has all the stability advantages associated with quartz crystals. Although shown at 10MHz, it works well with a wide variety of crystal types over a 100kHz-20MHz range. The use of the lamp to control amplifier gain is a classic technique, first described by Meacham in 1938.[12] Electronic gain control, while more complex, offers more precise control of amplitude.

Sine Wave Output Quartz Stabilized Oscillator with Electronic Gain Control

Figure 112's quartz stabilized oscillator replaces the lamp with an electronic amplitude stabilization loop. A2 compares the A1 oscillator's positive output peaks with a DC reference. The diode in the DC reference path temperature compensates the rectifier diode. A2 biases Q1, controlling its channel resistance. This influences loop gain, which is reflected in oscillator output amplitude. Loop closure around A1 occurs, stabilizing oscillator amplitude. The 1μF capacitor compensates the gain control loop.

The DC reference network is set up to provide optimum temperature compensation for the rectifier diode, which sees a 2Vp-p 20MHz waveform out of A1. A1's small amplitude swing minimizes distortion introduced by channel resistance modulation in Q1. To use this circuit, adjust the 50Ω trimmer until 2Vp-p oscillations appear at A1's output.

Figure 113 is a spectrum analysis of the oscillator's output. The fundamental sits at 20MHz, with the second harmonic 47dB down at 40MHz. A third harmonic, 50dB down, occurs at 60MHz. Resolution bandwidth for the spectrum analysis is 1kHz.

DC Tuned 1MHz-10MHz Wien Bridge Oscillator

In Figure 114 the quartz crystal is replaced with a Wien network at A2's positive input. A1 controls Q1 to amplitude stabilize A2's oscillations in identical fashion to the previous figure. Although the Wien network is not nearly as stable as a quartz crystal, it has the advantage of a variable frequency output. Normally, this is facilitated by varying either R, C, or both. Usually, manually adjustable elements such as dual potentiometers and two section variable

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Note 12: See Reference 20, as well as References 19 and 21 for supplemental information.

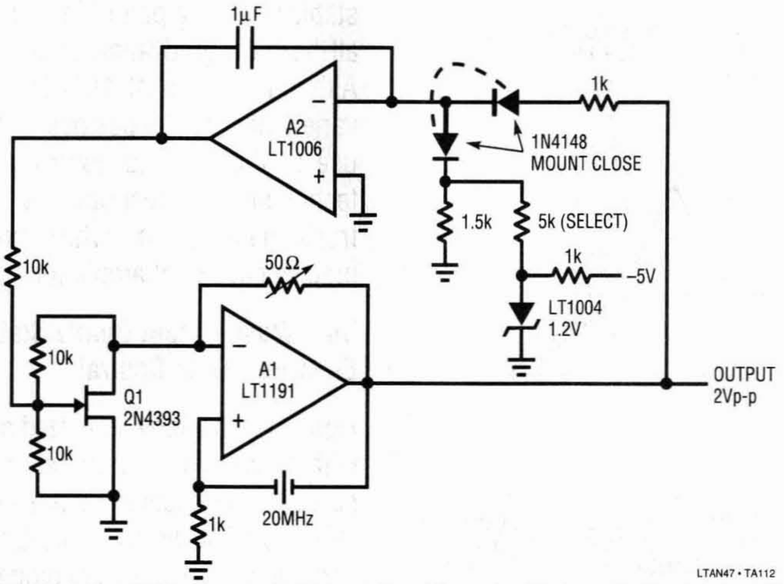
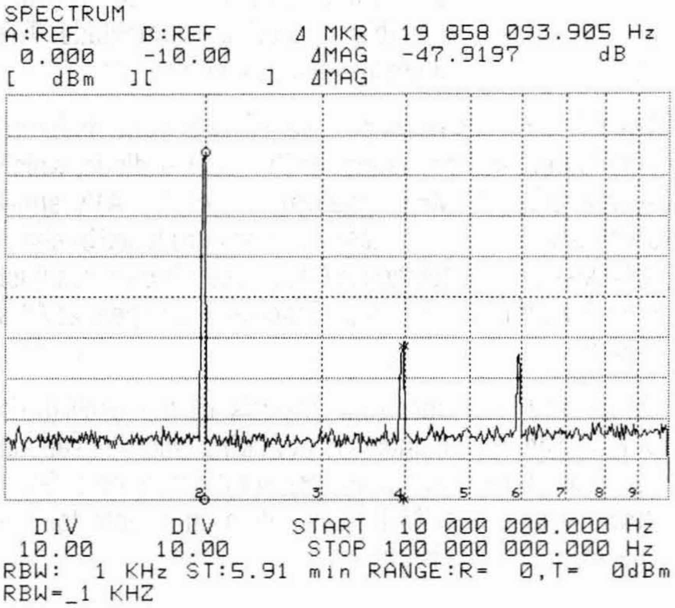


Figure 112. 20MHz Quartz Stabilized Sine Wave Oscillator with Electronic AGC



```
SPECTRUM
A:REF       B:REF        Δ MKR   19 858 093.905 Hz
 0.000      -10.00      ΔMAG    -47.9197      dB
[   dBm  ][          ]   ΔMAG
```

```
 DIV         DIV       START  10 000 000.000 Hz
10.00       10.00       STOP 100 000 000.000 Hz
RBW:   1 KHz ST:5.91 min RANGE:R=   0,T=   0dBm
RBW=_1 KHZ
```

Figure 113. Spectrum Analysis of the 20MHz Quartz Oscillator. Harmonic Content is at Least 47dB Down

capacitors are used. Here, the Wien network resistors are fixed at 360Ω, while the capacitive elements are realized with varactor diodes. The varactor diodes voltage-variable-capacitance characteristic allows DC tuning of the oscillator. DC inputs of 0V-10V to the varactors result in a 1MHz to 10MHz shift in oscillation frequency. The 0.1µF capacitor blocks the DC bias from A2's positive input while permitting the Wien network to function normally. A2's 2Vp-p output minimizes the varactor's junction effects, aiding distortion.

This ±5V powered circuit requires voltage step-up to develop adequate varactor drive. A3 and the LT1172 switching regulator form a simple voltage step-up regulator. A3 controls the LT1172 to produce the output voltage required to close a loop at A3's negative input. L1's high voltage inductive flyback events, rectified by the diode and zener connected Q2, are stored in the 22µF output capacitor. The 7.5k-2.5k divider provides a sample of the output's value to A3's negative input, closing the loop. The 0.1µF capacitor stabilizes this feedback action. Q2's zener drop allows the circuit to produce controlled outputs all the way down to 0V. This arrangement permits a 0V-2.5V input at A3 to produce a corresponding 0V-10V varactor bias. Figure 115, a spectral plot of the circuit running at 7.6MHz, shows the second harmonic down 35dB, with the third harmonic down almost 60dB. Resolution bandwidth is 3kHz.

Complete AM Radio Station

A complete microphone-to-antenna AM radio station appears in Figure 116.[13] The carrier is generated by A1, set up as a quartz stabilized oscillator similar to the one described in Figure 111. A1's output feeds A2, functioning as a modulated RF power output stage. A2's input signal range is restricted by the bias applied to offset pins 1 and

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[13] **Note 13:** The construction and operation of this apparatus may require Federal Communications Commission review and/or licensing. See Appendix G for FCC licensing and application information.

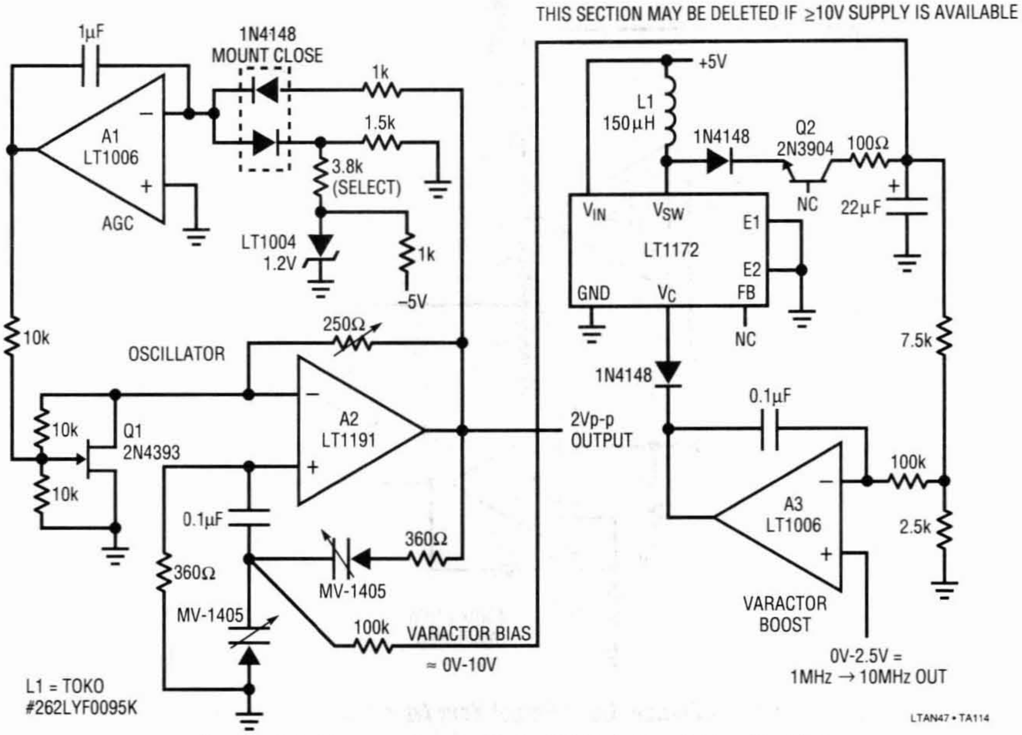
THIS SECTION MAY BE DELETED IF ≥10V SUPPLY IS AVAILABLE
1μF
1N4148
MOUNT CLOSE
1k
1.5k
A1
LT1006
AGC
3.8k
(SELECT)
LT1004
1.2V
1k
–5V
250Ω
10k
OSCILLATOR
10k
Q1
2N4393
10k
A2
LT1191
0.1μF
360Ω
360Ω
MV-1405
MV-1405
100k
VARACTOR BIAS
≈ 0V-10V
L1 = TOKO
#262LYF0095K
+5V
L1
150μH
1N4148
Q2
2N3904
100Ω
22μF
V_IN
V_SW
E1
LT1172
E2
GND
V_C
FB
NC
NC
1N4148
7.5k
0.1μF
2Vp-p
OUTPUT
100k
A3
LT1006
2.5k
VARACTOR
BOOST
0V-2.5V =
1MHz → 10MHz OUT
LTAN47 • TA114

Figure 114. Varactor Tuned 1MHz-10MHz Wien Bridge Oscillator

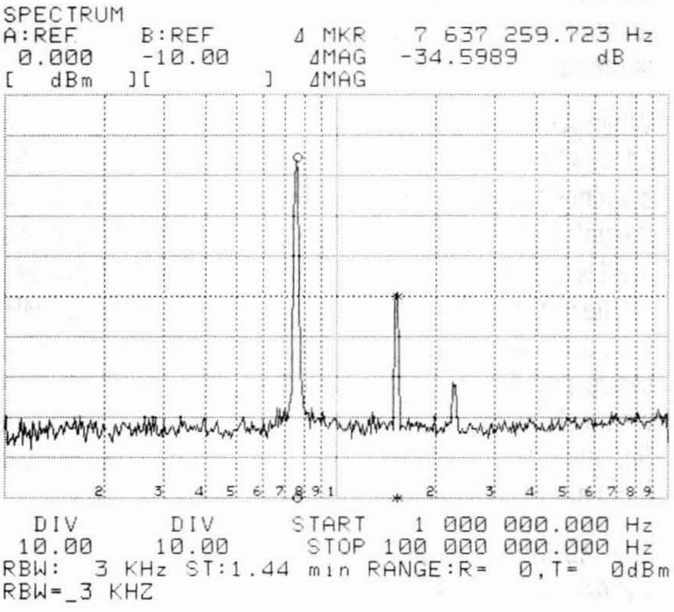

Figure 115. Spectrum Analysis for the Varactor Tuned Wien Bridge. Harmonics are at Least 34dB Down From Fundamental

8 (see LT1194 data sheet for details). A3, a microphone amplifier, supplies bias to these pins, resulting in an amplitude modulated RF carrier at A2's output. The DC term summed with the microphone biases A3's output to the appropriate level for good quality modulation characteristics. Calibration of this circuit involves trimming the 100Ω potentiometer in the oscillator for a stable 1Vp-p 1MHz A1 output.[14]

Figure 117 shows typical AM carrier output at the antenna. In this case the modulation is supplied by Mr. Chuck Berry, singing "Johnny Be Goode".

APPLICATIONS SECTION III - DATA CONVERSION

1Hz-1MHz Voltage-Controlled Sine Wave Oscillator

The oscillators presented to this point have limited frequency tuning range. Although Figure 118 is not a true oscillator, it produces a synthesized sine wave output over a wide dynamic range. Many applications such as audio, shaker table driving and automatic test equipment require voltage-controlled oscillators (VCO) with a sine wave output. This circuit meets this need, spanning a 1Hz-1MHz range (120dB or 6 decades) for a 0V to 10V input. It maintains 0.25% frequency linearity and 0.40% distortion specifications.[15] To understand the circuit, assume Q5 is

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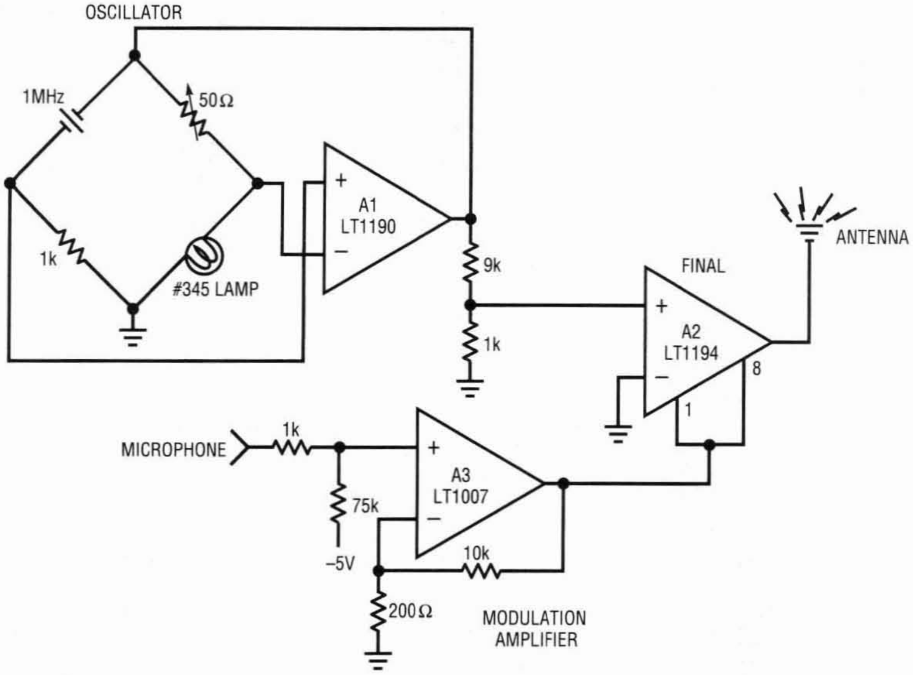
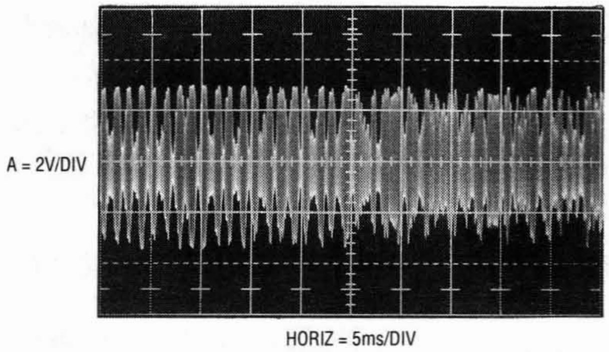
Note 14: Operating frequency subject to FCC approval and assignment. See Footnote 13 and Appendix G.

Note 15: Seasoned readers of LTC literature, a hardened corps, may recognize this and other circuits in this publication as updated versions of previous LTC applications. The partial repetition is justified based on improved specifications and/or simplification of the original circuit.



LTAN47 • TA116

Figure 116. A Complete AM Radio Station. Don't Forget Your Advertisers and FCC License (See Appendix G)



LTAN47 • TA117

Figure 117. Chuck Berry Lays a Little Modulation on the 1MHz Carrier

on and its collector (Trace A, Figure 119) is at –15V, cutting off Q1. The positive input voltage is inverted by A3, which biases the summing node of integrator A1 through the 3.6k resistor and the self-biased FETs. A current, –I, is pulled from the summing point. A2, a precision op amp, DC stabilizes A1. A1's output (Trace B, Figure 119) integrates positive until C1's input (Trace C) crosses 0V. When this happens, C1's inverting output goes negative, the Q4-Q5 level shifter turns off, and Q5's collector goes to +15V. This allows Q1 to come on. The resistors in Q1's path are scaled to produce a current, +2I, exactly twice the absolute magnitude of the current, –I, being removed from the summing node. As a result, the net current into the junction becomes +I and A1 integrates negatively at the same rate as its positive excursion.

When A1 integrates far enough in the negative direction, C1's "+" input crosses zero and its outputs reverse. This switches the Q4-Q5 level shifter's state. Q1 goes off and the entire cycle repeats. The result is a triangle waveform at A1's output. The frequency of this triangle is dependent on the circuit's input voltage and varies from 1Hz to 1MHz with a 0V-10V input. The LT1009 diode bridge and the series-parallel diodes provide a stable bipolar reference which always opposes the sign of A1's output ramp. The Schottky diodes bound C1's "+" input, assuring it clean recovery from overdrive.

The AD639 trigonometric function generator, biased via A4, converts A1's triangle output into a sine wave (Trace D).

The AD639 must be supplied with a triangle wave which does not vary in amplitude or output distortion will result. At higher frequencies, delays in the A1 integrator switching loop result in late turn on and turn off of Q1. If these delays are not minimized, triangle amplitude will increase with frequency, causing distortion level to also increase with frequency. The total delay generated by the LT1016,

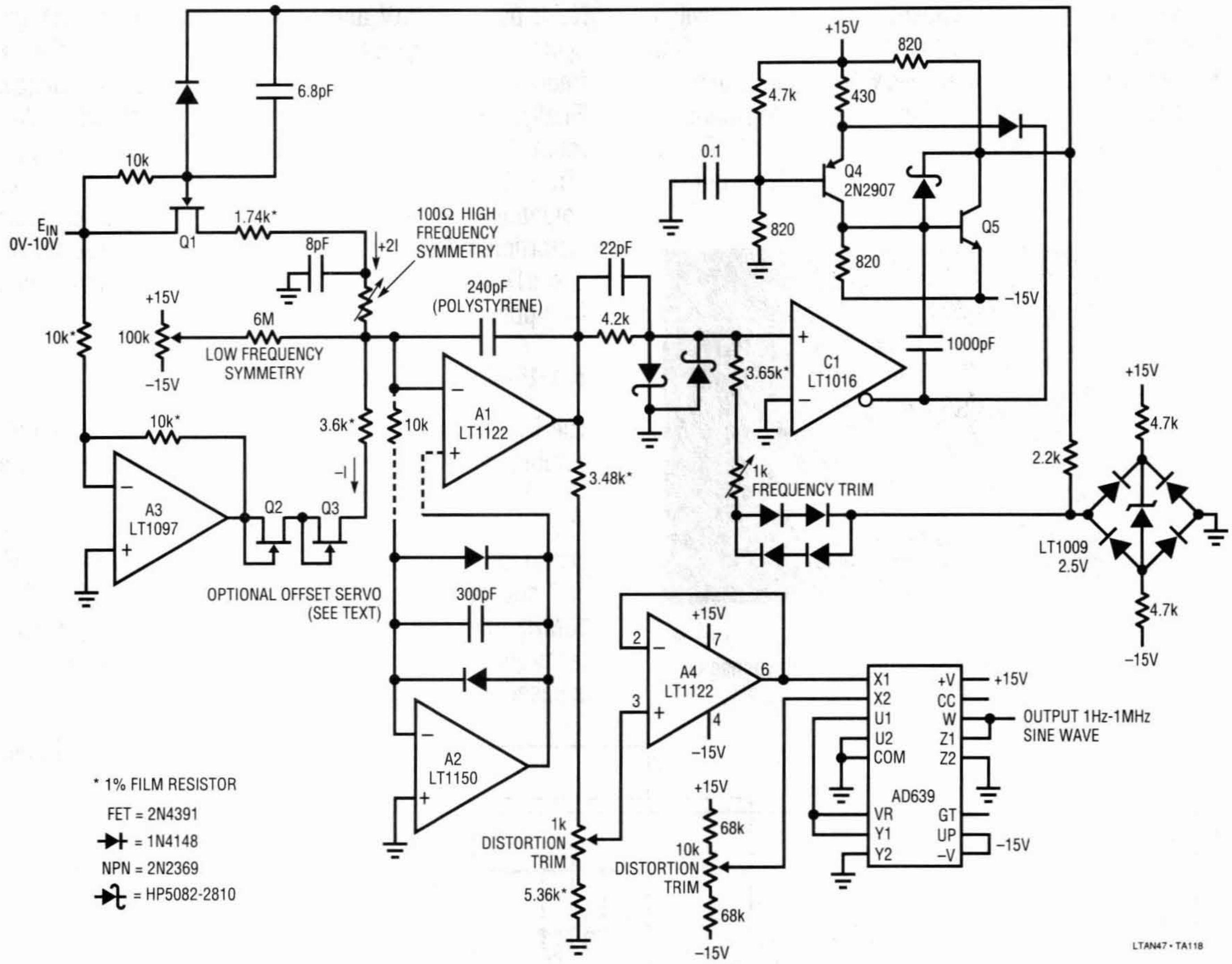

6.8pF
10k
EIN
0V-10V
Q1
1.74k*
8pF
+2I
100Ω HIGH FREQUENCY SYMMETRY
240pF (POLYSTYRENE)
22pF
4.2k
+15V
6M
10k*
100k
LOW FREQUENCY SYMMETRY
–15V
10k*
3.6k*
10k
A1 LT1122
3.48k*
–I
A3 LT1097
Q2
Q3
OPTIONAL OFFSET SERVO (SEE TEXT)
300pF
A2 LT1150
1k DISTORTION TRIM
5.36k*
+15V
820
4.7k
430
0.1
Q4 2N2907
Q5
820
820
–15V
C1 LT1016
3.65k*
1000pF
1k FREQUENCY TRIM
2.2k
+15V
4.7k
LT1009 2.5V
4.7k
–15V
A4 LT1122
2
3
6
7
4
+15V
–15V
X1
X2
U1
U2
COM
AD639
VR
Y1
Y2
+V
CC
W
Z1
Z2
GT
UP
–V
+15V
OUTPUT 1Hz-1MHz SINE WAVE
–15V
+15V
68k
10k DISTORTION TRIM
68k
–15V
* 1% FILM RESISTOR
FET = 2N4391
= 1N4148
NPN = 2N2369
= HP5082-2810
LTAN47 • TA118

Figure 118. 1Hz-1MHz Sine Wave Output VCO Has 0.25% Linearity and 0.4% Distortion

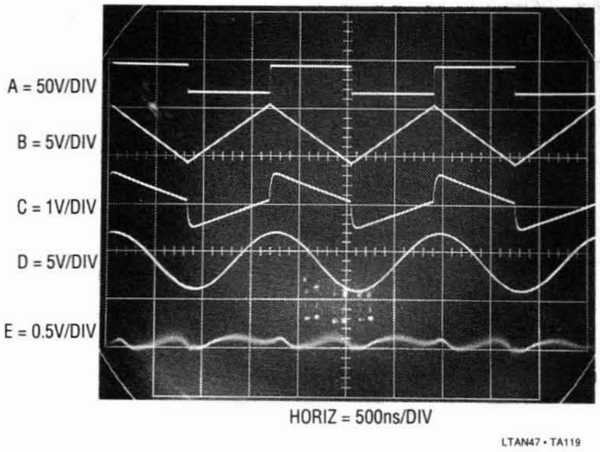


Figure 119. Sine Wave VCO Waveforms

the Q4-Q5 level shifter, and Q1 is 14ns. This small delay, combined with the 22pF feedforward network at the LT1016's input, keeps distortion to just 0.40% over the entire 1MHz range. At 100kHz, distortion is typically inside 0.2%. The effects of gate-source charge transfer, which happens whenever Q1 switches, are minimized by the 8pF unit in Q1's source line. Without this capacitor, a sharp spike would occur at the triangle peaks, increasing distortion. The Q2-Q3 FETs compensate the temperature-dependent on-resistance of Q1, keeping the +2I/–I relationship constant with temperature.

This circuit features extremely fast response to input changes, something most sine wave circuits cannot do.

Figure 120 shows what happens when the input switches between two levels (Trace A). A1's triangle output (Trace B) shifts frequency immediately, with no glitching or poor dynamics. The sine output (Trace C), reflecting this action, is similarly clean. To adjust this circuit, put in 10.00V and trim the 100Ω pot for a symmetrical triangle output at A1.

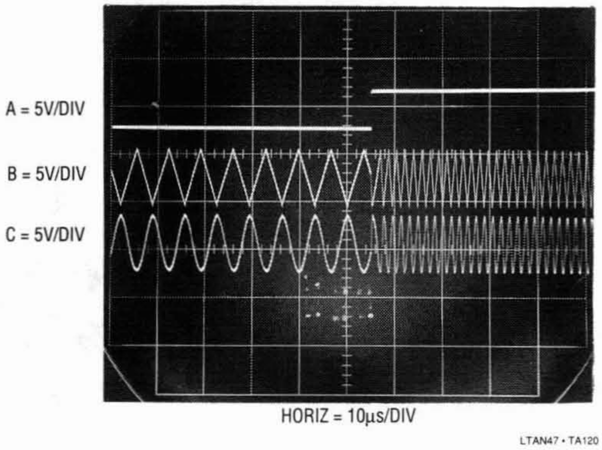


Figure 120. Sine Wave Output VCO Step Response is Quick and Clean

Next, put in 100μV and trim the 100k pot for triangle symmetry. Then, put in 10.00V again and trim the 1k frequency trim adjustment for a 1MHz output frequency. Finally, adjust the distortion trim potentiometers for minimum distortion as measured on a distortion analyzer (Trace E, Figure 119). Slight readjustment of the other potentiometers may be required to get lowest possible distortion. If operation below 100Hz is not required, the A2 based DC stabilization stage may be deleted. If this is done, A1's positive input should be grounded.

1Hz-10MHz V → F Converter

The LT1016 and the LT1122 high speed FET amplifier combine to form a high speed V → F converter in Figure 121. A variety of circuit techniques are used to achieve a 1Hz to 10MHz output. Overrange to 12MHz (V_{IN} = 12) is provided. This circuit has a wider dynamic range (140dB or 7 decades) than any commercially available unit. The 10MHz full-scale frequency is 10 times faster than currently available monolithic V → Fs. The theory of operation is based on the identity Q = CV.

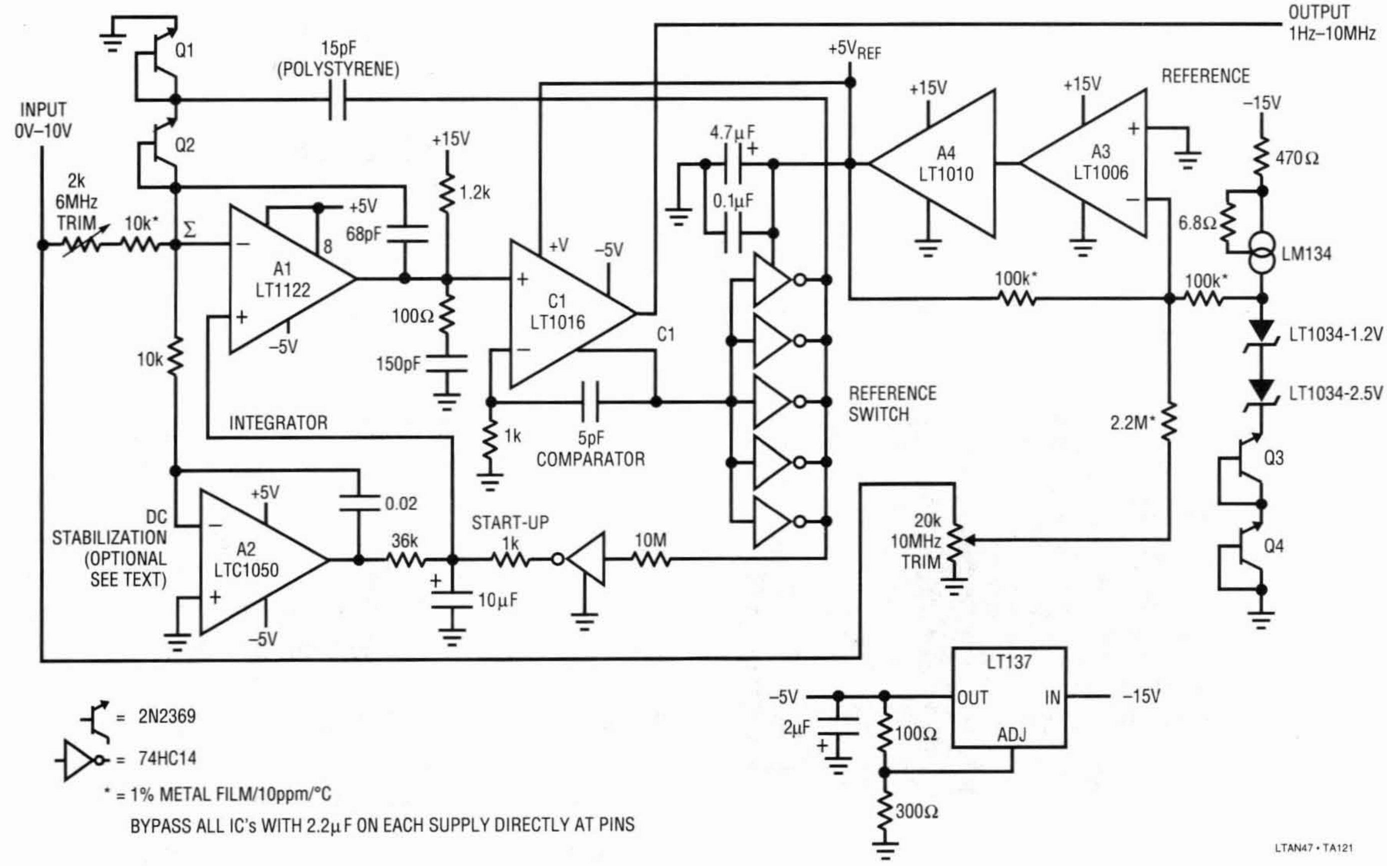

OUTPUT
1Hz–10MHz
Q1
Q2
15pF
(POLYSTYRENE)
INPUT
0V–10V
2k
6MHz
TRIM
10k*
Σ
+5V
8
68pF
+15V
1.2k
A1
LT1122
–5V
100Ω
150pF
+V
–5V
C1
LT1016
C1
1k
5pF
COMPARATOR
10k
INTEGRATOR
+5VREF
4.7μF
0.1μF
REFERENCE SWITCH
+15V
A4
LT1010
+15V
A3
LT1006
REFERENCE
–15V
470Ω
6.8Ω
LM134
100k*
100k*
LT1034-1.2V
LT1034-2.5V
2.2M*
Q3
Q4
20k
10MHz
TRIM
DC
STABILIZATION
(OPTIONAL
SEE TEXT)
+5V
A2
LTC1050
–5V
0.02
36k
START-UP
1k
10μF
10M
LT137
OUT
IN
ADJ
–5V
–15V
2μF
100Ω
300Ω
= 2N2369
= 74HC14
* = 1% METAL FILM/10ppm/°C
BYPASS ALL IC's WITH 2.2μF ON EACH SUPPLY DIRECTLY AT PINS
LTAN47 • TA121

Figure 121. 1Hz-10MHz V-to-F Converter. Linearity is 0.03% with 50ppm/°C Drift

Each time the circuit produces an output pulse, it feeds back a fixed quantity of charge (Q) to a summing node (Σ). The circuit's input furnishes a comparison current at the summing node. The difference signal at the node is integrated in a monitoring amplifier's feedback capacitor. The amplifier controls the circuit's output pulse generator, completing a feedback loop around the integrating amplifier. To maintain the summing node at zero, the pulse generator runs at a frequency which permits enough charge pumping to offset the input signal. Thus, the output frequency will be linearly related to the input voltage. A1 is the integrating amplifier.

0.05µV/°C offset drift performance is obtained by stabilizing A1 with A2, a chopper stabilized op amp. A2 measures the DC value of the negative input, compares it to ground, and forces the positive input to maintain offset balance in A1. Note that A2 is configured as an integrator and cannot see high frequency signals. It functions only at DC and low frequency.

A1 is arranged as an integrator with a 68pF feedback capacitor. When a positive voltage is applied to the input, A1's output integrates in a negative direction (Trace A, Figure 122). During this period, C1's inverting output is low. The paralleled HCMOS inverters form a reference voltage switch. The reference voltage is established by the LM134 current source driven LT1034's and the Q3-Q4 combination. Additionally, a small input voltage related term is summed into the reference, improving overall circuit linearity. A3-A4 provides low drift buffering, presenting a low impedance reference to the paralleled inverter's supply pin. The HCMOS outputs give low resistance, essentially errorless switching. The reference switch's output charges the 15pF capacitor via Q1's path.

When A1's output crosses zero, C1's inverting output goes high and the reference switch (Trace B) goes to ground. This causes the 15pF unit to dispense charge into the summing node via Q2's V_{BE}. The amount of charge dispensed is a direct function of the voltage the 15pF unit was charged to (Q = CV). Q1 and Q2 are temperature compensated by Q3 and Q4 in the reference string. The current through the 15pF unit (Trace C) reflects the charge pumping action. The removal of current from A1's summing junction (Trace D) causes the junction to be driven very quickly negative. The initial negative-going 15ns transient at A1's output is due to amplifier delay. The input signal feeds directly through the feedback capacitor and appears at the output. When the amplifier finally responds, its output (Trace A) slew limits as it attempts to regain control of the summing node. The class A 1.2kΩ pull-up and the RC damper at A1's output minimizes erroneous output movement, enhancing this slew recovery. The amount of time the reference switch remains at ground depends on how long it takes A1 to recover and the 5pF-1000Ω hysteresis network at C1. This 60ns interval is long enough for the 15pF unit to fully discharge. After this, C1 changes state, the reference switch swings positive, the capacitor is recharged and the entire cycle repeats. The frequency at which this oscillation occurs is directly related to the voltage-input-derived current into the summing junction. Any input current will require a corresponding oscillation frequency to hold the summing point at an average value of 0V.

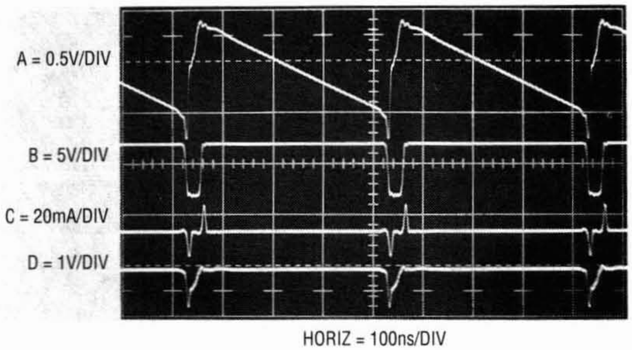


Figure 122. 10MHz V-to-F's Operating Waveforms. LT1122 Integrator is Completely Reset in 60ns

Maintaining this relationship at megahertz frequencies places severe restrictions on circuit timing. The key to achieving 10MHz full-scale operating frequency is the ability to transmit information around the loop as quickly as possible. The discharge-reset sequence is particularly critical and is detailed in Figure 123. Trace A is the A1 integrator output. Its ramp output crosses 0V at the first left vertical graticule division. A few nanoseconds later, C1's inverting output begins to rise (Trace B), switching the reference switch to ground (Trace C). The reference switch begins to head towards ground about 16ns after A1's output crosses 0V. 2ns later, the summing point (Trace D) begins to go negative as current is pulled from it through the 15pF capacitor. At 25ns, C1's inverting

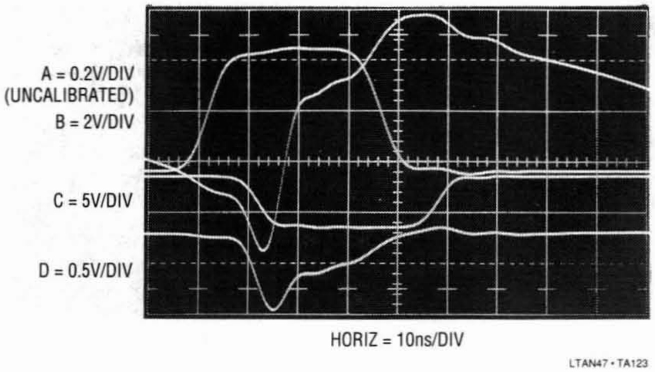


Figure 123. Detail of 60ns Reset Sequence (Whoosh!)

output is fully up, the reference switch is at ground, and the summing point has been pulled to its negative extreme. Now, A1 begins to take control. Its output (Trace A) slews rapidly in the positive direction, restoring the summing point. At 60ns, A1 is in control of the summing node and the integration ramp begins again.

Start-up and overdrive conditions could force A1's output to go to the negative rail and stay there. The AC-coupled nature of the charge dispensing loop can preclude normal operation and the circuit may latch. The remaining HCMOS inverter provides a watchdog function for this condition. If A1's output rails negative the reference switch tries to stay at ground. The remaining inverter goes high, lifting A1's positive input. This causes A1's output to slew positive, initiating normal circuit action. The 1k-10μF combination and the 10M-inverter input capacitance limit start-up loop bandwidth, preventing unwanted outputs.

The LM134 current source driving the reference string has a built in 0.33%/°C thermal coefficient, causing slight voltage modulation in the Q3-Q4 pair over temperature. This small change (≈ +120 ppm/°C) opposes the –120ppm/°C drift in the 15pF polystyrene capacitor, aiding overall circuit tempco.

To trim this circuit, apply exactly 6V at the input and adjust the 2kΩ potentiometer for 6.000MHz output. Next, put in exactly 10V and trim the 20k unit for 10.000MHz output. Repeat these adjustments until both points are fixed. A2's low drift eliminates a zero adjustment. If operation below 600Hz is not required, A2 and its associated components may be deleted.

Linearity of this circuit is 0.03% with full-scale drift of 50ppm/°C. Zero point error, controlled by A2, is 0.05Hz/°C.

8-Bit, 100ns Sample-Hold

Figure 124 shows a simple, very fast sample-hold circuit. This circuit will acquire a ±5V input to 8-bit accuracy in 100ns. Hold step is inside 1/4 LSB with hold settling inside 25ns. Aperture time is 4ns and droop rate about 1/2 LSB/μs.

The input is fed to a Schottky switching bridge via inverting buffer A1. The Schottky bridge, similar to types used in sampling oscilloscopes[16], gives 1ns switching and eliminates the charge pump-through that a FET switch would contribute. The switching bridge's output feeds output amplifier A2. A2, configured as an integrator, is the actual hold amplifier. Its output is fed back to the switching bridge's input, forming a summing point with A1's output resistor. This feedback loop places the bridge within a loop, enhancing accuracy.

The bridge is switched by driving the sample-hold input line. Q1 and Q2 drive L1's primary. L1's secondaries provide complementary drive to the bridge with almost no time skewing.

Figure 125 shows the circuit acquiring a full scale step. Trace A is the input command while Trace B is A2's output. The aberration visible in A2's output when switching into hold (hold step) is due to minute residual AC imbalances in the bridge. Figure 126 studies this effect in high resolution detail, with the hold step trim deliberately disconnected. After A2's output nominally settles at final value, the circuit is switched into hold. The bridge imbalance allows a small parasitic charge to be displaced into A2's summing point, causing A2 to step 10mV higher (in this case). If the trim is connected and properly adjusted, it supplies a small compensatory charge during switching. Figure 127 shows the effect of this on the output. The settled hold output is the same as the acquired value. To trim this circuit, ground the input while pulsing the sample-hold control line. Next, adjust the trim for minimal amplitude step between the sample and hold states.

In contrast to low frequency sample-hold circuits this design cannot pass signal if left in the sample mode. The transformer's inherent AC coupling precludes such operation. Similarly, extended sample mode duration (e.g., >500ns) will cause transformer saturation, resulting in erroneous outputs and excessive Q1-Q2 dissipation. If

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Note 16: See References 7, 8 and 28.

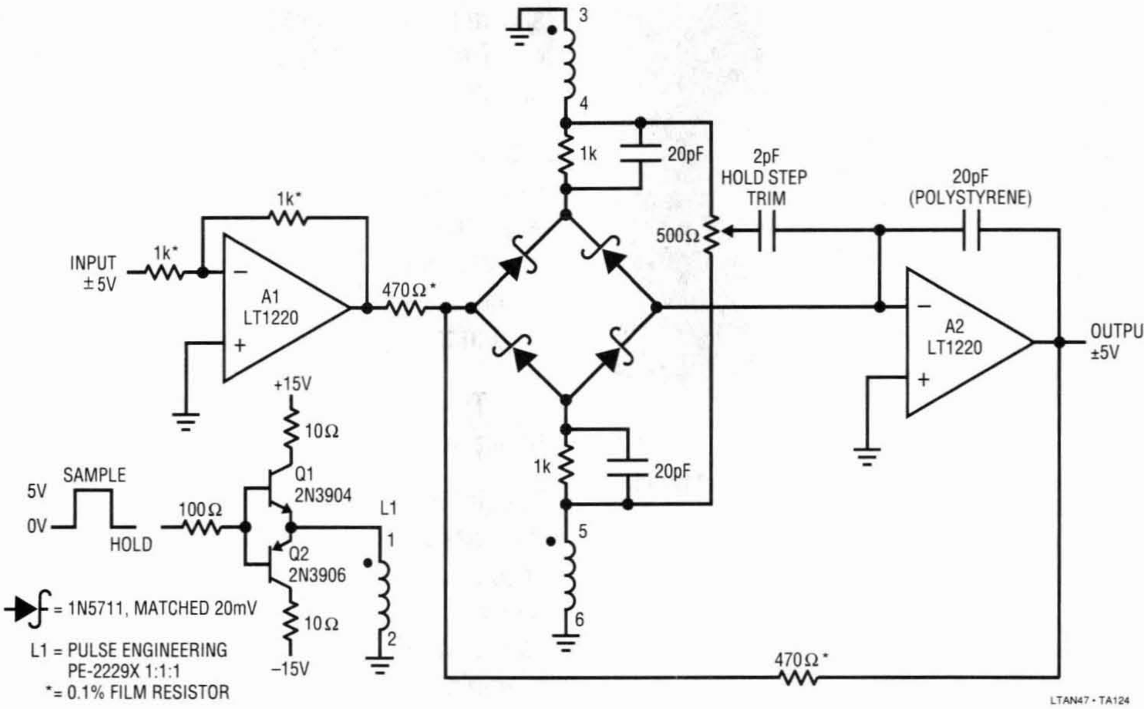
3
4
1k
20pF
2pF
HOLD STEP
TRIM
20pF
(POLYSTYRENE)
500Ω
1k*
INPUT
±5V
1k*
A1
LT1220
470Ω*
A2
LT1220
OUTPUT
±5V
+15V
10Ω
SAMPLE
5V
0V
HOLD
100Ω
Q1
2N3904
Q2
2N3906
L1
1
2
1k
20pF
5
6
10Ω
−15V
= 1N5711, MATCHED 20mV
L1 = PULSE ENGINEERING
PE-2229X 1:1:1
* = 0.1% FILM RESISTOR
470Ω*
LTAN47 • TA124

Figure 124. 8-Bit, 100ns Sample-Hold

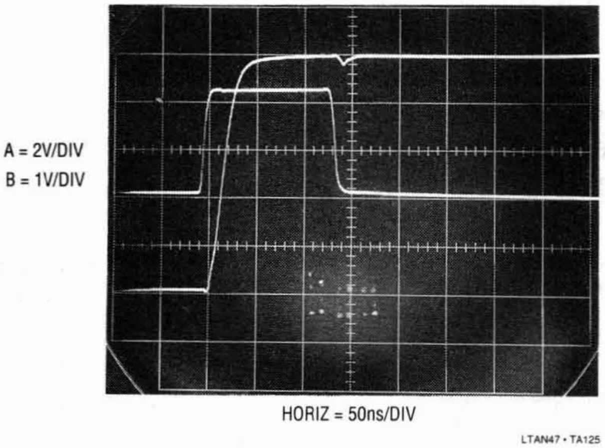

Figure 125. Fast Sample-Hold Acquiring a Full-Scale Input

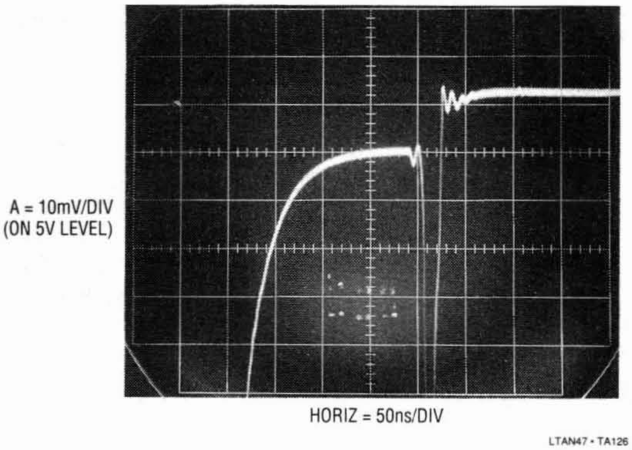

Figure 126. Hold Step with Mis-Adjusted Compensation

extended logic high durations are possible at the control input, it should be AC coupled.

15ns Current Summing Comparator

Figure 128 shows a way to build a high speed current comparator with resolution in the 12-bit range. Current comparison, the fastest way to compare D → A outputs and analog values, is commonly used in high speed A → D converters and instrumentation. A1 is set up as a Schottky bounded amplifier. The bound diodes prevent A1 from saturating due to excessive summing point overdrive, aiding response time. The 3pF capacitor, a typical value, compensates DAC output capacitance and is selected for best amplifier damping. The 10k feedback resistor, also typical, is chosen for best gain-bandwidth performance. Voltage gains of 4 to 10 are common. Figure 129 shows performance. Trace A, a test input, causes A1's output (Trace B) to slew through zero (screen center horizontal line). When A1 crosses zero, C1's input biases negative and it responds (C1's output is Trace C) 10ns later with a

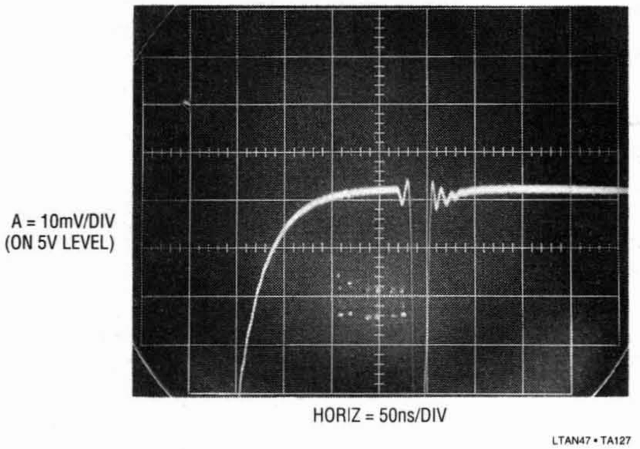

Figure 127. Hold Step with Properly Adjusted Compensation

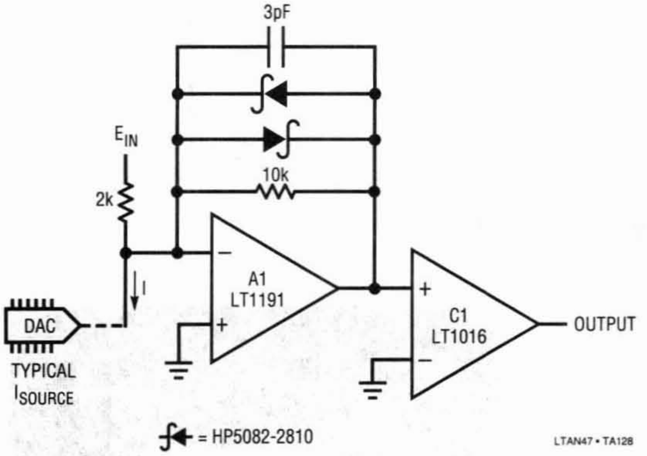

Figure 128. Fast Summing Comparator

TTL output. Total elapsed time from the test input arriving at a TTL high until the comparator output achieves a TTL high is inside 15ns.

50MHz Adaptive Threshold Trigger Circuit

Figure 130 is an extremely versatile trigger circuit. Designing a fast, stable trigger is not easy and often entails a considerable amount of discrete circuitry. This circuit reliably triggers from DC-50MHz over a 2mV-300mV input range with no level adjustment required.

A1, a gain of ten preamplifier, feeds an adaptive trigger configuration identical to the one described in Figure 97's fiber optic receiver. The adaptive trigger maintains the A3 output comparator's trip point at 1/2 input signal amplitude, regardless of its magnitude. This insures reliable automatic triggering over a wide input amplitude range, even for very low level inputs. As an option, the network shown in dashed lines permits changing the trip threshold. This allows any point on the input waveform edge to be selected as the actual trigger point.[17]

Figure 131 shows performance for a 40MHz input sine wave (Trace A). A1's output (Trace B) takes gain and the A3 comparator gives a clean logic output (Trace C). At the highest frequencies, any bandwidth limiting in A1 is irrelevant; the adaptive trigger threshold will simply vary ratiometrically to maintain circuit output.

Fast Time-to-Height (Pulsewidth-to-Voltage) Converter

The circuit of Figure 132 allows very short pulsewidths (in this case 250ns full-scale) to be determined to a typical accuracy of 1%. Digital methods of achieving similar results dictate clock speeds of 1GHz, which is cumbersome. In addition, processor based approaches using averaging techniques require repetitive pulses which this circuit does not. Circuits of this type are frequently required in automatic test equipment and nuclear and high energy physics work where determination of short pulsewidths is a common requirement.

The circuit functions by charging a capacitor during the period of a pulsewidth. When the pulse ends, charging ceases and the voltage across the capacitor is proportional to the width of the pulse.

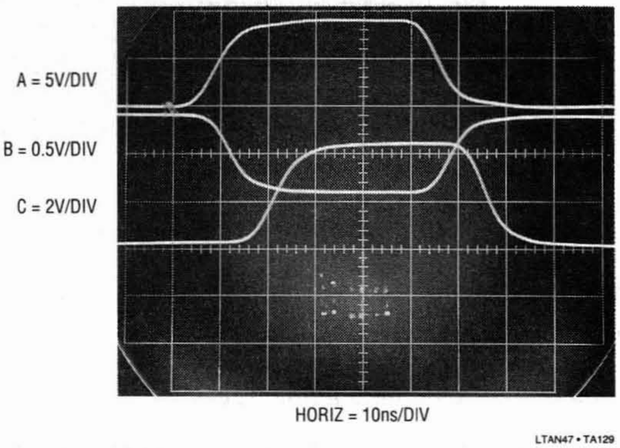

Figure 129. Fast Summing Comparator's Waveforms. Total Delay is 15ns

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Note 17: This technique is borrowed from oscilloscope trigger circuitry. See Reference 29.

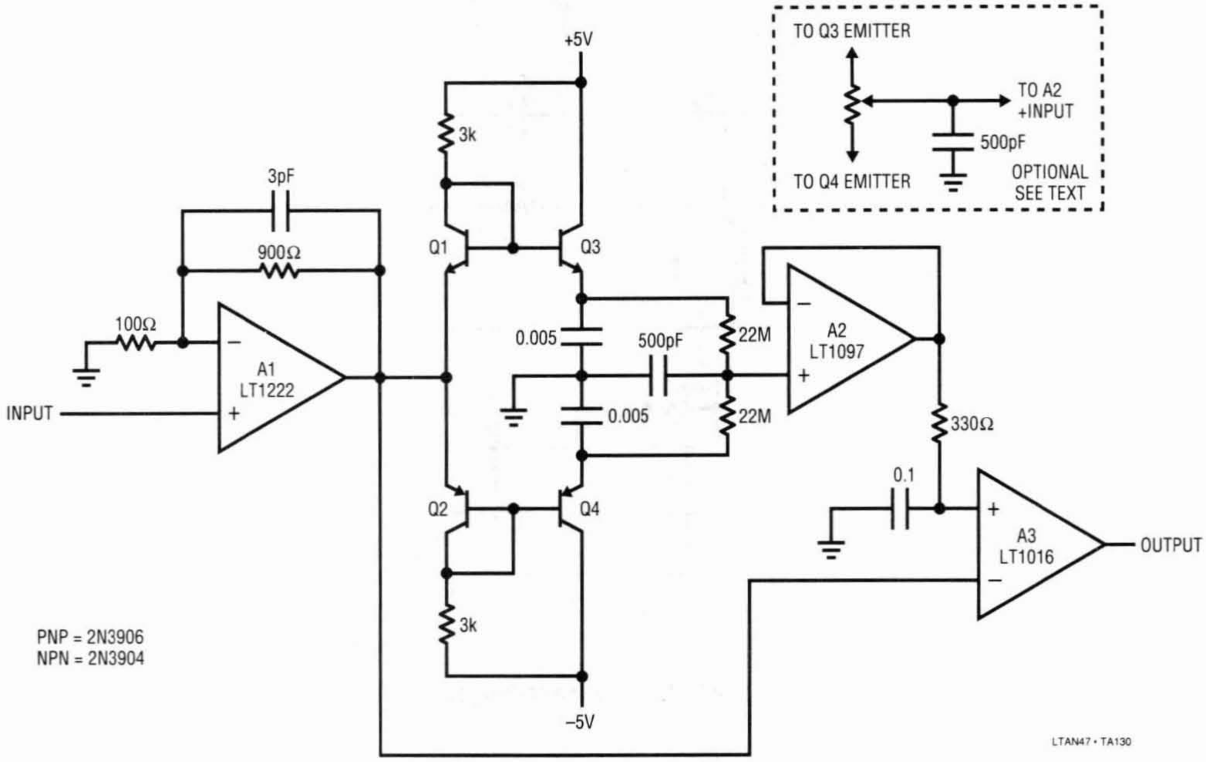
+5V
3k
3pF
900Ω
100Ω
A1
LT1222
INPUT
Q1
Q3
0.005
500pF
0.005
22M
22M
A2
LT1097
330Ω
0.1
A3
LT1016
OUTPUT
Q2
Q4
3k
-5V
PNP = 2N3906
NPN = 2N3904
TO Q3 EMITTER
TO A2 +INPUT
500pF
TO Q4 EMITTER
OPTIONAL SEE TEXT
LTAN47 • TA130

Figure 130. 50MHz Trigger with Adaptive Threshold

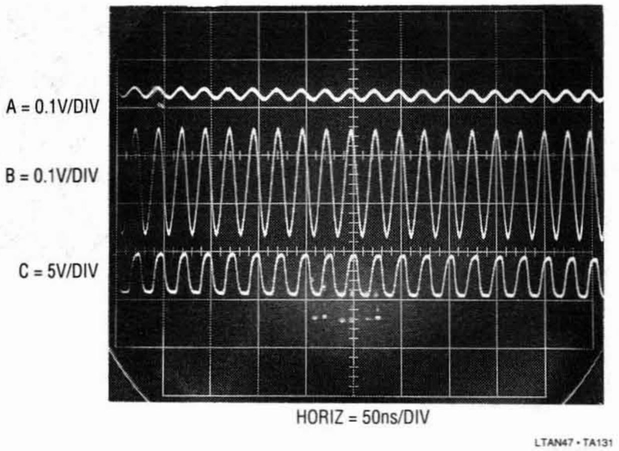

Figure 131. The Trigger Responds to a 40MHz Input. Input Amplitude Variations from 2mV-300mV Have No Effect

The input pulse to be measured (Trace A, Figure 133) simultaneously biases the 74C221 dual one shot and Q3. Q3, aided by Baker[18] clamping, capacitive feedforward and optimized DC base biasing, turns off in a few nanoseconds. Current source Q2's emitter forward biases and Q2 supplies constant current to the 100pF integrating capacitor. Q1 supplies temperature compensation for Q2, with the 2.5V LT1009 referencing the current source. Q2's collector (e.g., the 100pF capacitor) charges in ramp fashion (Trace B). A1 supplies a buffered output (Trace C). When the input pulse ends, Q3 rapidly turns on, reverse biasing Q2's emitter and turning off the current source. A1's voltage is directly proportional to the input pulse width. A monitoring A → D converter can acquire this data.

After a time set by the 74C221's RC programmed delay, a pulse appears at its Q2 output (Trace D). This pulse turns on Q4, discharging the 100pF capacitor to zero and readying the circuit for the next input pulse.

This circuit's accuracy and resolution are crucially dependent on minimizing delay in switching the Q1-Q2 current source. Figure 134 provides amplitude and time expanded versions of critical circuit waveforms. Trace A is the input pulse and Trace B is A1's input, showing the beginning of the ramp's ascent. Trace C, A1's output, shows about 13ns delay from A1's input. Traces D and E, A1's input and

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Note 18: See Reference 45.

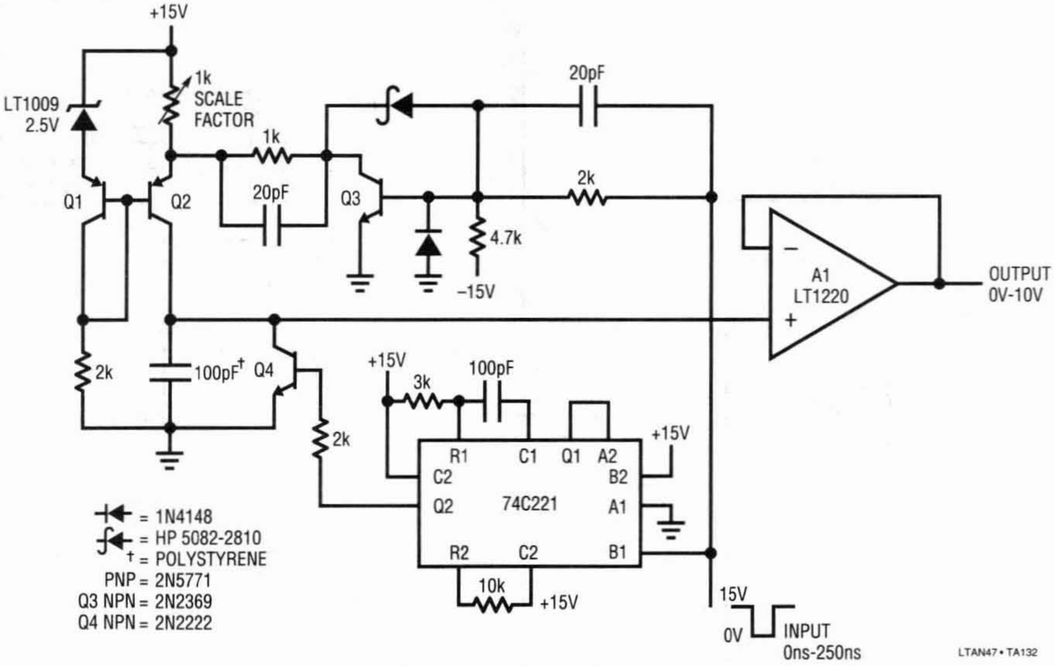
+15V
LT1009
2.5V
1k
SCALE
FACTOR
1k
20pF
20pF
2k
4.7k
–15V
Q1
Q2
Q3
Q4
2k
100pF†
A1
LT1220
OUTPUT
0V-10V
+15V
3k
100pF
+15V
R1
C1
Q1
A2
C2
B2
Q2
74C221
A1
R2
C2
B1
10k
+15V
2k
= 1N4148
= HP 5082-2810
† = POLYSTYRENE
PNP = 2N5771
Q3 NPN = 2N2369
Q4 NPN = 2N2222
15V
0V
INPUT
0ns-250ns
LTAN47 • TA132

Figure 132. Fast Time-to-Height Converter

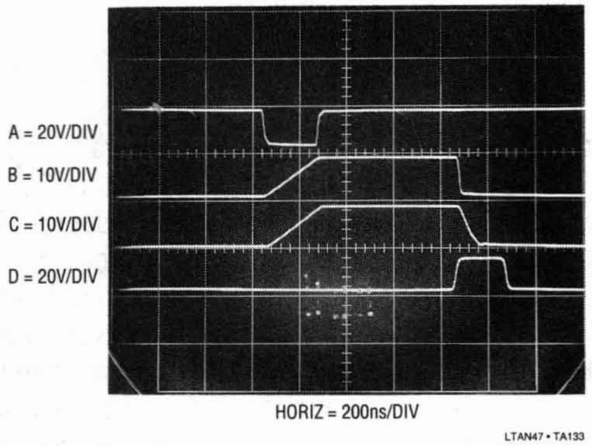

Figure 133. Time-to-Height Converter Acquires a 250ns Pulse

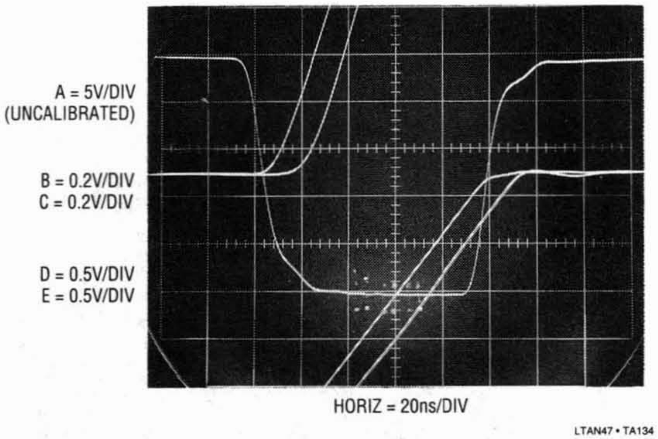

Figure 134. Detail of Time-to-Height Converter's Ramp Switching

output respectively, record similar A1 delays for ramp turn-off. The photo reflects the extremely fast current source switching; the vast majority of delay is due to A1's delay. A1's delay is far less critical than current source switching delays; A1 will always settle to the correct value well before the one shot resets the circuit. In practice, a monitoring A → D converter should not be triggered until about 50ns after the circuit's input pulse has ceased. This gives A1 plenty of time to catch up to the 100pF capacitor's settled value.

As mentioned, current source switching speed is essential for good results. Figure 135 details current source turn off. Trace A is the circuit's input pulse rising edge and Trace B shows the top of the ramp. Turn off occurs in a few nanoseconds. Similar speed is characteristic of the input's falling edge (current source turn on). Additionally, it is noteworthy that circuit accuracy and resolution limits are set by the *difference* in current source turn on and off delays. As such, the *effective* overall delay is extremely small.

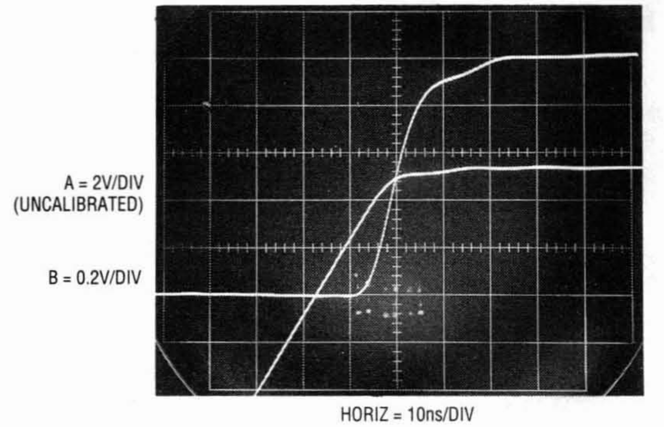

Figure 135. Current Source Turn-Off Detail for the Time-to-Height Converter

To calibrate this circuit, put in a 250ns width pulse and trim the 1kΩ potentiometer for 10V output. The circuit will convert pulse widths from 20ns to 250ns to a typical accuracy of 1%. The 20ns minimum measurable width is due to inability to fully discharge the 100pF capacitor. If this is objectionable, Q4 can be replaced with a lower saturation device or A1's output can be offset.

True RMS Wideband Voltmeter

Most AC RMS measurements use logarithmic techniques to compute the waveform's RMS value. This method limits bandwidth to below 1MHz and crest factor performance to about 10:1. Practically speaking, a waveform's RMS value is defined as its heating value in the load. Specialized instruments employ thermally based assemblies that compute the RMS value of the input. The thermal method provides substantially improved bandwidth and crest factor capability compared to logarithmically based converters.

Thermal RMS-DC converters are direct acting, thermoelectronic analog computers. The thermal technique is explicit, relying on first principles. The simple operation permits wideband performance unattainable with implicit, indirect methods based on logarithmic computing.

Figure 136 shows a classic scheme for implementing a thermally based RMS-DC converter. Here, the DC amplifier forces a second, identical, heater-sensor pair to the same thermal conditions as the input driven pair. This differentially sensed, feedback enforced loop makes ambient temperature shifts a common-mode term, eliminating their effect. Also, although the voltage and thermal interaction is non-linear, the input-output voltage relationship is linear with unity gain. The ability of this arrangement to reject ambient temperature shifts depends on the heater-sensor pairs being isothermal. This is achievable by thermally insulating them with a time constant well below that of ambient shifts. If the time constants to the heater-sensor pairs are matched, ambient temperature terms will affect the pairs equally in phase and amplitude. The DC amplifier will reject this common-mode term. Note that, although the pairs are isothermal, they are insulated from each other. Any thermal interaction between the pairs reduces the system's thermally based gain terms. This would cause unfavorable signal-to-noise performance, limiting dynamic operating range. Figure 136's output is linear because the matched thermal pair's non-linear voltage-temperature relationships cancel each other.

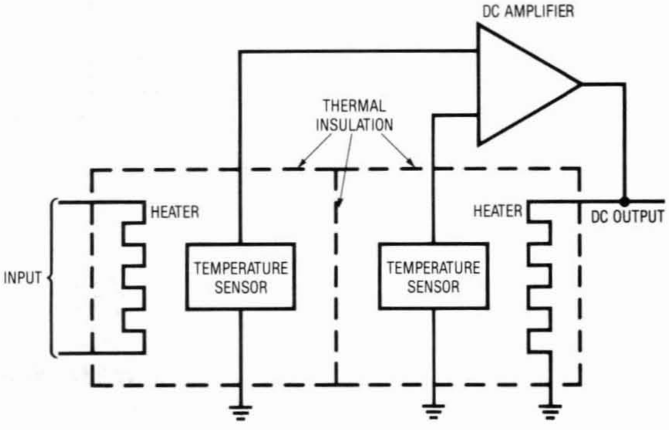

Figure 136. Conceptual Thermal RMS-DC Converter

The advantages of this approach have made its use popular in thermally based RMS-DC measurements. Typically, the assembly is composed of matched heater resistors, sensors and thermal insulation. These assemblies are relatively large and expensive to produce. Figure 137's economical wideband thermally based voltmeter is based on a monolithic thermal converter. The LT1223 provides gain, and drives the LT1088 RMS-DC thermal converter.[19] The LT1088's temperature sensing diodes are biased from the supply. A1, set up as a differential servo amplifier with a gain of 9000, extracts the diode's difference signal and biases Q1. Q1 drives one of the LT1088's heaters, completing a loop. The 3300pF capacitor gives a stable roll-off.

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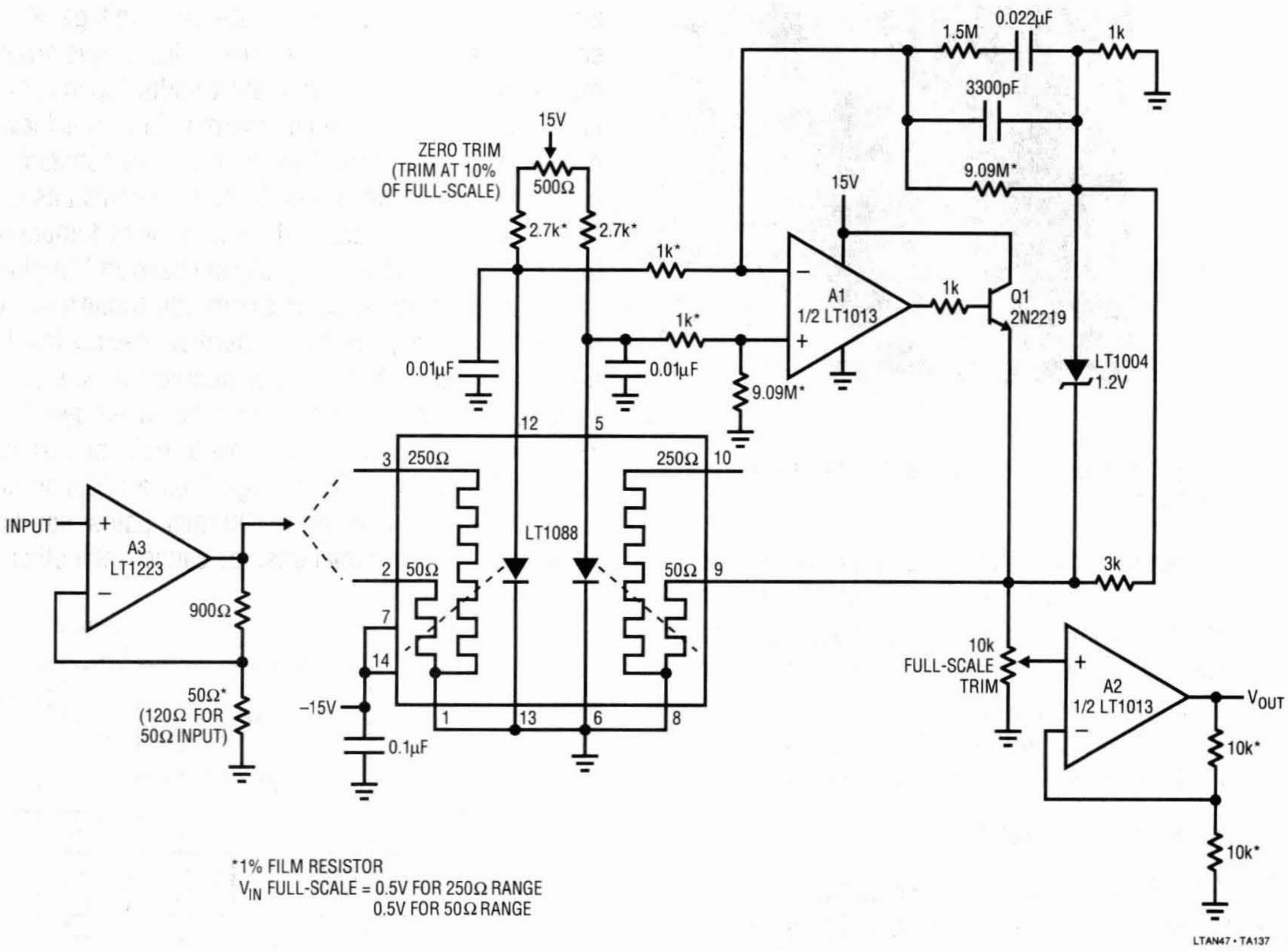
[19] **Note 19:** Complete details on this device and a discussion on thermal conversion considerations are found in Reference 40.


1.5M
0.022μF
1k
3300pF
9.09M*
15V
ZERO TRIM (TRIM AT 10% OF FULL-SCALE)
500Ω
2.7k*
2.7k*
1k*
1k*
A1 1/2 LT1013
1k
Q1 2N2219
LT1004 1.2V
0.01μF
0.01μF
9.09M*
12
5
3
250Ω
250Ω
10
LT1088
2
50Ω
50Ω
9
3k
INPUT
A3 LT1223
900Ω
7
14
10k FULL-SCALE TRIM
A2 1/2 LT1013
VOUT
10k*
10k*
50Ω* (120Ω FOR 50Ω INPUT)
–15V
1
13
6
8
0.1μF
LTAN47 • TA137

*1% FILM RESISTOR
V_{IN} FULL-SCALE = 0.5V FOR 250Ω RANGE
0.5V FOR 50Ω RANGE

Figure 137. Wideband True RMS Voltmeter

The 1.5M-0.022μF combination improves settling by reducing gain during output slew. The LT1088's square-law thermal gain means overall loop gain is lower for small inputs. Normally, this would result in slow settling for values below about 10%-20% of scale. The LT1004 1k-3k network is a simple breakpoint, boosting amplifier gain in this region to improve settling. A2, a gain trimmable output stage, serves to compensate for gain variations in the two sides of the LT1088. To trim the circuit, put in about a 10% scale DC signal (e.g., 0.05V). Adjust the zero trim so that $V_{OUT} = V_{IN}$. Next, apply a full-scale DC input and set the full-scale trim to that value at the output. Repeat the trims until both are fixed well within 1% of full-scale. An alternate trim scheme involves applying no input, grounding Q1's base and setting the zero trim until A1's output is active. Then, unground Q1's base, apply a full-scale input and trim the full-scale adjustment for that value at the output.

Figure 138 is a plot of error vs input frequency. The LT1088 is specified at 2% to 100MHz (50Ω heater) or 1% to 20MHz (250Ω heater). As such, most of the error shown is due to bandwidth restrictions in A3, but performance is still impressive. The plots include data taken at various input levels into both heaters. A 500mV input into 250Ω dips to 1% at 8MHz and 2.5% at 14MHz before peaking badly beyond 17MHz. This input level forces a 9.5 V_{RMS} output at A3, introducing large signal bandwidth limitations. The 400mV input to the 250Ω heater shows essentially flat results to 20MHz, the LT1088's 250Ω heater specification limit.

The 50Ω heater provides significantly wider bandwidth, although A3's 50mA output limits maximum input to about $100mV_{RMS}$ ($1.76V_{RMS}$ at the LT1088).

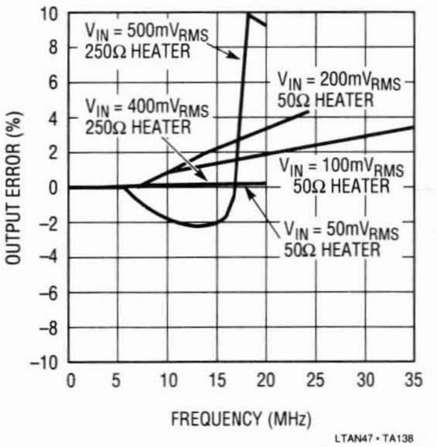


Figure 138. Accuracy Plot for the RMS Voltmeter

APPLICATIONS SECTION IV - MISCELLANEOUS CIRCUITS

RF Leveling Loop

Figure 137's wideband AC conversion can be applied in other areas. A common RF requirement is to stabilize the amplitude of a waveform against variations in input, time and temperature. Instruments and transmitters frequently require this function, which is not easy if waveform purity must be maintained. Figure 139A shows a 25MHz RF leveling loop. The RF input is applied to the AD539 wideband multiplier. The multiplier's output drives A1. A1's output is converted to DC by the LT1088 based RMS-DC converter (see previous circuit). A servo amplifier compares this output with a settable DC reference and biases the multiplier's control channel, completing a loop. The 0.33μF capacitor provides frequency compensation by rolling off gain at a frequency well below the response of the LT1088 servo. The loop maintains the output's 25MHz RMS amplitude at the DC reference's value. Changes in load, input, power supply and other variables are rejected.

Figure 139B, a similar circuit, offers significantly lower cost although performance is not quite as good. The RF input is applied to LT1228 A1, an operational transconductance amplifier. A1's output feeds LT1228 A2, a current feedback amplifier. A2's output, the circuit's output, is sampled by the A3 based gain control configuration. This arrangement, similar to the gain control loops described in Figures 112 and 114, closes a gain control loop back at A1. The 4pF capacitor compensates rectifier diode capacitance, enhancing output flatness vs frequency. A1's I_{SET} input current controls its gain, allowing overall output level control. This approach to RF leveling is simple and inexpensive, although output drift, distortion and regulation are somewhat higher than in the previous circuit.

Voltage Controlled Current Source

Figure 140 shows a voltage controlled current source with load and control voltage referred to ground. This simple, powerful circuit produces output current in accordance with the sign and magnitude of the control voltage. The circuit's scale factor is set by resistor R. A1, biased by V_{IN}, drives current through R (in this case 10Ω) and the load. A2, sensing differentially across R, closes a loop back to A1. The load current is constant because A1's loop forces a fixed voltage across R. The 2k-100pF combination sets roll off and the configuration is stable. Figure 141 shows dynamic response. Trace A is the voltage control input while Trace B is the output current. Response is quick and clean, with delay of 5ns and no slew residue or aberration.

High Power Voltage Controlled Current Source

Figure 142 is identical to the basic current source, except that it adds a 1A booster stage (adapted from Figure 104) for increased output power. Including the booster inside A1's feedback loop eliminates its DC errors. Note that the booster's current limiting features have been removed, because of this circuit's inherent current limiting nature of operation. Figure 143 shows this circuit's response to be as clean as the lower power version, although delay is about 20ns slower. It is worth mentioning that the loop stability considerations involved in placing A2 *and* the booster in A1's feedback path are significant. This circuit receives treatment in Appendix C, "The Oscillation Problem - Frequency Compensation Without Tears".

18ns Circuit Breaker

Figure 144 shows a simple circuit which will turn off current in a load 18ns after it exceeds a preset value. This circuit has been used to protect integrated circuits during developmental probing and is also useful for protecting expensive loads during trimming and calibration. The circuit's versatility is enhanced because one side of the load is grounded. Under normal conditions, Q1's emitter (Trace A, Figure 145, is Q1's current, and Trace C is its

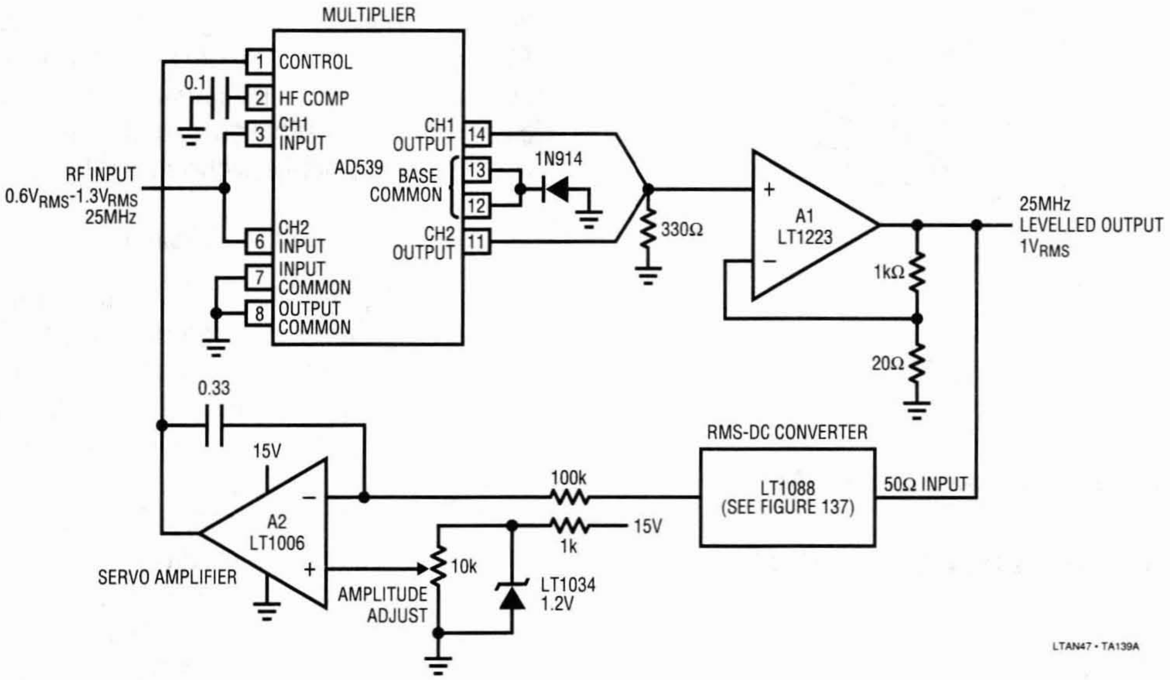

MULTIPLIER
1 CONTROL
0.1
2 HF COMP
3 CH1 INPUT
CH1 OUTPUT 14
AD539
BASE COMMON 13 12
1N914
RF INPUT
0.6V$_{RMS}$-1.3V$_{RMS}$
25MHz
6 CH2 INPUT
CH2 OUTPUT 11
7 INPUT COMMON
8 OUTPUT COMMON
330Ω
A1
LT1223
1kΩ
20Ω
25MHz
LEVELLED OUTPUT
1V$_{RMS}$
0.33
15V
A2
LT1006
SERVO AMPLIFIER
100k
1k
15V
10k
AMPLITUDE ADJUST
LT1034
1.2V
RMS-DC CONVERTER
LT1088
(SEE FIGURE 137)
50Ω INPUT
LTAN47 • TA139A

Figure 139A. RF Leveling Loop

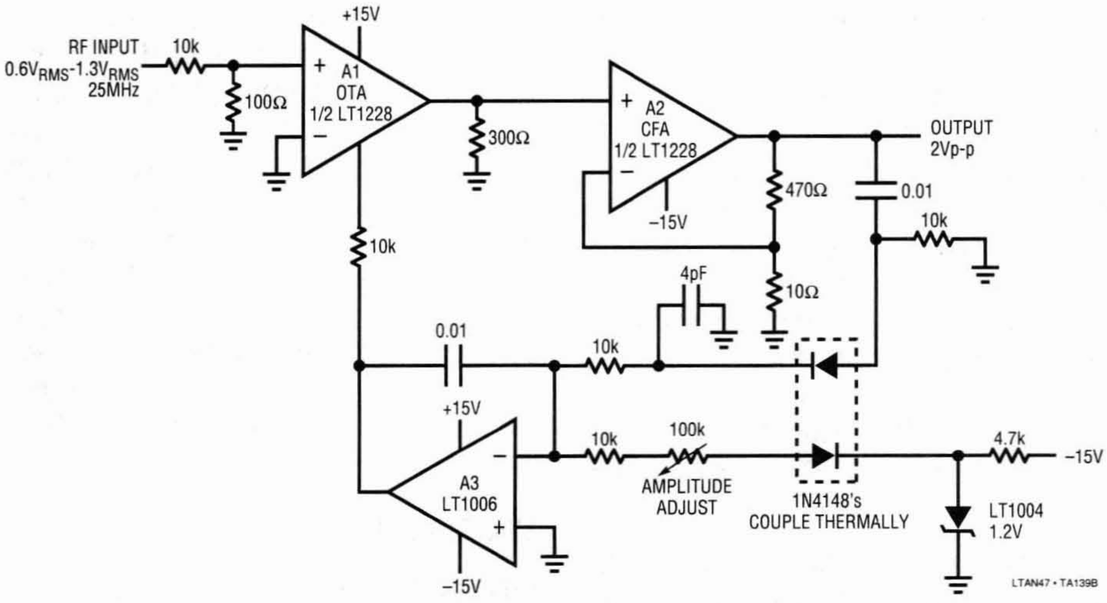

+15V
RF INPUT
0.6V$_{RMS}$-1.3V$_{RMS}$
25MHz
10k
100Ω
A1
OTA
1/2 LT1228
300Ω
A2
CFA
1/2 LT1228
−15V
OUTPUT
2Vp-p
470Ω
0.01
10k
10k
4pF
10Ω
0.01
10k
+15V
A3
LT1006
−15V
10k
100k
AMPLITUDE ADJUST
1N4148's
COUPLE THERMALLY
4.7k
−15V
LT1004
1.2V
LTAN47 • TA139B

Figure 139B. Simple RF Leveling Loop

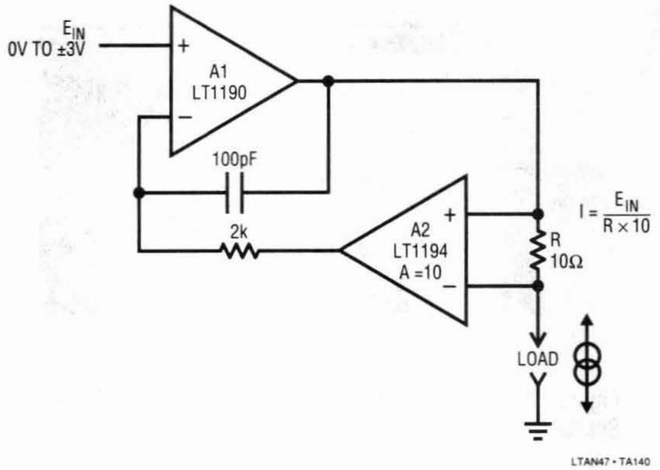

E_IN
0V TO ±3V
A1
LT1190
100pF
2k
A2
LT1194
A =10
R
10Ω
I = E_IN / R × 10
LOAD
LTAN47 • TA140

Figure 140. Fast, Precise, Voltage Controlled Current Source with Grounded Load

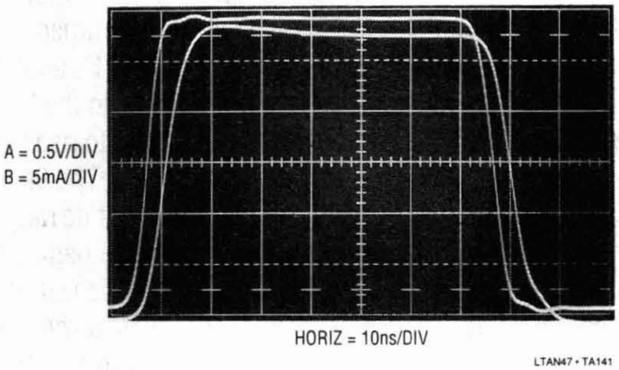


Figure 141. Dynamic Response of the Current Source. Delay is 4ns, with Clean Settling

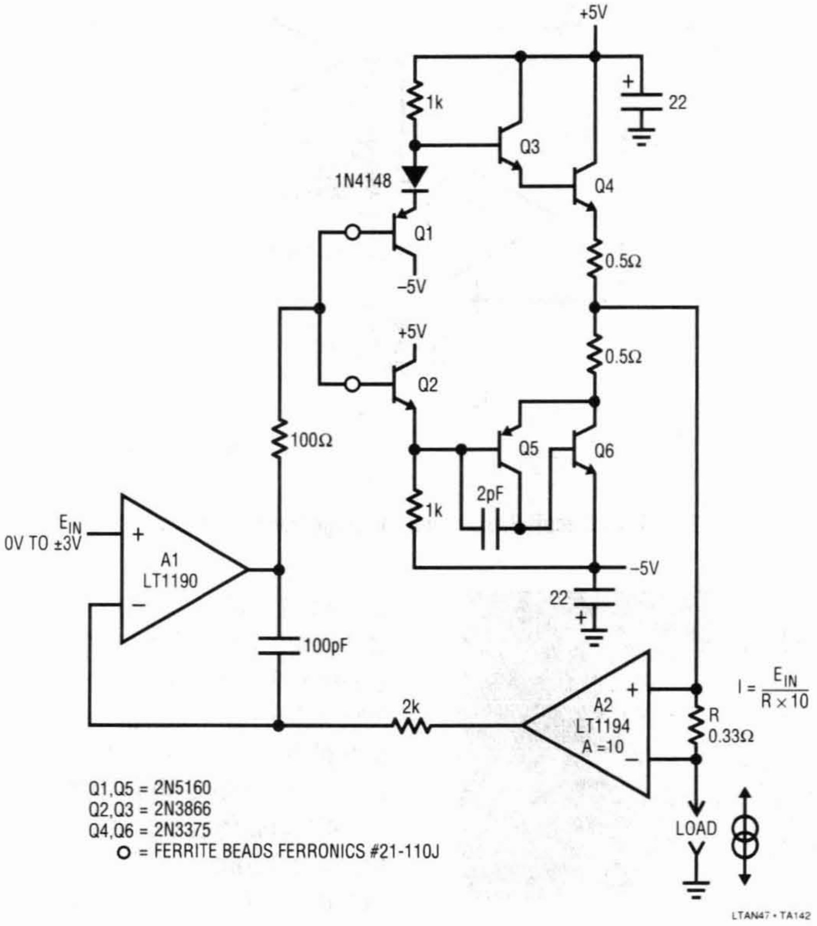

+5V
1k
22
Q3
Q4
1N4148
Q1
–5V
0.5Ω
+5V
0.5Ω
Q2
100Ω
Q5
Q6
2pF
1k
–5V
22
E_IN
0V TO ±3V
A1
LT1190
100pF
2k
A2
LT1194
A =10
R
0.33Ω
I = E_IN / R × 10
LOAD
Q1,Q5 = 2N5160
Q2,Q3 = 2N3866
Q4,Q6 = 2N3375
○ = FERRITE BEADS FERRONICS #21-110J
LTAN47 • TA142

Figure 142. High Power, Wideband Voltage Controlled Current Source

voltage) is biased on, supplying power to the load via the 10Ω current shunt. Differential amplifier A1's output resides below comparator A2's voltage programmed trip point and Q2 is off. When an overload occurs, Q1's emitter current begins to increase (Trace A, just prior to the third vertical division). A1's output (Trace B) begins to rise as it tracks the increase in the 10Ω shunt's voltage. The 9k-1k dividers keep A1 inputs inside their common-mode range. Simultaneously, Q3's emitter voltage (Trace C) begins to drop as it beta limits. When A1's version of the load current exceeds A2's trip point, A2 (Trace D) goes high, turning on Q2. Q2's turn on steals Q1's base drive, turning off the load current. Local positive feedback at A2's latch pin causes it to latch in this off state. When the load fault has been cleared, the pushbutton can be used to reset the circuit. The delay from the onset of excessive load current to complete shutdown is inside 18ns. The 4ns delay of Trace A's current probe should be factored in when interpreting waveforms. To calibrate this circuit, ground Q2's base and install a 250mA load. Adjust the 200Ω trim for a 2.5V output at A1. Next, remove the load, unground Q2's base and press the reset button. Finally, put in the desired trip set voltage and the circuit is ready for use.

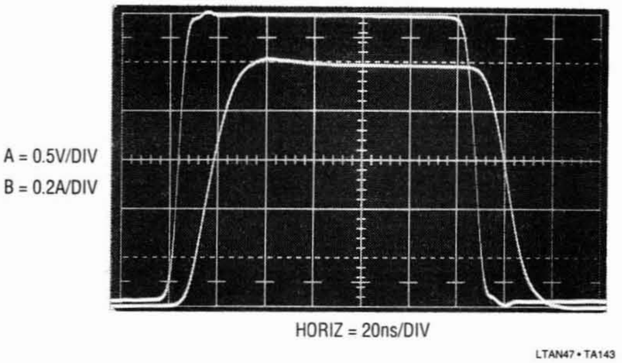


Figure 143. 1A Pulse Response of the High Power Current Source

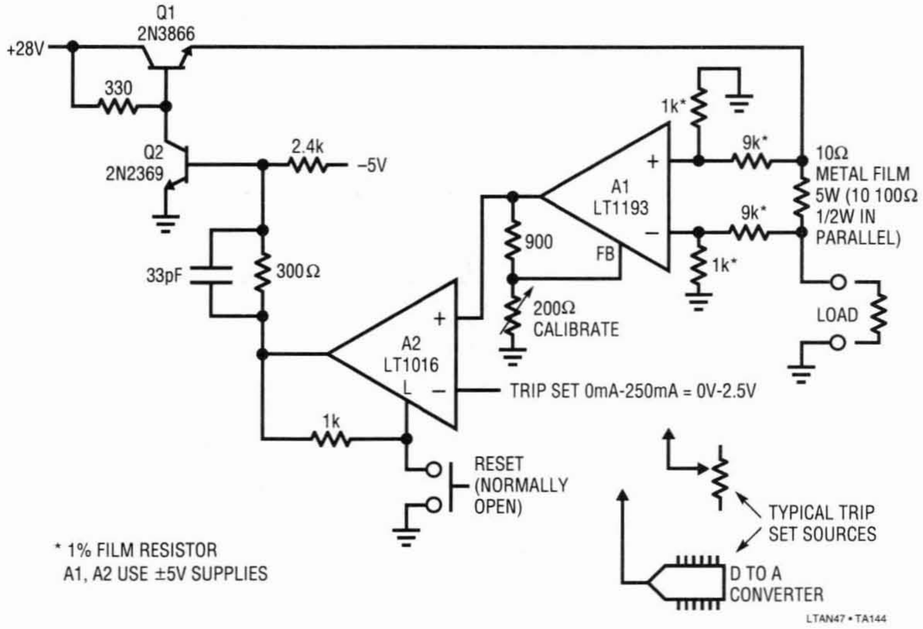

+28V
Q1
2N3866
330
Q2
2N2369
2.4k
–5V
33pF
300Ω
A2
LT1016
L
+
–
1k
RESET
(NORMALLY
OPEN)
900
200Ω
CALIBRATE
A1
LT1193
FB
1k*
9k*
9k*
1k*
10Ω
METAL FILM
5W (10 100Ω
1/2W IN
PARALLEL)
LOAD
TRIP SET 0mA-250mA = 0V-2.5V
TYPICAL TRIP
SET SOURCES
D TO A
CONVERTER
* 1% FILM RESISTOR
A1, A2 USE ±5V SUPPLIES
LTAN47 • TA144

Figure 144. 18ns Circuit Breaker with Voltage Programmable Trip Point

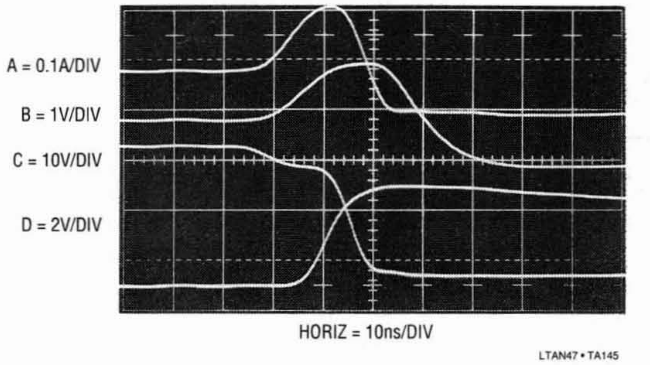


Figure 145. Operating Waveforms for the 18ns Circuit Breaker. Circuit Output (Trace C) is Shut Down 18ns After Output Current (Trace A) Begins to Rise

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Note: *This application note was derived from a manuscript originally prepared for publication in EDN Magazine.*

APPENDIX A

ABC's of Probes – Tektronix, Inc.

This appendix, guest written by the engineering staff of Tektronix, Inc., is a distillation of their booklet, "ABC's of Probes". The complete booklet is available, at no charge, through any Tektronix sales office or call 800-835-9433 ext. 170. For excellent technical background on probe theory see Reference 42.

PART I: UNDERSTANDING PROBES

The vital link in your measurement system

Probes connect the measurement test points in a DUT (device under test) to the inputs of an oscilloscope. Achieving optimized system performance depends on selecting the proper probe for your measurement needs.

Though you could connect a scope and DUT with just a wire, this simplest of connections would not let you realize the full capabilities of your scope. By the same token, a probe that is not right for your application can mean a significant loss in measurement results, plus costly delays and errors.

Why not use a piece of wire?

Good question: There are legitimate reasons for using a piece of wire or, more correctly, two pieces of wire; some low bandwidth scopes and special purpose plug-in amplifiers only provide binding post input terminals, so they offer a convenient means of attaching wires of various lengths.

DC levels associated with battery operated equipment could be measured. Low frequency (audio) signals from the same equipment could also be examined. Some high output transducers could also be monitored. However, this type of connection should be kept away from line-operated equipment for two basic reasons, safety and risk of equipment damage.

Safety: Attachment of hookup wires to line-operated equipment could impose a health hazard, either because the "hot" side of the line itself could be accessed, or because internally generated high voltages could be contacted. In both cases, the hookup wire offers virtually no operator protection, either at the equipment source or at the scope's binding posts.

Risk of Equipment Damage: Two unidentified hookup wires, one signal lead and one ground, could cause havoc in line-operated equipment. If the "ground" wire is attached to **any** elevated signal in line-operated equipment, various degrees of damage will result simply because both the scope and the equipment are (or should be) on the same three-wire outlet system, and short-circuit continuity is completed through one common ground.

Performance Considerations: In addition to the hazards just mentioned, there are two major performance limitations associated with using hookup wires to transfer the signal to the scope: circuit loading and susceptibility to external pickup.

Circuit Loading: This subject will be discussed in detail later, but circuit loading by the test equipment (scope-probe) is a combination of resistance and capacitance. Without the benefit of using an attenuator (10X) probe, the loading on the device under test (DUT) will be 1M ohm (the scope input resistance) and more than 15 picofarad (15pF), which is the typical scope input capacitance plus the stray capacitance of the hookup wire.

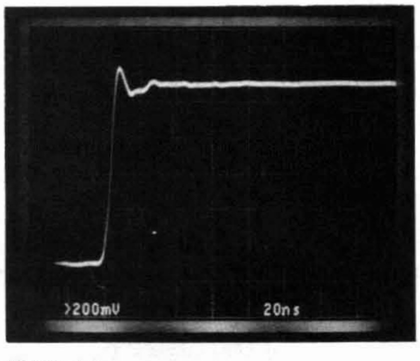


Figure 1-1

Figure 1-1 shows what a "real world" signal from a 500 ohm impedance source looks like when loaded by a 10M ohm, 10 pF probe: the scope-probe system is 300MHz. Observed risetime is 6 nSec.

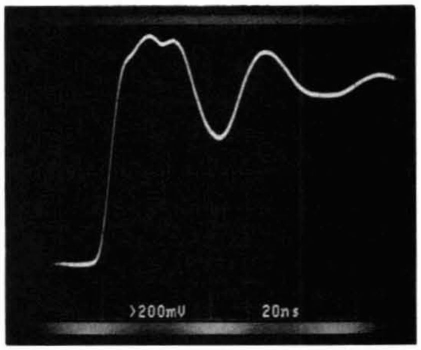


Figure 1-2

Figure 1-2 shows what happens to the same signal when it is accessed by two 2-meter lengths of hookup wire: loading is 1M ohm (the scope input resistance) and about 20 pF (the scope input capacitance, plus the stray capacitance of the wires). Observed risetime has slowed to 10 nSec and the transient response of the system has become unusable.

Susceptibility to External Pickup: An unshielded piece of wire acts as an antenna for the pickup of external fields, such as line frequency interference, electrical noise from fluorescent lamps, radio stations and signals from nearby equipment. These signals are not only injected into the scope along with the wanted signal, but can also be injected into the device under test (DUT) itself.

The source impedance of the DUT has a major effect on the level of interference signals developed in the wire. A very low source impedance would tend to shunt any induced voltages to ground, but high frequency signals could still appear at the scope input and mask the wanted signal. The answer, of course, is to use a probe which, in addition to its other features, provides coaxial shielding of the center conductor and virtual elimination of external field pickup.

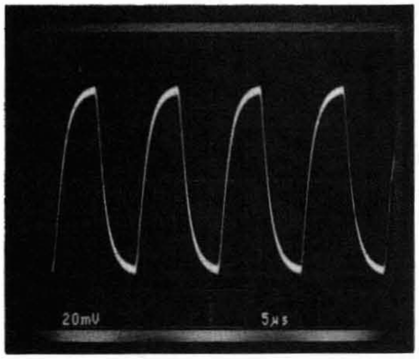


Figure 1-3

Figure 1-3 shows what a low level signal from a high impedance source (100mV from 100K ohm) looks like when accessed by a 300MHz scope-probe system. Loading is 10M ohm and 10 pF. This is a true representation of the signal, except that probe resistive loading has reduced the amplitude by about 1%: the observed high frequency noise is part of the signal at the high impedance test point and would normally be removed by using the BW (bandwidth) limit button on the scope. (See Figure 1-4.)

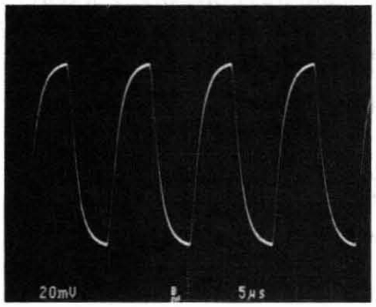


Figure 1-4

If we look at the same test point with our pieces of wire, two things happen. The amplitude drops due to the increased resistive and capacitive loading, and noise is added to the signal because the hookup wire is completely unshielded. (See Figure 1-5)

Most of the observed noise is line frequency interference from fluorescent lamps in the test area.

Probably the most annoying effect of using hookup wire to observe high frequency signals is its unpredictability. Any touching or rearrangement of the leads can produce different and nonrepeatable effects on the observed display.

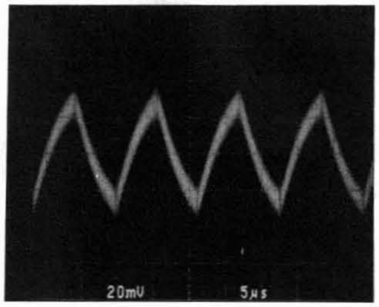


Figure 1-5

Benefits of using probes

Not all probes are alike and, for any specific application, there is no one ideal probe; but they share common features and functions that are often taken for granted.

Probes are convenient. They bring a scope's vertical amplifier to a circuit. Without a probe, you would either need to pick up a scope and attach it to a circuit, or pick up the circuit and attach it to the scope. Properly used, probes are convenient, flexible and safe extensions of a scope.

Probes provide a solid mechanical connection. A probe tip, whether it's a clip or a fine solid point, makes contact at just the place you want to examine.

Probes help minimize loading. To a certain extent, all probes load the DUT—the source of the signal you are measuring. Still, probes offer the best means of making the connections needed. A simple piece of wire, as we have just seen, would severely load the DUT; in fact, the DUT might stop functioning altogether.

Probes are designed to minimize loading. Passive, non-attenuating 1X probes offer the highest capacitive loading of any probe type—even these, however, are designed to keep loading as low as possible.

Probes protect a signal from external interference. A wire connection, as described earlier, in addition to loading the circuit, would act as an antenna and pick up stray signals such as 60Hz power, CBers, radio and TV stations. The scope would display these stray signals as well as the signal of interest from the DUT.

Probes extend a scope's signal amplitude-handling ability. Besides reducing capacitive and resistive loading, a standard passive 10X (ten times attenuation) probe extends the on-screen viewability of signal amplitudes by a factor of ten.

A typical scope minimum sensitivity is 5V/division. Assuming an eight-division vertical graticule, a 1X probe (or a direct connection) would allow on-screen viewing of 40V p-p maximum. The standard 10X passive probe provides 400V p-p viewing. Following the same line, a 100X probe should allow 4kV on-screen viewing. However, most 100X probes are rated at 1.5kV to limit power dissipation in the probe itself.

Check the specs. Bandwidth is the probe specification most users look at first, but plenty of other features also help to determine which probe is right for your application. Circuit loading, signal aberrations, probe dynamic range, probe dimensions, environmental degradation and ground-path effects will all impact the probe selection process, as discussed in the pages that follow.

By giving due consideration to probe characteristics that your application requires, you will achieve successful measurements and derive full benefit from the instrument capabilities you have at hand.

How probes affect your measurements

Probes affect your measurements by loading the circuit you are examining. The loading effect is generally stated in terms of impedance at some specific frequency, and is made up of a combination of resistance and capacitance.

Source Impedance. Obviously, source impedance will have a large impact on the net affect of any specific probe loading. For example, a device under test with a near zero output impedance would not be affected in terms of amplitude or risetime to any significant degree by the use of a typical 10X passive probe. However, the same probe connected to a high impedance test point, such as the collector of a transistor, could affect the signal in terms of risetime and amplitude.

Capacitive Loading. To illustrate this effect, let's take a pulse generator with a very fast risetime. If the initial risetime was assumed to be zero (tr = 0), the output tr of the generator would be limited by the associated resistance and capacitance of the generator. This integration network produces an output rise time equal to 2.2 RC. This limitation is derived from the universal time-constant curve of a capacitor.

Figure 1-6 shows the effect of internal source resistance and capacitance on the equivalent circuit. At no time can the output risetime be faster than 2.2 RC or 2.2 nSec.

If a typical probe is used to measure this signal, the probe's specified input capacitance and resistance is added to the circuit as shown in Figure 1-7.

Because the probe's 10M ohm resistance is much greater than the generator's 50 ohm output resistance, it can be ignored.

Figure 1-8 shows the equivalent circuit of the generator and probe, appling the 2.2 RC formula again. The actual risetime has slowed from 2.2 n Sec. to 3.4 nSec.

Percentage change in risetime due to the added probe tip capacitance:

$$\% \text{ change } \frac{tr_2 - tr_1}{tr_1} \times 100 = \frac{3.4 - 2.2}{2.2} \times 100 = 55\%$$

Another way of estimating the affect of probe tip capacitance on a source is to take the ratio of probe tip capacitance (marked on the probe compensation box) to the known or estimated source capacitance.

Using the same values:

$$\frac{C_{\text{probe tip}}}{C_1} \times 100 = \frac{11\text{pF}}{20\text{pF}} \times 100 = 55\%$$

To summarize, any added capacitance slows the source risetime when using high impedance passive probes. In general, the greater the attenuation ratio, the lower the tip capacitance. Here are some examples:

Probe	Attenuation	Tip Capacitance
Tektronix P6101A	X1	54 pF
Tektronix P6105A	X10	11.2 pF
Tektronix P6007	X100	2 pF

Capacitive Loading: Sinewave. When probing continuous wave (CW) signals, the probe's capacitive reactance at the operating frequency must be taken into account.

The total impedance, as seen at the probe tip, is designated Rp and is a function of frequency. In addition to the capacitive and resistive elements, designed-in inductive elements serve to offset the pure capacitive loading to some degree.

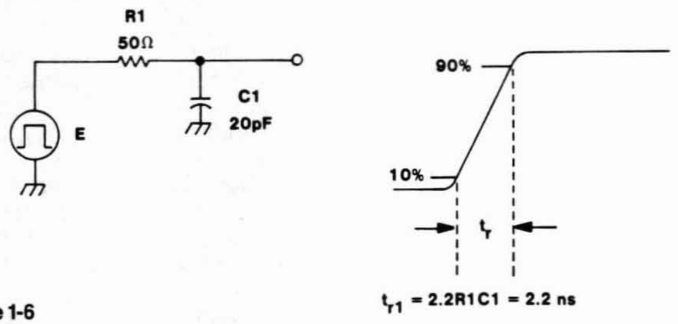


Figure 1-6

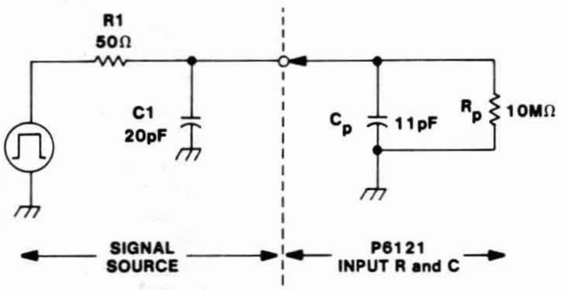


Figure 1-7

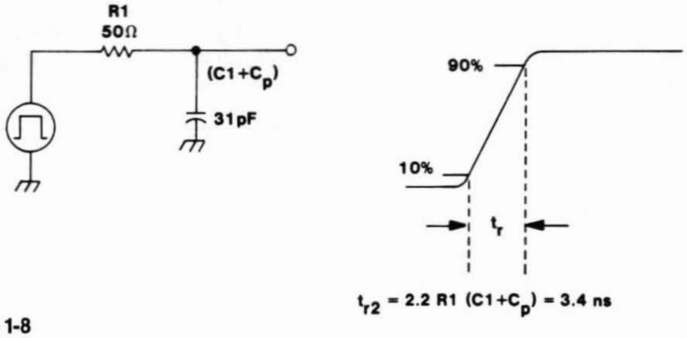


Figure 1-8

Curves showing typical input impedance vs frequency, or typical Xp and Rp vs frequency are included in most Tektronix probe instruction manuals. Figure 1-9A shows the typical input impedance and phase relationship vs frequency of the Tektronix P6203 Active Probe. Note that the 10 KΩ input impedance is maintained to almost 10 MHz by careful design of the associated resistive, capacitive and inductive elements.

Figure 1-9B shows a plot of Xp and Rp vs frequency for a typical 10 MΩ passive probe. The dotted line (Xp) shows capacitive reactance vs frequency. The total loading is again offset by careful design of the associated R, C and L elements.

If you do not have ready access to the information and need a worst-case guide to probe loading, use the following formula:

$$Xp = \frac{1}{2\pi FC}$$

Xp = Capacitive reactance (ohms)
F = Operating frequency
C = Probe tip capacitance (marked on the probe body or compensation box.)

For example, a standard passive 10M ohm probe with a tip capacitance of 11 pF will have a capacitive reactance (Xp) of about 290 ohm at 50MHz.

Depending, of course, on the source impedance, this loading could have a major effect on the

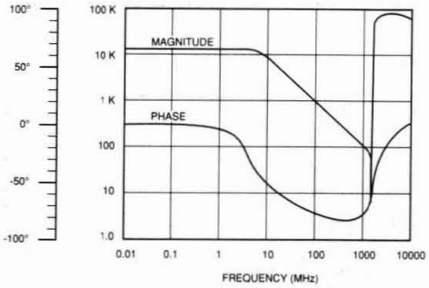


Figure 1-9A. Typical Input Impedance vs Frequency for the Tektronix P6203 Active Probe

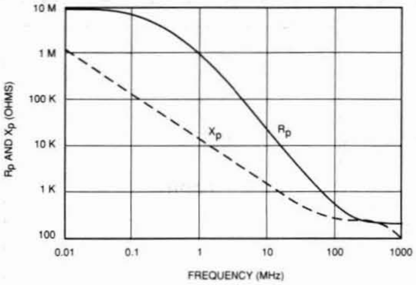


Figure 1-9B. Xp and Rp vs Frequency for a Typical 10 MΩ Passive Probe

signal amplitude (by simple divider action), and even on the operation of the circuit itself.

Resistive Loading. For all practical purposes, a 10X, 10M ohm passive probe has little effect on today's circuitry in terms of resistive loading, however, they do carry a trade-off in terms of relatively high capacitive loading as we have previously discussed.

Low Z Passive Probes. A "Low Z" passive probe offers very low tip capacitance at the expense of relatively high resistive loading. A typical 10X "50 ohm" probe has an input C of about 1 pF and a resistive loading of 500 ohm: Figure 1-10 shows the circuit and equivalent model of this type of probe.

This configuration forms a high frequency 10X voltage divider because, from transmission line theory, all that the 450 ohm tip resistor "sees" looking into the cable is a pure 50 ohm resistance, no C or L component. No low frequency compensation is necessary because it is not a capacitive divider. Low Z probes are typically high bandwidth (up to 3.5GHz and risetimes to 100 pS) and are best suited for making risetime and transit-time measurements. They can, however, affect the pulse amplitude by simple resistive divider action between the source and the load (probe). Because of its resistive loading effects, this type of probe performs best on 50 ohm or lower impedance circuits under test.

Note also that these probes operate into 50 ohm scope inputs only. They are typically teamed up with fast (500MHz to 1GHz) real time scopes or with scopes employing the sampling principle.

Bias-Offset Probes. A Bias/Offset probe is a special kind of Low Z design with the capability of providing a variable bias or offset voltage at the probe tip.

Bias/Offset probes like the Tektronix P6230 or P6231 are useful for probing high speed ECL circuitry, where resistive loading could upset the operating point. These special probes are fully described in Part 3; under Advanced Probing Techniques.

The Best of Both Worlds. From the foregoing, it can be seen that the totally "non-invasive" probe does not exist. However, one type of probe comes close—the active probe.

Active probes are discussed in the Tutorial section, but in general, they provide low resistance loading (10M ohm) with very low capacitive loading (1 to 2 pF). They do have trade-offs in terms of limited dynamic range, but under the right conditions, do indeed offer the best of both worlds.

Bandwidth. Bandwidth is the point on an amplitude versus frequency curve where the measurement system is down 3dB from a starting (reference) level. Figure 1-11 shows a typical response curve of an oscilloscope system.

Scope vertical amplifiers are designed for a Gaussian roll-off at the high end (a discussion of Gaussian response is beyond the scope of this primer). With this type of response, risetime is approximately related to bandwidth by the following equation:

$$T_r = \frac{.35}{BW} \quad \text{or, for convenience:}$$

$$\text{Risetime (nanoseconds)} = \frac{350}{\text{Bandwidth (MHz)}}$$

It is important to note that the measurement system is −3dB (30%) down in amplitude at the specified bandwidth limit.

Figure 1-12 shows an expanded portion of the −3dB area. The horizontal scale shows the input frequency derating factor necessary to obtain accuracies better than 30% for a specific bandwidth scope. For example, with no derating, a "100MHz" scope will have up to a 30% amplitude error at 100MHz (1.0 on the graph). If this scope is to have an amplitude accuracy better than 3%, the input frequency must be limited to about 30MHz (100MHz X .3).

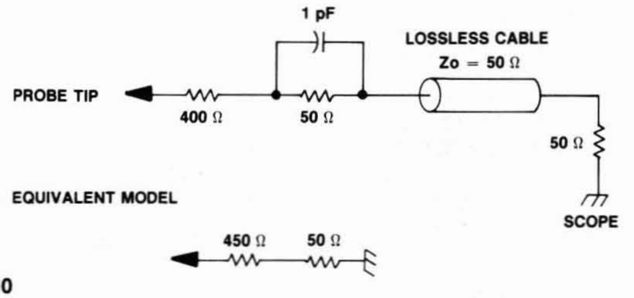


Figure 1-10

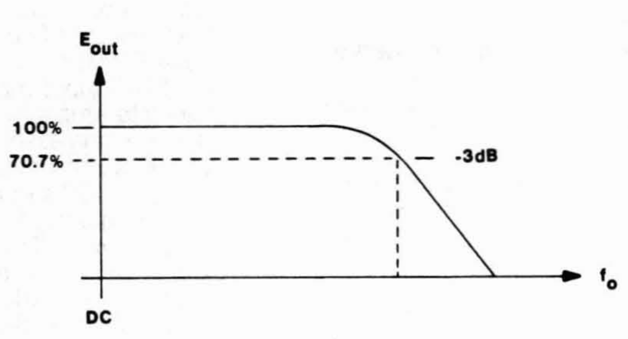


Figure 1-11

For making amplitude measurements within 3% at a specific frequency, choose a scope with at least four times the specified bandwidth as a general rule of thumb.

Probe Bandwidth. All probes are ranked by bandwidth. In this respect, they are like scopes or other amplifiers that are ranked by bandwidth. In these cases we apply the square root of the sum of the squares formula to obtain the "system risetime." This formula states that:

$$\text{Risetime system} = \sqrt{Tr^2\ \text{displayed} - Tr^2\ \text{source}}$$

Passive probes do not follow this rule and should not be included in the square root of the sum of the squares formula.

Tektronix provides a probe bandwidth ranking system that specifies "the bandwidth (frequency range) in which the probe performs within its specified limits. These limits include: total abberrations, risetime and swept bandwidth."

Both the source and the measurement system shall be specified when checking probe specifications (see Test Methods, this page).

In general, a Tektronix "100MHz" probe provides 100MHz performance (−3dB) when used on a compatible 100MHz scope. In other words, it provides full scope bandwidth **at the probe tip.**

However, not all probe/scope systems can follow this general rule. Refer to the sidebar, "Scope Bandwidth at the Probe Tip?."

Figure 1-13 shows examples of Tektronix scopes and their recommended passive probes.

Test Methods: As with all specifications, matching test methods must be employed to obtain specified performance. In the case of bandwidth and risetime measurements, it is essential to connect the probe to a properly terminated source. Tektronix specifies a 50 ohm source terminated in 50 ohm, making this a 25 ohm source impedance. Furthermore, the probe must be connected to the source via a proper probe tip to BNC adaptor. (Figure 1-14).

Figure 1-14 shows an equivalent circuit of a typical setup. The displayed risetime should be a 3.5 nSec or faster.

Figure 1-15 shows an equivalent circuit of a typical passive probe connected to a source.

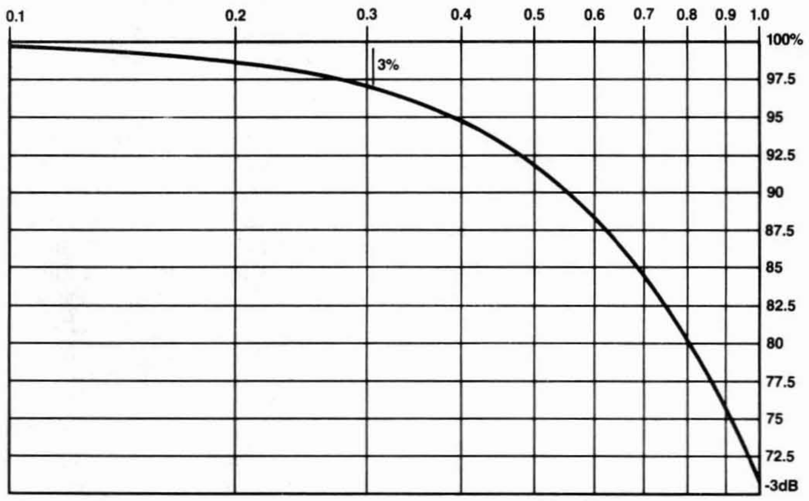


Figure 1-12

SCOPE	BW (1 MΩ input)	PROBE	BW	SYSTEM
2235	100	P6109	150	100
2245A	100	P6109	150	100
2246A	100	P6109	150	100
2445B	150	P6133 Opt 25	150	150
485	350	P6106A	250	250
2465B	400	P6137	400	400
2467B	400	P6137	400	400

Figure 1-13

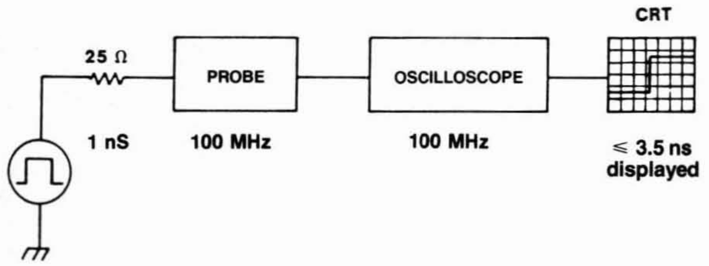


Figure 1-14

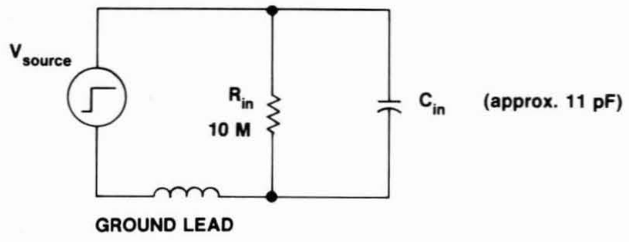


Figure 1-15

Scope Bandwidth at the Probe Tip ?

Most manufacturers of general-purpose oscilloscopes that include standard accessory probes in the package, promise and deliver the advertised scope bandwidth **at the probe tip.**

For example, the Tektronix 2465B 400 MHz Portable Oscilloscope and its standard accessory P6137 Passive Probes deliver 400 MHz (−3db) at the probe tip.

However, not all high performance scopes can offer this feature, even when used with their recommended passive probes. For example, the Tektronix 11A32 400 MHz plug-in has a system bandwidth of 300 MHz when used with its recommended P6134 passive probe. This is simply because even the highest impedance passive probes are limited to about 300 to 350 MHz, while still meeting their other specifications.

It is important to note that the above performance is only obtainable under strictly controlled, and industry recognized conditions; which states that the signal must originate from a 50 Ω back-terminated source (25 Ω), and that the probe must be connected to the source by means of a probe tip to BNC (for other) adaptor.

This method ensures the shortest ground path and necessary low impedance to drive the probe's input capacitance, and to provide the specified bandwidth at the signal acquisition point, the probe tip.

Real-world signals rarely originate from 25 Ω sources, so less than optimum transient response and bandwidth should be expected when measuring higher impedance circuits.

How ground leads affect measurements

A ground lead is a wire that provides a local ground-return path when you are measuring any signal. An inadequate ground lead (one that is too long or too high in inductance) can reduce the fidelity of the high frequency portion of the displayed signal.

What grounding system to use. When making **any** measurement, some form of ground path is required to make a basic two-terminal connection to the DUT. If you want to check the presence or absence of signals from low-frequency equipment, **and** if the equipment is line-powered and plugged into the same outlet system as the scope, then the common 3-wire ground system provides the signal ground return. However, this indirect route adds inductance in the signal path—it can also produce ringing and noise on the displayed signal and is not recommended.

When making any kind of absolute measurement, such as amplitude, risetime or time delay measurements, you should use the shortest grounding path possible, consistent with the need to move the probe among adjacent test points. The ultimate grounding system is an in-circuit ECB (etched circuit board) to probe tip adaptor. Tektronix can supply these for either miniature, compact or subminiature probe configurations.

Figure 1-15 shows an equivalent circuit of a typical passive probe connected to a source. The ground lead L and C_{in} form a series resonant circuit with only 10M ohm for damping. When hit with a pulse, it will ring. Also, excessive L in the ground lead will limit the changing current to C_{in}, limiting the risetime.

Without going into the mathematics, an 11pF passive probe with a 6-inch ground lead will ring at about 140MHz when excited by a fast pulse. As the ring frequency increases, it tends to get outside the passband of the scope and is greatly attenuated. So to increase the ring frequency, use the shortest ground lead possible and use a probe with the lowest input C.

Probe Ground Lead Effects. The effect of inappropriate grounding methods can be demonstrated several ways. Figs. 1-16A, B and C show the effect of a 12-inch ground lead when used on various bandwidth scopes.

In Figure 1-16A, the display on the 15MHz scope looks OK because the ringing abberations are beyond the passband of the instrument and are greatly attenuated. Figs. 1-16B and C show what the same signal looks like on 50MHz and 100MHz scopes.

Even with the shortest ground lead, the probe-DUT interface has the **potential** to ring. The potential to ring depends on the **speed** of the step function. The ability to **see** the resultant ringing oscillation depends on the scope system bandwidth.

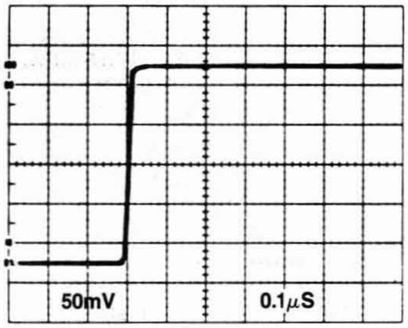


Figure 1-16A

Scope BW = 15MHz
Ground lead 12 inches

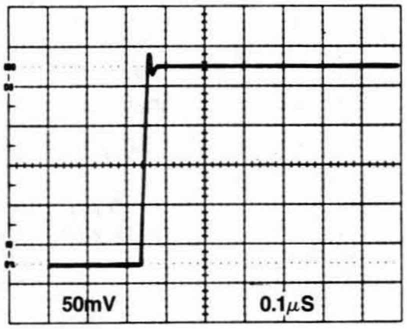


Figure 1-16B

Scope BW = 50MHz
Ground lead 12 inches

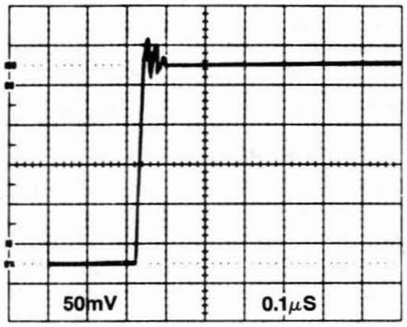


Figure 1-16C

Scope BW = 100MHz
Ground lead 12 inches

Figs. 1-17A through F show the effects of various grounding methods and ground lead lengths on the display of a very fast pulse. This is the most critical way of looking at ground lead effects: we used a fast pulse, with a risetime of about 70 pico seconds and a fast (400 MHz) scope with a matching P6137 probe.

Fig. 1-17A shows the input pulse under the most optimum conditions when using 50 ohm coax cable. Scope: the Tektronix 2465B with 50 ohm input and 50 ohm cable from a 50 ohm source. Displayed risetime is < 1 nSec.

Fig. 1-17B shows the same signal when using the scope-probe combination under the most optimum conditions. A BNC to probe adaptor or an in-circuit test jack provides a coaxial ground that surrounds the probe ground ring. This sytem provides the shortest probe ground connection available. Displayed risetime is < 1nSec.

Figures 1-17C through E show the effects of longer ground leads on the displayed signal. Fig. 1-17C shows the effect of a short semi-flexible ground connection, called a "Z" lead. Finally, Fig. 1-17F shows what happens when no probe ground lead is used.

How probe design affects your measurements

Probes are available in a variety of sizes, shapes and functions, but they do share several main features: a probe head, coaxial cable and either a compensation box or a termination.

The probe head contains the signal-sensing circuitry. This circuitry may be passive (such as a 9-M ohm resistor shunted by an 11 pF capacitor in a passive voltage probe or a 125-turn transformer secondary in a current probe); or active (such as a source follower or Hall generator) in a current probe or active voltage probe.

The coaxial cable couples the probe head output to the termination. Cable types vary with probe types.

The termination has two functions:

- to terminate the cable in its characteristic impedance.
- to match the input impedance of the scope.

The termination may be passive or active circuitry. For easy connection to various test points, many probes feature interchangeable tips and ground leads.

A unique feature of most Tektronix probes is the Tektronix-patented coaxial cable that has a resistance-wire center conductor. This distributed resistance suppresses ringing caused by impedance mismatches between the cable and its terminations when you're viewing fast pulses on wideband scopes.

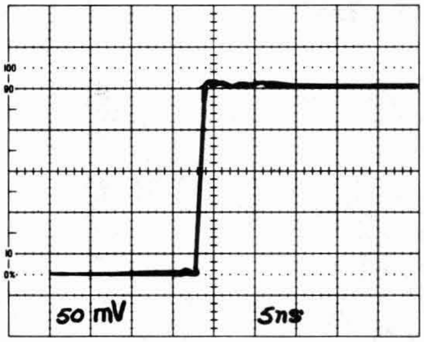


Figure 1-17A

50 ohm Source/Cable/2465B/50 ohm input

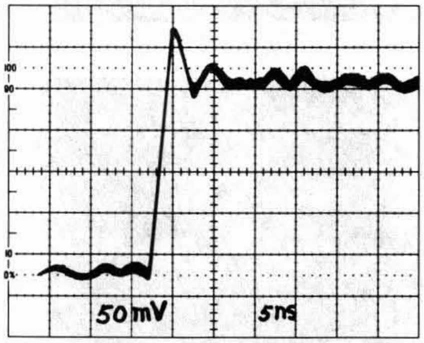


Figure 1-17C

P6137 - Probe/Z Ground Tr = 1.5 nS

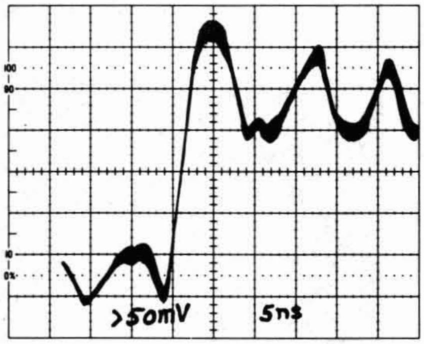


Figure 1-17E

P6137 - Probe/6" Gnd Lead Tr = 4 nS

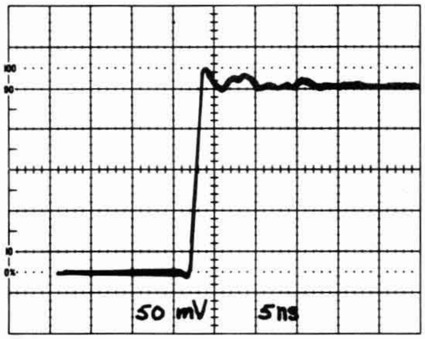


Figure 1-17B

P6137-BNC/Probe Adaptor Tr = < 1nS

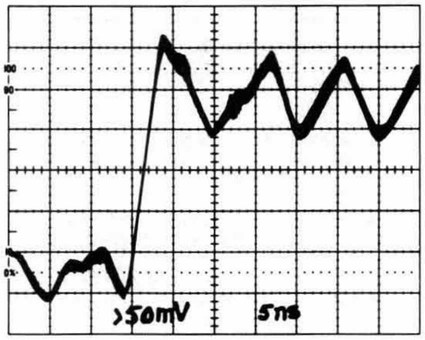


Figure 1-17D

P6137 - Probe/3" Gnd Lead Tr = 4 nS

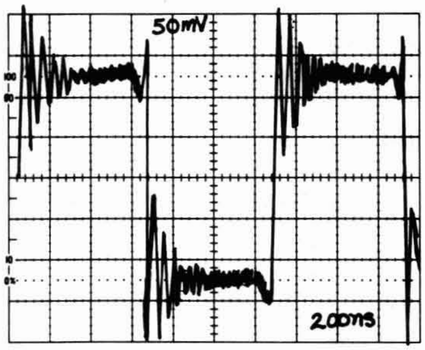
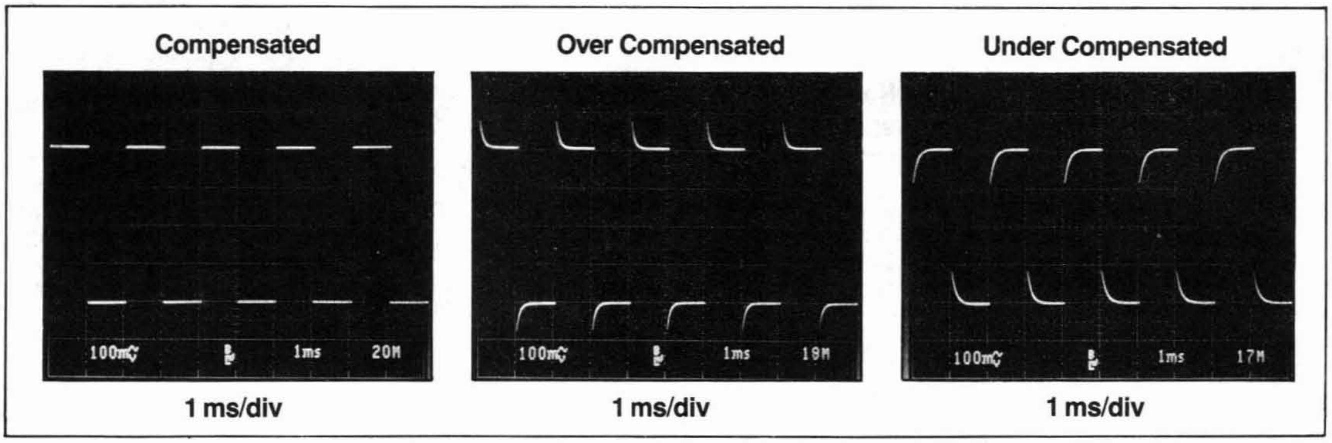


Figure 1-17F

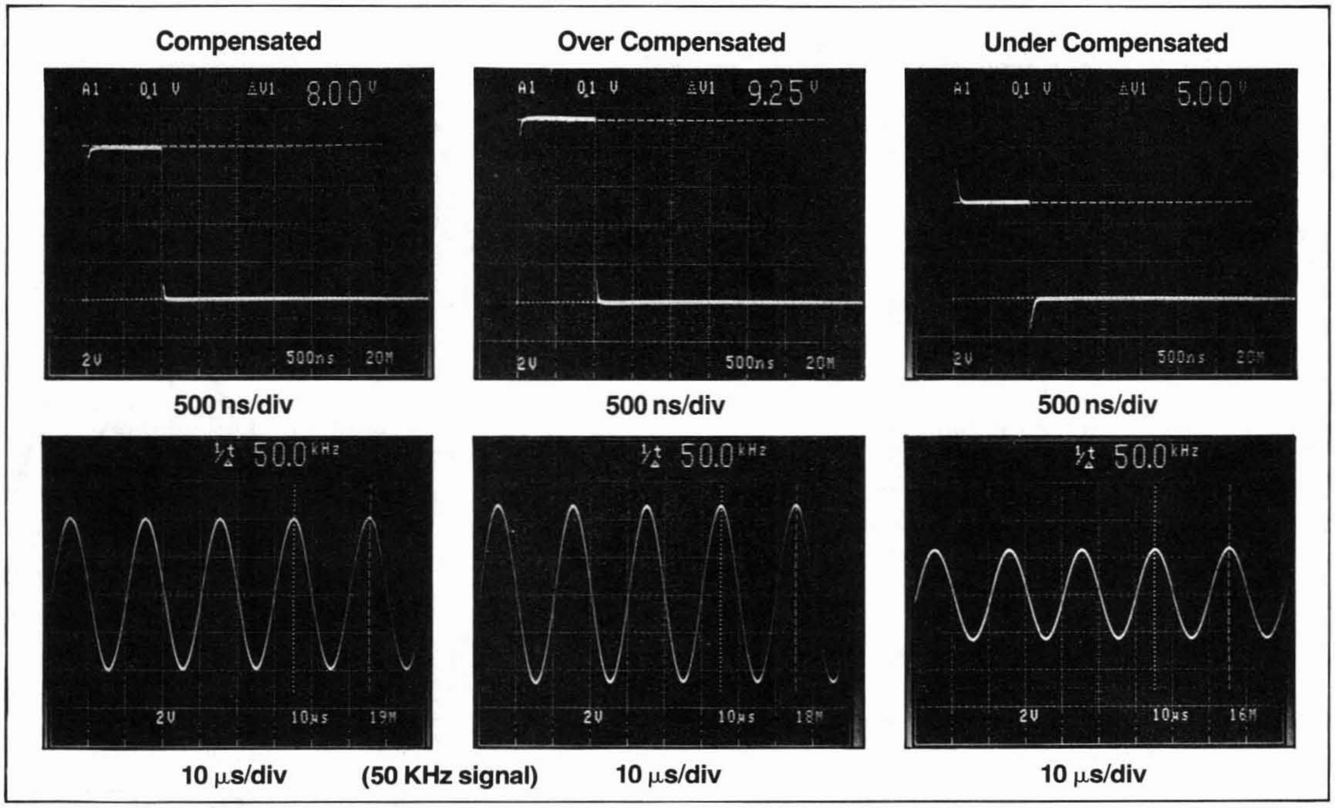
No Ground Lead

PART II: EFFECTS OF PROBE COMPENSATION — UNDERSTANDING PROBES



Compensated 1 ms/div | Over Compensated 1 ms/div | Under Compensated 1 ms/div

Figure 2-1. Shows the display associated with correctly and incorrectly compensated probes.



Compensated 500 ns/div | Over Compensated 500 ns/div | Under Compensated 500 ns/div

10 μs/div (50 KHz signal) 10 μs/div 10 μs/div

Figure 2-2. Shows the effects on faster pulses and sinewaves when an incorrectly compensated probe is used. Note that the much faster sweep rates used to correctly view these waveforms does not warn the user of an adjustment problem.

Tips on using probes

Compensating the probe. The most common mistake in making scope measurements is forgetting to compensate the probe. Improperly compensated probes can distort the waveforms displayed on the scope. The probe should be compensated as it will be used when you make the measurement.

The basic low frequency compensation (L.F. comp.) procedure is simple:

- Connect the probe tip to the scope CALIBRATOR (refer to Scope Calibrator Outputs.)
- Switch the channel 1 input coupling to dc.
- Turn on the scope and move the CH1 VOLTS/DIV switch to produce about four divisions of vertical display.
- Set the sweep rate to 1mSec/div. (for line-driven calibrators see Scope Calibrators Outputs.)
- Use a non-metalic alignment tool to turn the compensation adjust until the tops and bottoms of the square-wave are flat.

PART III: ADVANCED PROBING TECHNIQUES

Introduction:

In Part III we will examine some of the more advanced probing techniques associated with accessing high frequency and complex signals, such as fast ECL, waveforms offset from ground, and true differential signals.

Most of the techniques to be described follow recommended practices outlined throughout this Booklet, and to a large extent involve proper grounding techniques.

Workers in the audio and relatively low frequency fields may wonder what all the fuss is about, and may comment "I don't have any of these problems," or "I can't see any difference when I use different ground lead lengths, or even when I leave the ground lead completely off?"

In order to see abberrations caused by poor grounding techniques, two conditions must exist:

1. The scope system bandwidth must be great enough to handle the high frequency content existing at the probe tip.
2. The input signal must contain enough high frequency information (fast risetime) in order to cause ringing and aberrations due to poor grounding techniques.

To illustrate these points, a 20 MHz scope was used to access a 1.7 nS pulse by using a standard passive probe with a 6″ ground lead.

NOTE: A fast scope can be made into a slow scope simply by pushing the Bandwidth Limit (B/W Limit) button ?.

We used a 350 MHz scope with a 20 MHz B/W Limit function.

Figure 3-1 shows the resultant clean displayed pulse with a risetime of about 20 nS (17.5 MHz).

This display does not represent conditions actually existing at the probe tip, because the 20 MHz measurement system cannot "see" what's really happening.

Figure 3-2 shows what the probe tip signal really looks like when a 350 MHz scope is used under the same conditions (B/W Limit off).

The observed risetime has improved to about 2 nS, but we have serious problems with ringing and aberrations, caused by incorrect grounding techniques.

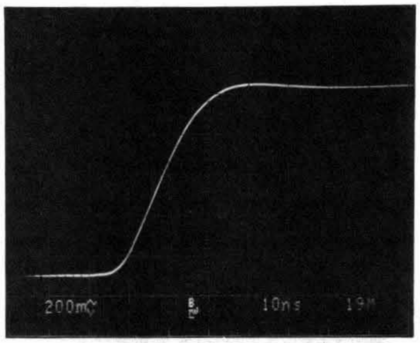


Figure 3-1. Resultant clean, but incorrect display caused by inadequate scope system bandwidth.

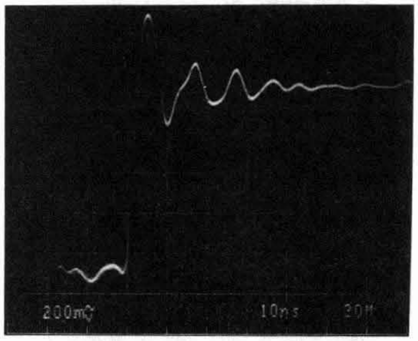


Figure 3-2. The same input signal as shown in figure 3-1, but accessed by a 350 MHz system bandwidth scope (same 6″ ground lead).

The problem can now be seen because the scope system bandwidth is great enough to pass and display all the frequency content existing at the probe tip.

To further stress the points about high frequency content and scope system bandwidth, let's assume an input pulse with a risetime of about 20 nS. If the signal is accessed by the same probe /6″ ground lead /350 MHz system, it would look very much like the display in figure 3-1.

There would be no frequency content higher than 17.5 MHz (20 nS Tr). The 6″ ground lead would not ring, and would therefore be the correct choice for accessing this relatively slow signal.

In the following sections we discuss how to recognize signal acquisition problems, and how to avoid them.

Techniques for probing ECL, high speed 50 Ω environments, and accessing true differential signals are also discussed.

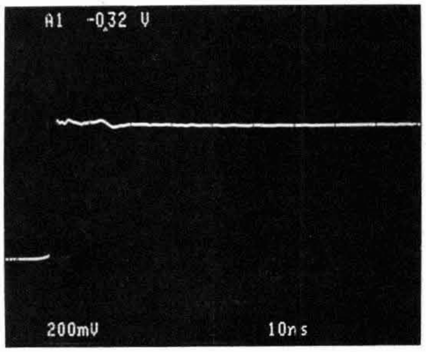


Figure 3-3. 1 nS Tr pulse accessed via an ECB to Probe Tip Adaptor (test point)

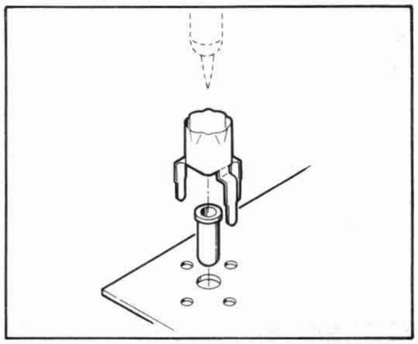


Figure 3-4. Typical ECB to Probe Tip Adaptor installation

Probe Ground Lead Effects. In Part I we discussed the basic need for probe grounding, and showed several different ways of looking at the effects of correct, and incorrect probe grounding.

In this section, we will expand upon these techniques and show how to identify problem areas.

When a probe (high Z, low Z, passive or active) is connected to the circuit under test via an ECB to Probe Tip Adaptor (test point), the coaxial environment existing at the probe tip is extended through the adaptor to the signal pick-off point, and to the ECB ground plane (or device ground).

Figure 3-3 shows what a typical 1 nS Tr pulse looks like when a suitable probe is connected to the circuit via an ECB to Probe Tip Adaptor.

Figure 3-4 shows a typical ECB to Probe Tip Adaptor (test point) installation.

These test points are available in three sizes to accept miniature, compact or sub-miniature series probes.

If a flexible ground lead is used in place of the ECB to Probe Tip Adaptor, the 1 nS Tr input step (with high frequency content up to 350 MHz) will cause the ground lead to ring at a frequency determined by the ground lead inductance and the probe tip and source capacitance.

Figure 3-5 shows the effect of using a 6″ ground lead to make the ground connection.

The ring frequency for the 6″ ground lead/probe tip C combination is 87.5 MHz. This signal is injected in series with the wanted signal and appears at the probe tip, as shown in figure 3-6.

Unfortunately, the problem is not this simple.

The probe's coaxial environment has been disrupted at the signal acquisition point by ground lead inductance, and is no longer correctly terminated (for high speed signal acquisition).

This abrupt transition leaves the probe's outer shield susceptible to ring frequency injection (the ground lead inductance is in series with the outer braid).

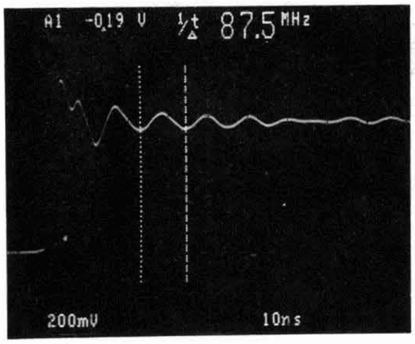


Figure 3-5. Effect of a 6″ ground lead on a 1 nS Tr input step.

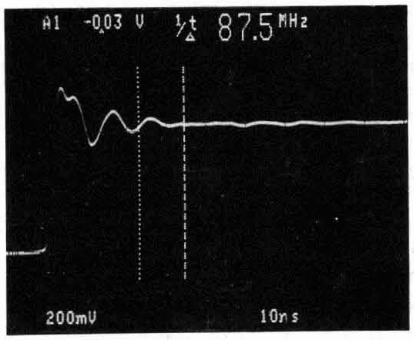


Figure 3-7. The same setup as in figure 3-5, except that the probe cable has been repositioned, and a hand has been placed over part of the probe cable.

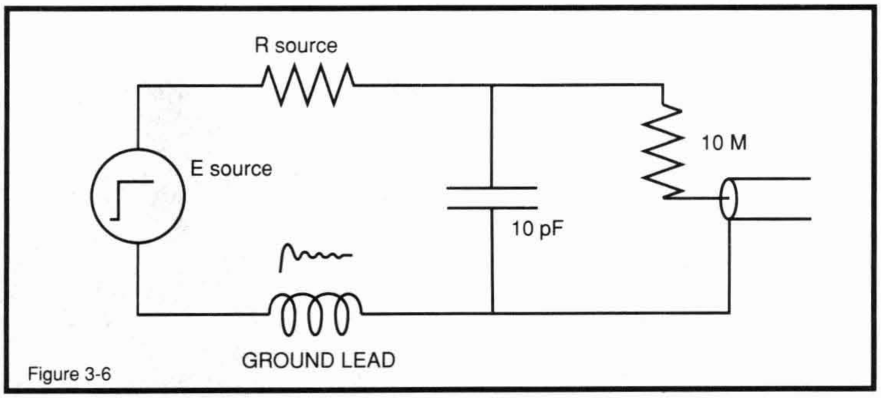


Figure 3-6. Equivalent circuit, ground lead inductance (excess inductance).

The now unterminated probe cable system develops reflections, which intermix with the ring frequency and the signal to produce a multitude of problems and unpredictable results.

Herein lies the key to the identification of ground lead problems.

Figure 3-7 shows exactly the same setup as in figure 3-5, except that the probe cable has been moved, and a hand has been placed over part of the probe cable.

KEY: If touching or moving the probe cable produces changes in the display, you have a probe grounding problem.

A correctly grounded (terminated) probe should be completely insensitive to cable positioning or touch.

Ground Lead Length. All things being equal, the shortest ground lead produces the highest ring frequency.

If the lead is very short, the ring frequency might be high enough to be outside the passband of the scope, and/or the input frequency content may not be high enough to stimulate the ground lead's resonant circuit.

In all cases, the shortest ground lead should be used, consistant with the need for probe mobility.

If possible, use 3″ or shorter ground leads, such as the Low Impedance Contact (Z Lead). These are supplied with the Tektronix P613X and P623X family or probes.

One final note. The correct probe grounding method depends on the signal's high frequency content, the scope system bandwidth, and the need for mobility between test points.

A 12″ ground lead may be perfect for many lower frequency applications. It will provide you with extra mobility, and nothing will be gained by using shorter leads.

If in doubt, apply the cable touch test outlined previously.

Ground Loop Noise Injection. Another form of signal distortion can be caused by signal injection into the grounding system.

This can be caused by unwanted current flow in the ground loop existing between the common scope and test circuit power line grounds, and the probe ground lead and cable.

Normally, all these points are, or should be at zero volts, and no ground current will flow.

However, if the scope and test circuit are on different building system grounds, there could be small voltage differences, or noise on one of the building ground systems.

The resulting current flow (at line frequency or noise frequency) will develop a voltage drop across the probe cable's outer shield, and be injected into the scope in series with the desired signal.

Inductive Pickup in Ground Loops. Noise can enter a common ground system by induction into long 50 Ω signal acquisition cables, or into standard probe cables.

Proximity to power lines or other current-carrying conductors can induce current flow in the probe's outer cable, or in standard 50 Ω coax. The circuit is completed through the building system common ground.

Prevention of Ground Loop Noise Problems. Keep all signal acquisition probes and/or cables away from sources of potential interference.

Verify the integrity of the building system ground.

If the problem persists, open the ground loop:

1. By using a Ground Isolation Monitor like the Tektronix A6901.
2. By using a power line isolation transformer on either the test circuit or on the scope.
3. By using an Isolation Amplifier like the Tektronix A6902B.
4. By using differential probes (see Differential Measurements).

NOTE: Never defeat the safety 3-wire ground system on either the scope or on the test circuit.

Do not "float" the scope, except by using an approved isolation transformer, or preferably, by using the Tektronix A6901 Ground Isolation Monitor.

The A6901 automatically reconnects the ground if scope ground voltages exceed ± 40 V.

Induced Noise in Probe Ground Leads. The typical probe ground lead resembles a single-turn loop antenna when it is connected to the test circuit.

The relatively low impedance of the test circuit can couple any induced voltages into the probe, as shown in figure 3-8.

High speed logic circuits can produce significant electro-magnetic (radiated) noise at close quarters.

If the probe ground lead is positioned too close to certain areas on the board, interference signals could be picked up by the loop antenna formed by the probe ground lead, and mix with the probe tip signal.

Question: Is this what my signal really looks like?

Moving the probe ground lead around will help identify the problem.

If the **noise level** changes, you have a ground lead induced noise problem.

A more positive way of identification is to disconnect the probe from the signal source and clip the ground lead to the probe tip.

Now use the probe/ground lead as a loop antenna and search the board for radiated noise.

Figure 3-9 shows what can be found on a logic board, **with the probe tip shorted to the ground lead.**

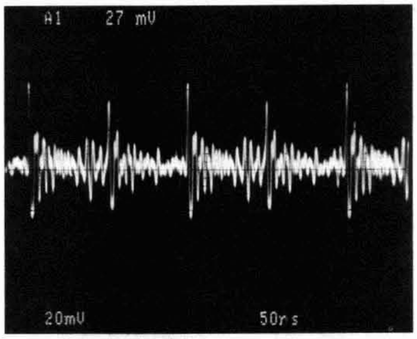


Figure 3-9. Induced noise in the probe ground loop (tip shorted to the ground clip).

This is radiated noise, induced in the single-turn loop and fed to the probe tip.

The significance of any induced or injected noise increases with reduced working signal levels, because the signal to noise ratio will be degraded. This is especially true with ECL, where signal levels are 1 V or less.

Prevention: If possible, use an ECB to Probe Tip Adaptor (test point). If not, use a Z Lead or short flexible ground lead.

Also, bunch the ground lead together to make the loop area as small as possible.

Bias Offset Probes. A Bias/Offset probe is a special kind of Low Z design with the capability of providing a variable bias or offset voltage at the probe tip.

Bias/Offset probes like the Tektronix P6230 and P6231 are useful for probing high speed ECL circuitry, where resistive loading could upset the operating point.

They are also useful for probing higher amplitude signals (up to ± 5 V), where resistive loading could affect the DC level at some point on the waveform.

Bias/Offset probes are designed with a tip resistance of 450 Ω (10X). When these probes are connected into a 50 Ω environment, this loading results in a 10% reduction in peak to peak source amplitude. This round-figure loading is more convenient to handle than that produced by a standard 500 Ω (10 X) Low Z probe, which would work out at 9.09% under the same conditions.

It is important to note that bias/offset probes always present a 450 Ω resistive load to the source, regardless of the bias/offset voltage selected.

The difference between bias/offset and standard Low Z probes lies in their ability to null current flow **at some specific and selectable point** on the input waveform (within ± 5 V).

To see how bias/offset probes work, let's take a typical 10 × 500 Ω Low Z probe and connect it in the circuit shown in figure 3-10.

By taking a current flow approach we find that at one point on the waveform the source voltage is − 4 V, therefore the load current will be;

$$I = ER = 4/Rs + Rp + R\,scope = 4/550 = 7.27\ mA.$$

Therefore the voltage drop across the 50 Ω source resistance (Rs) will be;

$$E = IR = 7.27 \times 10^{-3} \times 50 = 0.363\ V$$

And the measured pulse amplitude will be −4 −0.363 = 3.637 V (E dut), or about 9% down from its unloaded state.

If we substitute the 500 Ω Low Z probe with a 450 Ω bias/offset probe, the circuit will look like figure 3-11.

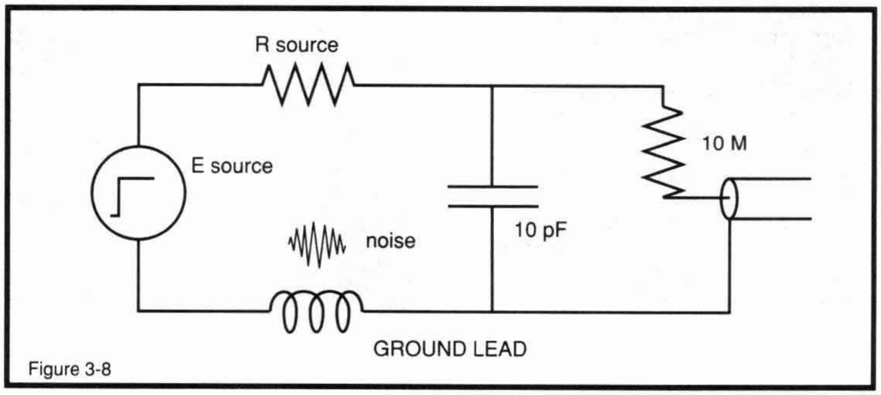


Figure 3-8

Figure 3-8. Equivalent Circuit. Ground Lead Induced Noise.

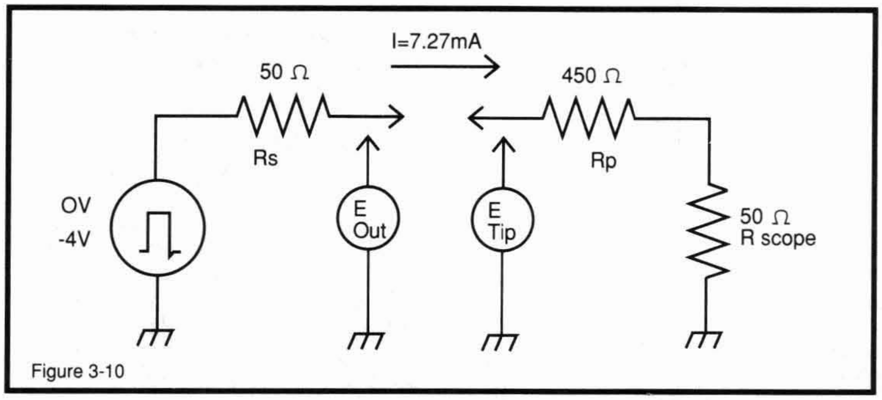


Figure 3-10

Figure 3-10. Low Z 10X 500 Ω probe connected to a 50 Ω source.

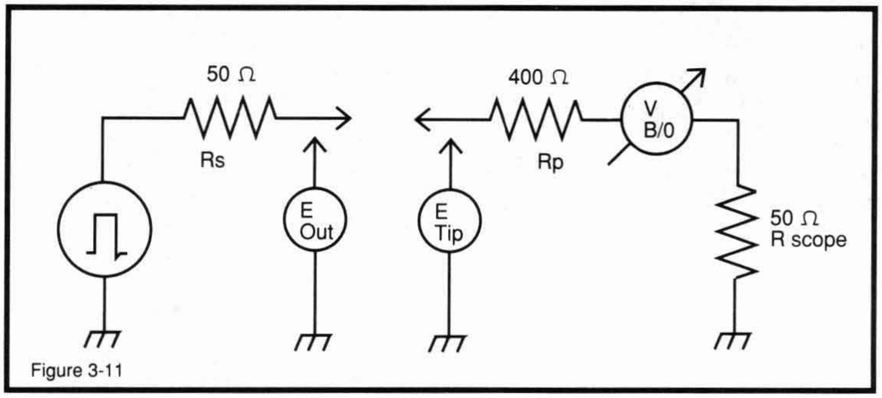


Figure 3-11

Figure 3-11. A 450 Ω Bias/Offset probe connected to a 50 Ω source.

With the bias/offset adjusted for 0 V, the effect on the circuit will be similiar to a 500 Ω Low Z probe, except for the small resistive change.

Figure 3-12 shows the source waveform acquired by a 10 M Ω probe.

Figure 3-13 shows the effect on the waveform when the 450 Ω probe is added.

As expected, the pulse amplitude has reduced from −4 V to 3.60 V, or exactly 10% down.

Figure 3-14 shows the effect of adjusting the offset to −4 V. The −4 V bias opposes the signal at the −4 V level and results in zero current flow, and the source is effectively unloaded **at this point.**

However, when the signal returns to ground level, there is a 4 V differential between the top of the pulse and the bias/offset source. Current will flow, and Ohms Law will dictate that the top of the pulse will go negative by −40 mV (10%).

Sometimes it is desirable to adjust the offset mid-way between the peak to peak excursions. This distributes the effect of resistive loading between the two voltage swings.

Figure 3-15 shows the effect of adjusting the bias/offset to −2 V. Current flow will be the same for both signal swings, and they will be equally down by 5%, for a total of 10%.

Summary:

1. Bias/Offset probes can be adjusted (within ± 5 V) to provide zero resistive (effective) loading at one selected point on the input waveform.
2. Bias/Offset probes can be used to simulate the effect of pull-up or pull-down voltages (within ± 5 V) on the circuit under test (voltage source impedance is 450 Ω).
3. Bias/Offset probes always present a total resistive load of 450 Ω, and reduce the peak to peak amplitude of 50 Ω sources by 10%.
4. For simplicity, we have ignored the effects of capacitive loading. Typically, Bias/Offset probes have less than 2 pF tip C.

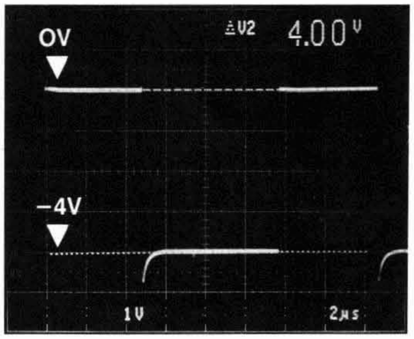


Figure 3-12. Unloaded negative-going 4 V pulse acquired by a 10 M Ω probe.

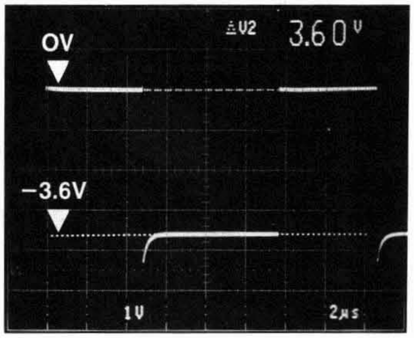


Figure 3-13. Effect of connecting a 450 Ω Bias/Offset probe (offset = 0 V). Minus level has been reduced by 10%.

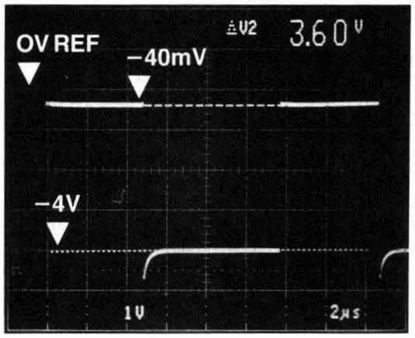


Figure 3-14. Bias/Offset adjusted for −4 V. Signal current at the −4 V level is zero. Current flow at ground level is maximum. Peak to peak amplitude remains the same (10% down).

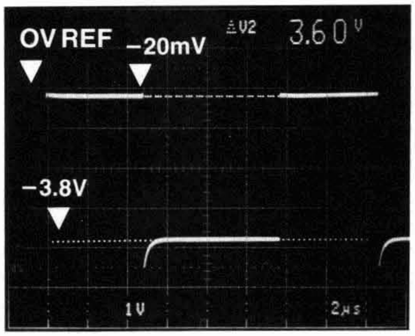


Figure 3-15. Bias/Offset adjusted for −2 V. Load current distributed between the negative and positive-going swings. Peak to peak amplitude remains the same (10% down).

Bias/Offset probes like the Tektronix P6230 or P6231 have bandwidths to 1.5 GHz, 450 Ω input R, and 1.3 pF (P6230), or 1.6 pF (P6231) input C.

They provide offset voltages of ± 5 V DC, and function with 1 M Ω or 50 Ω input systems (P6231, 50 Ω only).

The P6230 obtains operating power, either from the scope itself, or from the Tektronix 1101A or 1102 Power Supply.

The P6231 is designed to operate with the Tektronix 11000 Series scopes, and obtains operating power and bias/offset from the scope. Offset is selectable from the mainframe touch screen.

Differential Probing Techniques. Accessing small signals elevated from ground, either at an AC level or a combination of AC and DC, requires the use of differential probes and a differential amplifier system.

One of the problems associated with differential measurements is the maintenance of high common mode rejection ratio (CMRR) at high common mode frequencies.

Poor common mode performance allows a significant portion of the common (elevated) voltage to appear across the differential probe's inputs. If the common mode voltage is pure DC, the result may only be a displayed baseline shift. However, if the common mode voltage is AC, or a combination of AC and DC, a significant portion may appear across the differential input and will mix with the desired signal.

Figure 3-16 shows the basic items necessary to make a differential measurement.

In this example two similar but un-matched passive probes are used. The probe ground leads are usually either removed or clipped together. They are **never** connected to the elevated DUT (device under test).

CMRR depends upon accurate matching of the probe-pair's electrical characteristics, including cable length. System CMRR can be no better than the differential amplifier's specifications, and in all cases, CMRR degrades as a function of frequency.

Figure 3-17 shows a simplified diagram of a DUT with a pulsed output of 1 V p-p floating on a 5 V p-p 20 MHz sinewave.

CMRR at 20 MHz is a poor 10:1 because of the un-matched probes.

Observed signal. (referred to probe input) = 1 V p-p pulse + (5 V p-p sine/10) = 1 V p-p pulse + 0.5 V p-p sine.

Figure 3-18a shows what the displayed waveform might look like under the conditions shown in figure 3-17.

In comparison, figures 3-18b and 3-18c show what the displayed signal might look like at CMRR's of 100:1 and 1000:1.

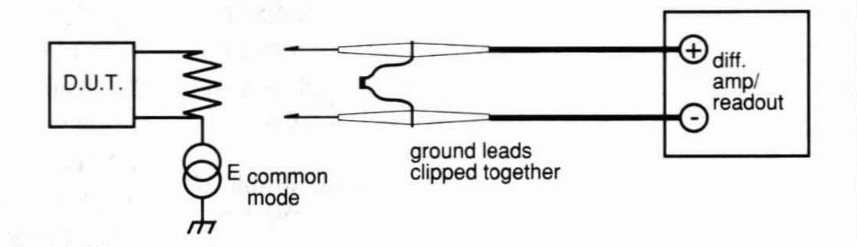


Figure 3-16

Figure 3-16. Basic connections to a device under test to make a differential measurement.

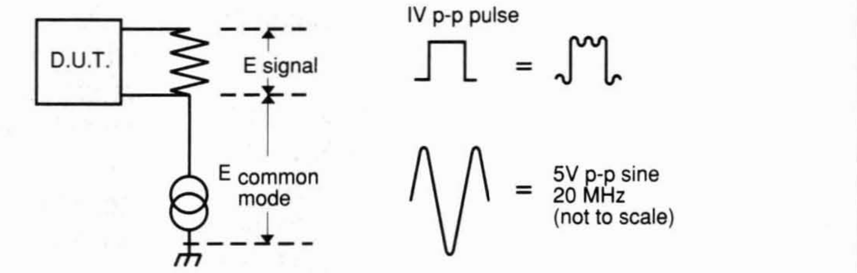


Figure 3-17

Figure 3-17. Simplified diagram. Elevated DUT. Common mode rejection is 10:1 at 20 MHz.

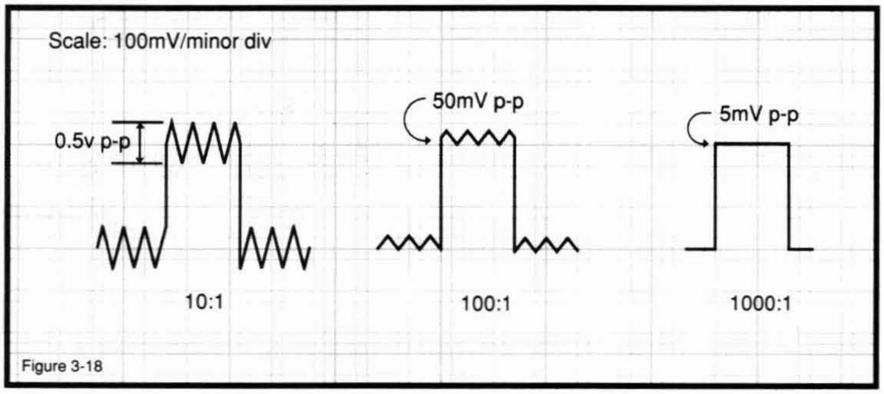


Figure 3-18

Figures 3-18, a, b and c. Displayed waveforms from the circuit shown in figure 3-17 at CMRR's of 10:1, 100:1 and 1000:1.

APPENDIX B

Measuring Amplifier Settling Time

High resolution measurement of amplifier settling at high speed is often necessary. Frequently, the amplifier is driven from a digital-to-analog converter (DAC). In particular, the time required for the DAC-amplifier combination to settle to final value after an input step is especially important. This specification allows setting a circuit's timing margins with confidence that the data produced is accurate. The settling time is the total length of time from input step application until the amplifier output remains within a specified error band around the final value.

Figure B1 shows one way to measure DAC amplifier settling time. The circuit uses the false sum node technique. The resistors and amplifier form a summing network. The amplifier output will step positive when the DAC moves. During slew, the oscilloscope probe is bounded by the diodes, limiting voltage excursion. When settling occurs, the summing node is arranged so the oscilloscope probe voltage should be zero. Note that the resistor divider's attenuation means the probe's output will be one-half the actual settled voltage.

In theory, this circuit allows settling to be observed to small amplitudes. In practice, it cannot be relied upon to produce useful measurements. Several flaws exist. The oscilloscope connection presents problems. As probe capacitance rises, AC loading of the resistor junction will influence observed settling waveforms. The 20pF probe shown alleviates this problem but its 10X attenuation sacrifices oscilloscope gain. 1X probes are not suitable because of their excessive input capacitance. An active 1X FET probe might work, but another issue remains.

The clamp diodes at the probe point are intended to reduce swing during amplifier slewing, preventing excessive oscilloscope overdrive. Unfortunately, oscilloscope overdrive recovery characteristics vary widely among different types and are not usually specified. The diodes' 600mV drop means the oscilloscope may see an unacceptable overload, bringing displayed results into question (for a discussion of oscilloscope overdrive considerations, see the Tutorial Section on Oscilloscopes). With the oscilloscope set at 1mV per division, the diode bound allows a 600:1 overdrive. Schottky diodes can cut this in half, but this is still much more than any real-time vertical amplifier is designed to accommodate.[1] The oscilloscope's overload recovery will completely dominate the observed waveform and all measurements will be meaningless.

One way to achieve reliable settling time measurements is to clip the incoming waveform in *time*, as well as amplitude. If the oscilloscope is prevented from seeing the waveform until settling is nearly complete, overload is avoided. Doing this requires placing a switch at the settle circuit's output and controlling it with an input-triggered, variable delay. FET switches are not suitable because of their gate-source capacitance. This capacitance will allow gate drive artifacts to corrupt the oscilloscope display,

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Note 1: See Reference 3 for history and wisdom about vertical amplifiers.

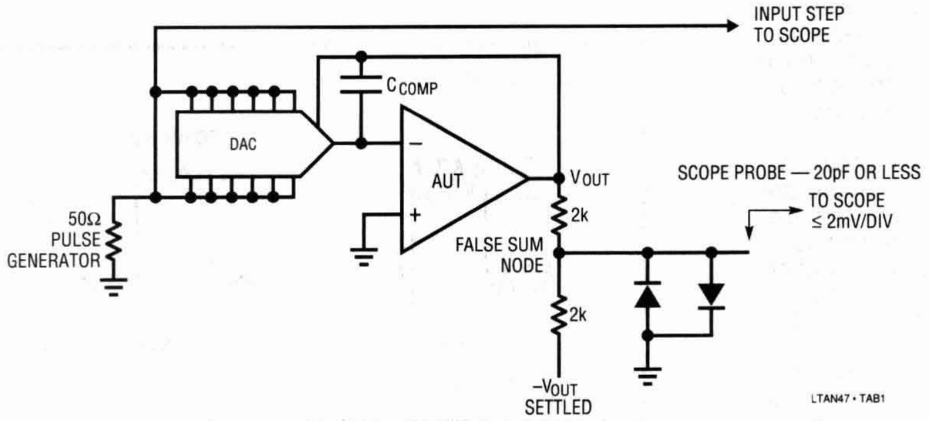

Figure B1. One (Not Very Good) Way to Measure DAC-Op Amp Settling Time

producing confusing readings. In the worst case, gate drive transients will be large enough to induce overload, defeating the switch's purpose.

Figure B2 shows a way to implement the switch which largely eliminates these problems. This circuit allows settling within 1mV to be observed. The Schottky sampling bridge is the actual switch. The bridge's inherent balance, combined with matched diodes and very high speed complementary bridge switching, yields a clean switched output. An output buffer stage unloads the settle node and drives the diode bridge.

The operation of the DAC-amplifier is as before. The additional circuitry provides the delayed switching function, eliminating oscilloscope overdrive. The settle node is buffered by A1, a unity gain broadband FET input buffer with 3pF input capacitance and 350MHz bandwidth. A1 drives the Schottky bridge. The pulse generator's output fires the 74123 one shot. The one shot is arranged to produce a delayed (controllable by the 20k potentiometer) pulse whose width (controllable by the 5k potentiometer) sets diode bridge on-time. If the delay is set appropriately, the oscilloscope will not see any input until settling is nearly complete, eliminating overdrive. The sample window width is adjusted so that all remaining settling activity is observable. In this way the oscilloscope's output is reliable and meaningful data may be taken. The one shot's output is level shifted by the Q1-Q4 transistors, providing complementary switching drive to the bridge. The actual switching transistors, Q1-Q2, are UHF types, permitting true differential bridge switching with less than 1ns of time skew.[2] The bridge's output may be observed directly (by oscilloscopes with adequate sensitivity) or A2 provides a times 10 amplified version. A2's gain of 20 (and the direct output's ÷ 2 scaling) derives from the 2k-2k settle node dividers attenuation. A third output, taken directly from A1, is also available. This output, which bypasses the entire switching circuitry, is designed to be monitored by a sampling oscilloscope. Sampling oscilloscopes are inherently immune to overload.[3] As such, a good test of this settling time test fixture (and the above statement) is to compare the signals displayed by the sampling 'scope and the Schottky-bridge-aided real time 'scope. As an *additional* test, a completely different method of measuring settling time (albeit considerably more complex) described by Harvey[4] was also employed. If all three approaches represent good measurement technique and are constructed properly, results should be identical.[5] If this is the case, the identical data produced by the three methods has a high probability of being valid. Figures B3, B4 and B5 show settling time details of an AD565A DAC and an LT1220 op amp. The photos represent the sampling bridge, sampling 'scope and Harvey methods, respectively. Photos B3 and B5 display the input step for convenience in ascertaining elapsed time. Photo B4, taken with a single trace sampling oscilloscope (Tektronix 1S1 with P6032 cathode follower probe in a 556 mainframe) uses the leftmost vertical graticule line as its zero time reference. All methods agree on 280ns to 0.01% settling (1mV on a 10V step). Note that Harvey's method inherently adds 30ns, which must be subtracted from the displayed 310ns to get the real number.[6] Additionally, the shape of the settling waveform, in every detail, is identical in all three photographs. This kind of agreement provides a high degree of credibility to the measured results.

Some poorly designed amplifiers exhibit a substantial thermal tail after responding to an input step. This phenomenon, due to die heating, can cause the output to wander outside desired limits long after settling has apparently occurred. After checking settling at high speed, it is always a good idea to slow the oscilloscope sweep down and look for thermal tails. Often the thermal tail's effect can be accentuated by loading the amplifier's output. Such a tail can make an amplifier appear to have settled in a much shorter time than it actually has.

To get the best possible settling time from any amplifier, the feedback capacitor, C_F, should be carefully chosen. C_F's purpose is to roll-off amplifier gain at the frequency which permits best dynamic response. The optimum value for C_F will depend on the feedback resistor's value and the characteristics of the source. DAC's are one of the most common sources and also one of the most difficult. DAC's current outputs must often be converted to a

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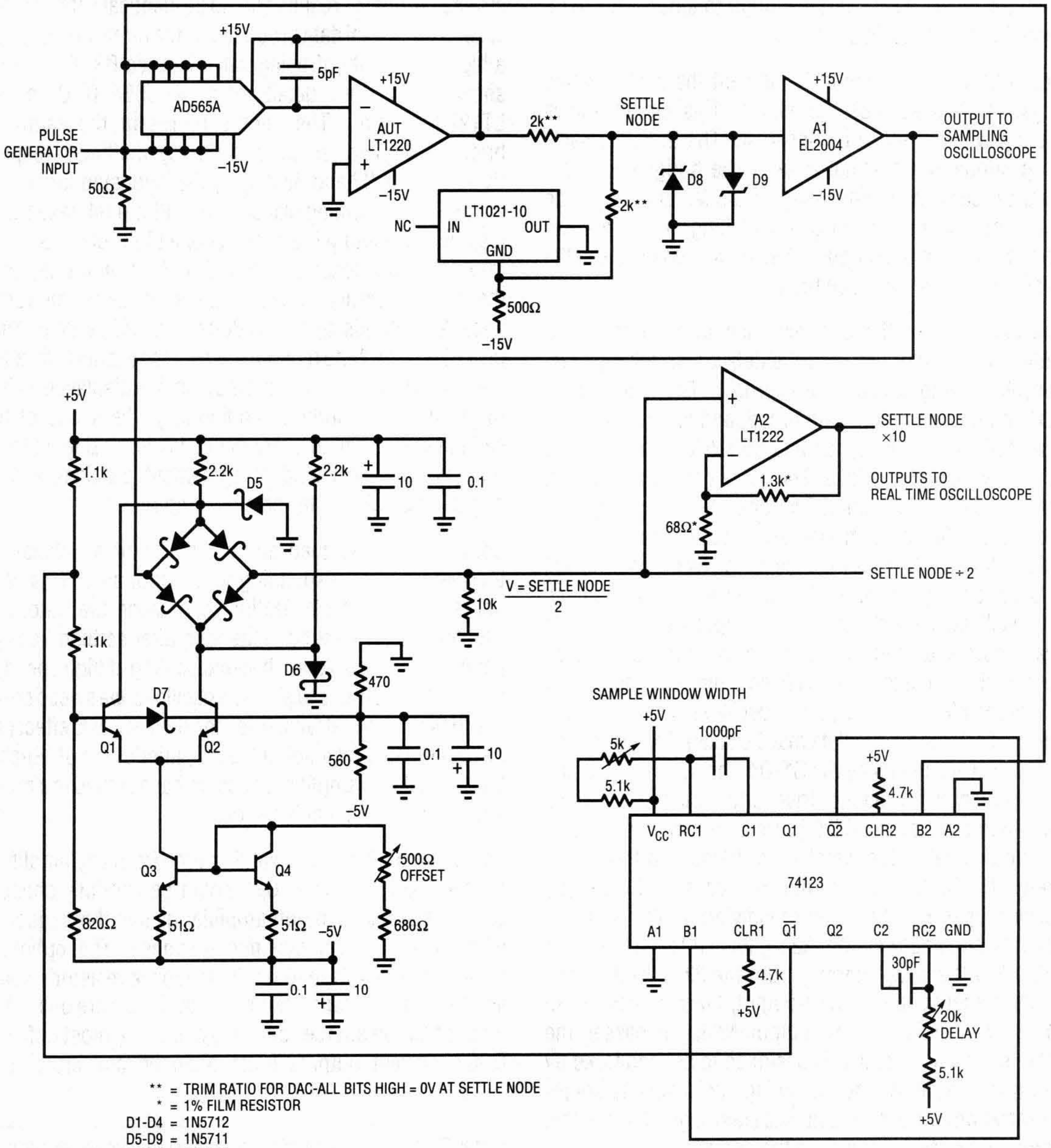
Note 2: The Q1-Q4 bridge switching scheme, a variant of one described in Reference 14, was developed at LTC by George Feliz.

Note 3: See References 7, 8 and 18.

Note 4: See Reference 17.

Note 5: Construction details of the settling time fixture discussed here appear (literally) in Appendix F, "Additional Comments on Breadboarding". Also see the Tutorial Section on Breadboarding Techniques.

Note 6: See Reference 17.


+15V
5pF
AD565A
PULSE
GENERATOR
INPUT
50Ω
–15V
+15V
AUT
LT1220
–15V
2k**
SETTLE
NODE
D8
D9
+15V
A1
EL2004
–15V
OUTPUT TO
SAMPLING
OSCILLOSCOPE
LT1021-10
NC
IN
OUT
GND
2k**
500Ω
–15V
+5V
1.1k
2.2k
2.2k
D5
10
0.1
A2
LT1222
SETTLE NODE
×10
1.3k*
OUTPUTS TO
REAL TIME OSCILLOSCOPE
68Ω*
SETTLE NODE ÷ 2
10k
V = SETTLE NODE / 2
1.1k
D6
470
D7
Q1
Q2
560
0.1
10
–5V
SAMPLE WINDOW WIDTH
+5V
5k
1000pF
5.1k
+5V
4.7k
V_{CC} RC1 C1 Q1 Q̄2 CLR2 B2 A2
74123
A1 B1 CLR1 Q̄1 Q2 C2 RC2 GND
Q3
Q4
500Ω
OFFSET
820Ω
51Ω
51Ω
–5V
680Ω
0.1
10
4.7k
+5V
30pF
20k
DELAY
5.1k
+5V

** = TRIM RATIO FOR DAC-ALL BITS HIGH = 0V AT SETTLE NODE
* = 1% FILM RESISTOR
D1-D4 = 1N5712
D5-D9 = 1N5711
Q3, Q4 = 2N3904
Q1, Q2 = MRF501

BYPASS ALL ACTIVE DEVICES

LTAN47 • TAB2

Figure B2. Settling Time Test Circuit Using a Sampling Bridge Eliminates Oscilloscope Overdrive

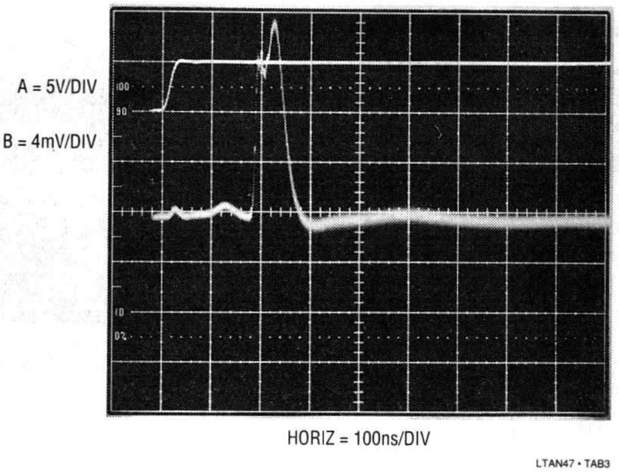


Figure B3. 280ns Settling Time as Measured by Figure B2's Circuit. Sampling Switch Closes Just Before Third Vertical Division, Allowing Settling Detail to be Observed Without Overdriving the Oscilloscope

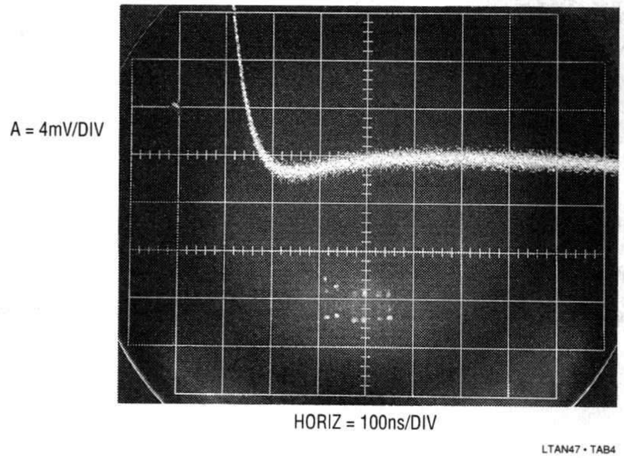


Figure B4. 280ns Settling Time as Measured at Figure B2's Sampling Oscilloscope Output by a Sampling 'Scope. Settling Time and Waveform Shape is Identical to Figure B3

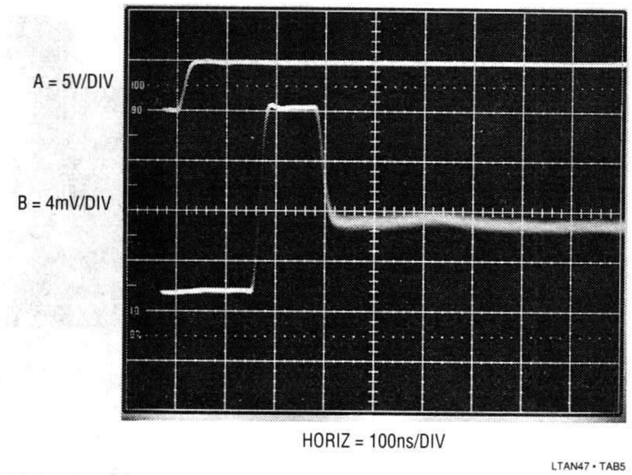


Figure B5. 280ns Settling Time as Measured by Harvey's Method. After Subtraction of this Method's Inherent 30ns Delay, Settling Time and Waveform Shape are Identical to Figures B3 and B4

voltage. Although an op amp can easily do this, care is required to obtain good dynamic performance. A fast DAC can settle to 0.01% in 200ns or less but its output also includes a parasitic capacitance term, making the amplifier's job more difficult. Normally, the DAC's current output is unloaded directly into the amplifier's summing junction, placing the parasitic capacitance from ground to the amplifier's input. The capacitance introduces feedback phase shift at high frequencies, forcing the amplifier to hunt and ring about the final value before settling. Different DACs have different values of output capacitance. CMOS DACs have the highest output capacitance and it varies with code. Bipolar DACs typically have 20pF-30pF of capacitance, stable over all codes. Because of their output capacitance, DAC's furnish an instructive example in amplifier compensation. Figure B6 shows the response of an industry standard DAC-80 type and a relatively slow (for this publication) op amp. Trace A is the input, while Traces B and C are the amplifier and settle outputs, respectively. In this example no compensation capacitor is used and the amplifier rings badly before settling. In Figure B7, an 82pF unit stops the ringing and settling time goes down to 4μs. The overdamped response means that C_F dominates the capacitance at the AUT's input and stability is assured. If fastest response is desired, C_F must be reduced. Figure B8 shows critically damped behavior obtained with a 22pF unit. The settling time of 2μs is the best obtainable for this DAC-amplifier combination. Higher speed is possible with faster amplifiers and DACs but the compensation issues remain the same.

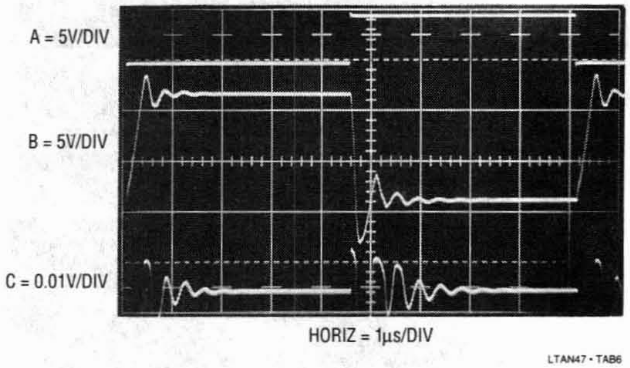


Figure B6. No Feedback Capacitor

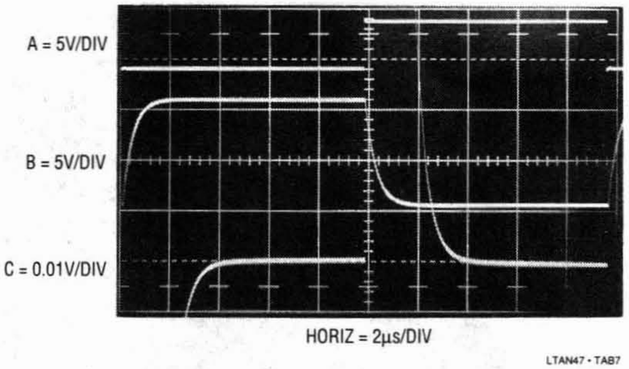


Figure B7. Relatively Large Feedback Capacitor

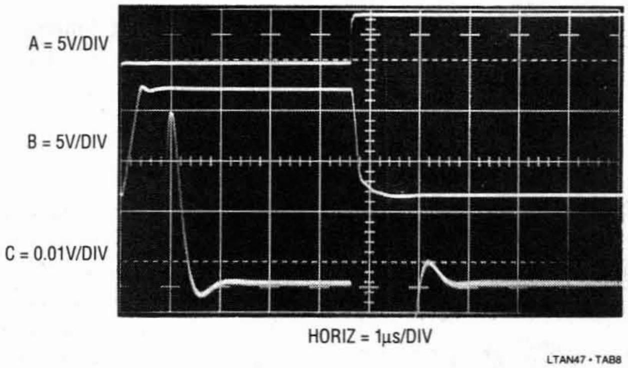


Figure B8. Reduced Feedback Capacitor Gives Fastest Settling

Figures B6-B8. Effects of Different Feedback Capacitors on a DAC-Op Amp Combination

APPENDIX C

The Oscillation Problem – Frequency Compensation Without Tears

All feedback systems have the propensity to oscillate. Basic theory tells us that gain and phase shift are required to build an oscillator. Unfortunately, feedback systems, such as operational amplifiers, have gain and phase shift. The close relationship between oscillators and feedback amplifiers requires careful attention when an op amp is designed. In particular, excessive input-to-output phase shift can cause the amplifier to oscillate when feedback is applied. Further, any time delay placed in the amplifier's feedback path introduces additional phase shift, increasing the likelihood of oscillation. This is why feedback loop enclosed stages can cause oscillation.

A large body of complex mathematics is available which describes stability criteria and can be used to predict stability characteristics of feedback amplifiers. For the most sophisticated applications, this approach is required to achieve optimum performance.

However, little has appeared which discusses, in practical terms, how to understand and address the issues of compensating feedback amplifiers. Specifically, a practical approach to stabilizing amplifier-power gain stage combinations is discussed here, although the considerations can be generalized to other feedback systems.

Oscillation problems in amplifier-power booster stage combinations fall into two broad categories; local and loop oscillations. *Local* oscillations can occur in the boost stage, but should not appear in the IC op amp, which presumably was debugged prior to sale. These oscillations are due to transistor parasitics, layout and circuit configuration-caused instabilities. They are usually relatively high in frequency, typically in the 0.5MHz to 100MHz range. Usually, local booster stage oscillations do not cause loop disruption. The major loop continues to function, but contains artifacts of the local oscillation. Text Figure 101, repeated here as Figure C1 for reader convenience, furnishes an instructive example. The Q1, Q2 emitter follower pair has reasonably high f_t. These devices will oscillate if driven from a low impedance source (see insert, Figure C1 and References 43 and 44). The 100Ω resistor and the ferrite beads are included to make the op amps output look like a higher impedance to prevent problems. Q5 and Q6, also followers, have even higher f_t, but are driven from 330Ω sources, eliminating the problem.The photo in Figure C2 shows Figure C1 following an input with the 100Ω resistor and ferrite beads removed. Trace A is the input, while Trace B is the output. The resultant high frequency oscillation is typical of locally caused disturbances. Note that the major loop is functional, but the local oscillation corrupts the waveform.

Eliminating such local oscillations starts with device selection. Avoid high f_t transistors unless they are needed. When high frequency devices are in use, plan layout carefully. In very stubborn cases, it may be necessary to lightly bypass transistor junctions with small capacitors or RC networks. Circuits which use local feedback can sometimes require careful transistor selection and use. For example, transistors operating in a local loop may require different f_ts to achieve stability. Emitter followers are notorious sources of oscillation and should never be directly driven from low impedance sources (again, see References 43 and 44).

Loop oscillations are caused when the added gain stage supplies enough delay to force substantial phase shift. This causes the control amplifier to run too far out of phase with the gain stage. The control amplifier's gain combined with the added delay causes oscillation. Loop oscillations are usually relatively low in frequency, typically 10Hz-1MHz.

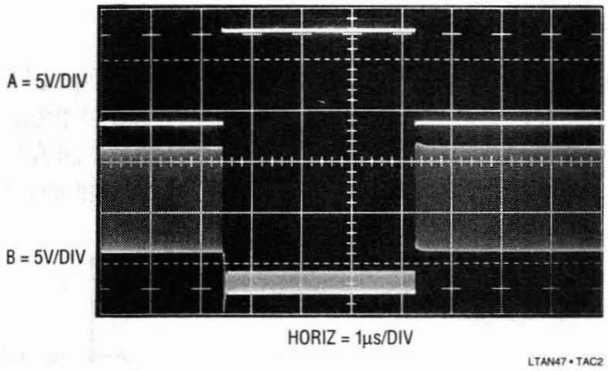


Figure C2. Local Oscillations Due to Booster Stage Instabilities

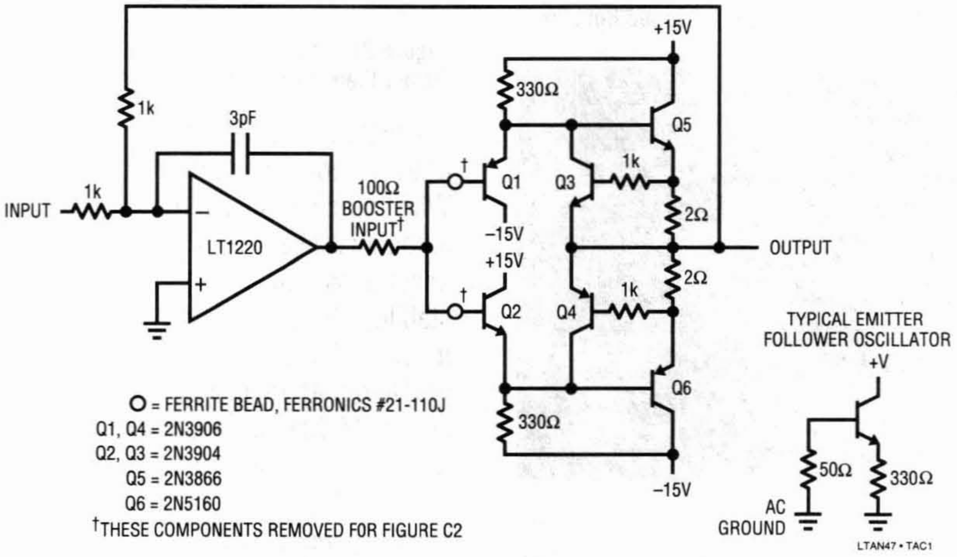

+15V
330Ω
1k
3pF
Q5
1k
†
Q1
Q3
INPUT
1k
100Ω
BOOSTER
INPUT†
2Ω
LT1220
–15V
+15V
OUTPUT
2Ω
1k
†
Q2
Q4
TYPICAL EMITTER
FOLLOWER OSCILLATOR
+V
Q6
○ = FERRITE BEAD, FERRONICS #21-110J
Q1, Q4 = 2N3906
330Ω
Q2, Q3 = 2N3904
Q5 = 2N3866
50Ω
330Ω
Q6 = 2N5160
–15V
AC
GROUND
†THESE COMPONENTS REMOVED FOR FIGURE C2
LTAN47 • TAC1

Figure C1. Figure 101's Booster Circuit with a Few Components Removed Begins Our Study of Loop Stability

A good way to eliminate loop-caused oscillations is to limit the gain-bandwidth of the control amplifier. If the booster stage has higher gain-bandwidth than the control amplifier, its phase delay is easily accommodated in the loop. When control amplifier gain-bandwidth dominates, oscillation is assured. Under these conditions, the control amplifier hopelessly tries to servo a feedback signal which consistently arrives too late. The servo action takes the form of an electronic tail chase with oscillation centered around the ideal servo point.

Frequency response roll-off of the control amplifier will almost always cure loop oscillations. In many situations it is preferable to brute force compensation using large capacitors in the major feedback loop. As a general rule, it is wise to stabilize the loop by rolling off control amplifier gain-bandwidth. The feedback capacitor serves only to trim step response and should not be relied on to stop outright oscillation.

Figures C3 and C4 illustrate these issues. The LT1006 amplifier used with the LT1010 current buffer produces the output shown in Figure C4. As before, Trace A is the input and Trace B the output. The LT1006 has less than 1MHz gain-bandwidth. The LT1010's 20MHz gain-bandwidth introduces negligible loop delay, and dynamics are clean. In this case, the LT1006's internal roll-off is well below that of the output stage and stability is achieved with no external compensation components. Figure C5 uses a 100MHz bandwidth LT1223 as the control amplifier. The associated photo (Figure C6) shows the results. Here, the control amplifier's roll-off is well beyond the output stage's, causing problems. The phase shift through the LT1010 is now appreciable and oscillations occur. Stabilizing this circuit requires degenerating the control amplifier's gain-bandwidth.

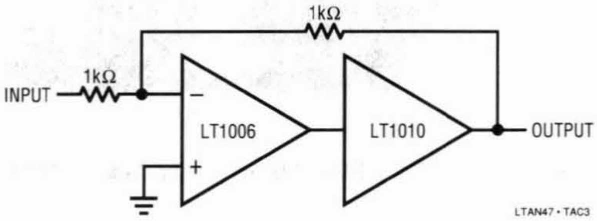


Figure C3. A Slow Op Amp and a Medium Speed Booster

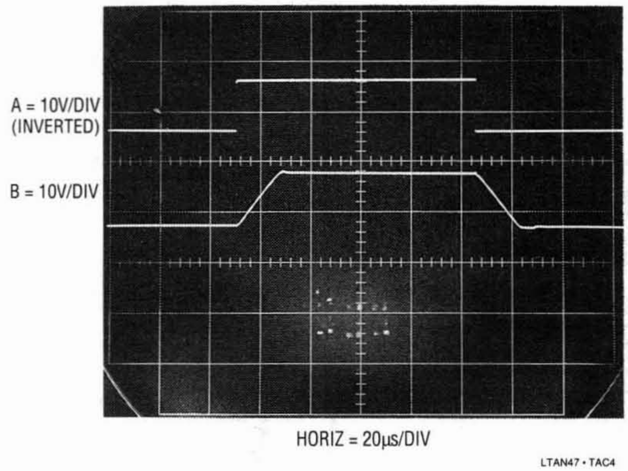


Figure C4. Loop Stability is "Free" When the Op Amp is Much Slower than the Booster

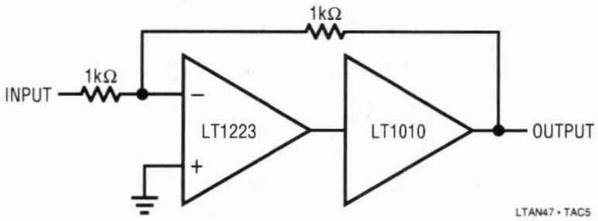


Figure C5. A Fast Op Amp and a Medium Speed Booster

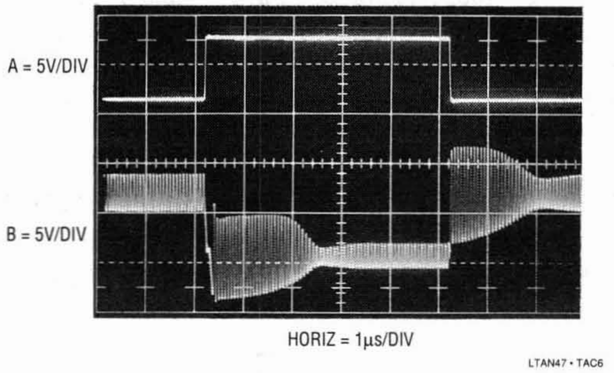


Figure C6. Loop Oscillation is "Free" When the Op Amp is Much Faster than the Booster

The fact that the slower op amp circuit doesn't oscillate is a key to understanding how to compensate booster loops. With the slow device, compensation is free. The faster amplifier makes the AC characteristics of the output stage become significant and requires roll-off components for stability. Practically, the LT1223's speed is simply too much for the LT1010. A somewhat slower amplifier is the way to go. Alternately, a faster booster may be employed. Figure C7 attempts this, but doesn't quite make it. Photo C8 is less corrupted, but 100MHz oscillation indicates the booster stage (borrowed from text Figure 101) is still too slow for the LT1223. Attempts to use another booster design in Figure C9 (similarly purloined from text Figure

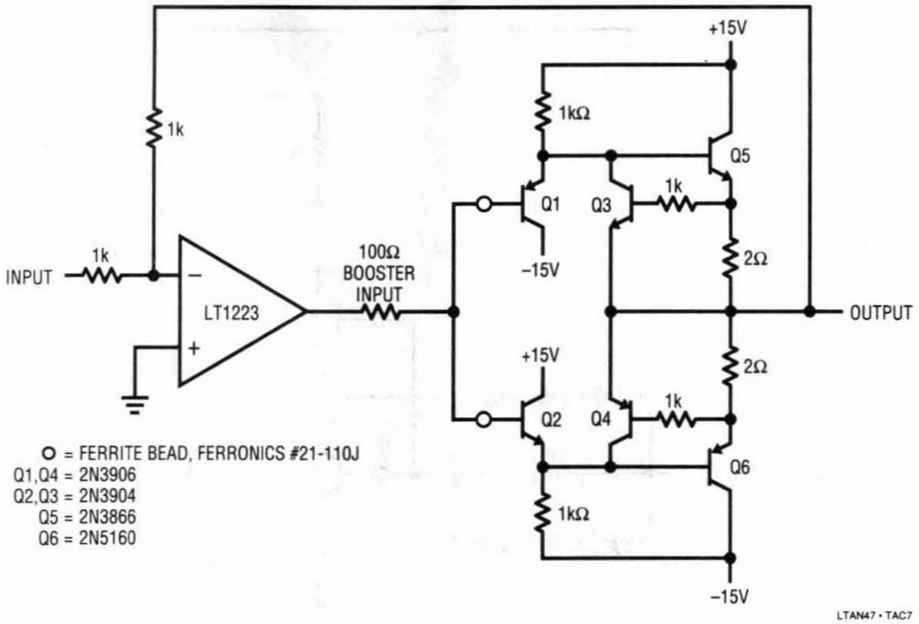


Figure C7. A Very Fast Amplifier with a Fast Booster

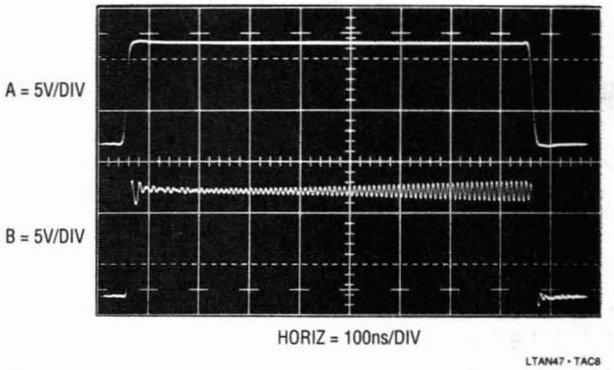


Figure C8. Figure C7's Booster is Not Quite Quick Enough to Prevent Loop Oscillation

104) fail for the same reason. Figure C10 shows 40MHz oscillation, indicative of this high power booster's slower speed.

Figure C11 has much more pleasant results. Here a 45MHz gain-bandwidth LT1220 has been substituted for the 100MHz LT1223 in Figure C7's circuit. The slower amplifier, combined with light local compensation, works well with the booster stage in its loop. Figure C12 shows a well controlled high speed output, nicely damped, with no sign of oscillations.

Power boosters are not the only things that can be placed within an amplifier's feedback loop. Text Figure 140's current source, reproduced here as Figure C13, is an interesting variation. There is no power booster in the loop, but rather a 40MHz differential amplifier with a gain of 10. To stabilize the circuit the slowest amplifier in the 1190 family, the 50MHz LT1190, is chosen. The local 100pF feedback slows it down a bit more and the loop is fast and stable (Figure C14). What happens if we remove the 100pF feedback path? Figure C15 shows that the loop is no longer stable under this condition because the LT1190 control amplifier cannot servo the phase shifted feedback at higher frequency. Put that 100pF capacitor back in!

It's worth mentioning that similar results to those obtained back in Figure C3 are obtainable by substituting a very slow control amplifier (e.g., an LT1006 which has less than 1MHz gain-bandwidth). The slower amplifier would give "free" compensation, eliminating the necessity for the 100pF unit. However, the circuit's frequency response would be severely degraded.

Text Figure 142's high power current source furnishes further instruction. This loop contains the differential amplifier *and* a booster, seemingly making things even more difficult. Figure C16, recognizable as text Figure 142's high power current source with the 100pF local compensation removed, oscillates above 10MHz. Replacing the compensation restores proper response. Figure

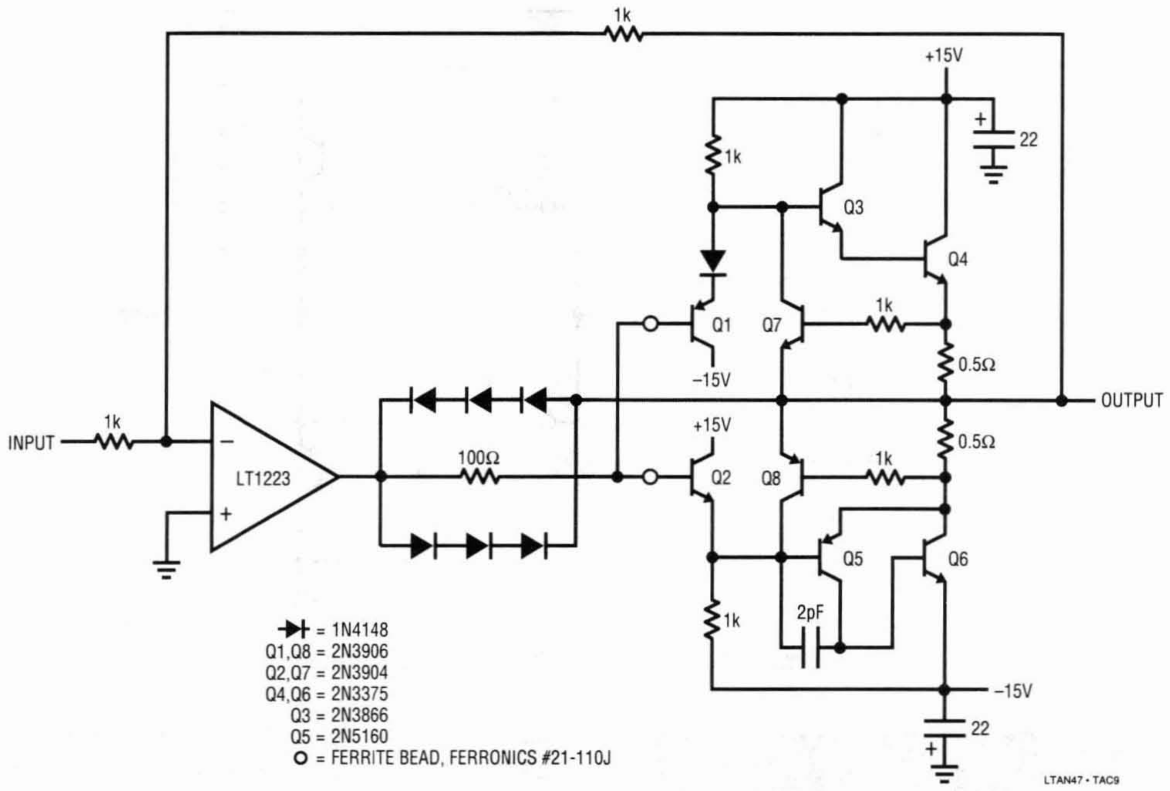

1k
+15V
22
1k
Q3
Q4
1k
Q1
Q7
0.5Ω
–15V
OUTPUT
INPUT
1k
LT1223
100Ω
+15V
Q2
Q8
1k
0.5Ω
Q5
Q6
1k
2pF
–15V
22
= 1N4148
Q1,Q8 = 2N3906
Q2,Q7 = 2N3904
Q4,Q6 = 2N3375
Q3 = 2N3866
Q5 = 2N5160
O = FERRITE BEAD, FERRONICS #21-110J
LTAN47 • TAC9

Figure C9. A Very Fast Amplifier with a Fast High Power Booster

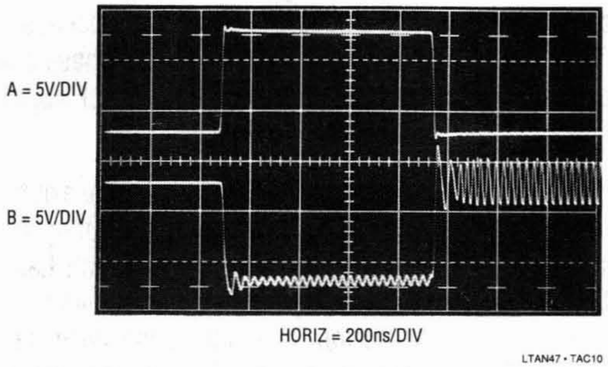


Figure C10. C9's High Power Booster is Fast But Causes Loop Oscillations

C17 shows the loop has no oscillations. What this tells us is that the control amplifier doesn't care just what generates the causal feedback between its input and output, so long as there isn't excessive delay. This circuit has a fairly busy feedback loop, but the control amplifier is oblivious to its bustling nature....unless you leave that 100pF feedback capacitor out!

When compensating loops like these, remember to investigate the effects of various loads and operating conditions. Sometimes a compensation scheme which appears fine gives bad results for some conditions. For this reason, check the completed circuit over as wide a variety of operating conditions as possible.

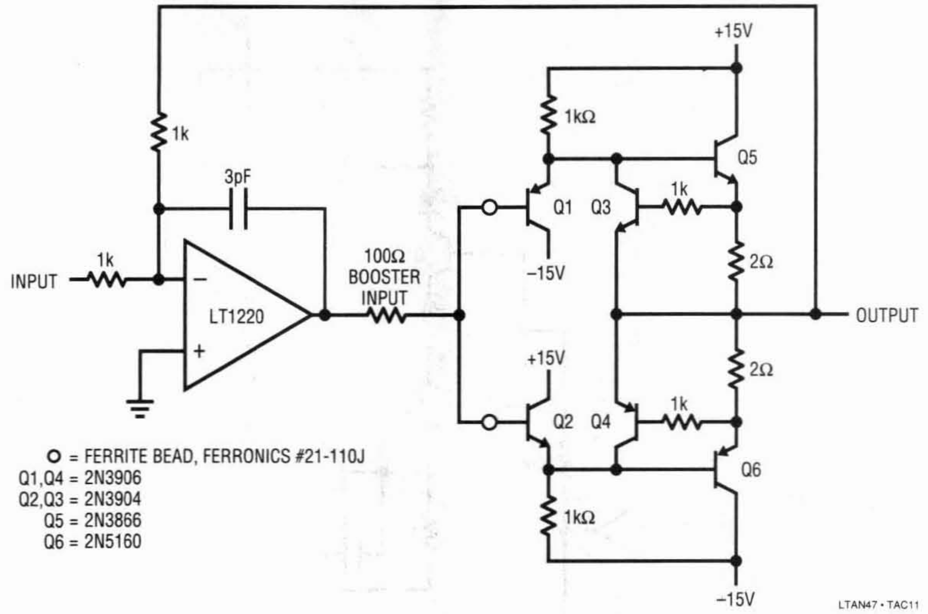

+15V
1k
3pF
INPUT
1k
LT1220
100Ω
BOOSTER
INPUT
1kΩ
Q1
Q3
Q5
1k
–15V
2Ω
OUTPUT
+15V
2Ω
Q2
Q4
1k
Q6
1kΩ
–15V
○ = FERRITE BEAD, FERRONICS #21-110J
Q1,Q4 = 2N3906
Q2,Q3 = 2N3904
Q5 = 2N3866
Q6 = 2N5160
LTAN47 • TAC11

Figure C11. Figure 101 (Again) with 100Ω Resistor and Beads Reinstalled

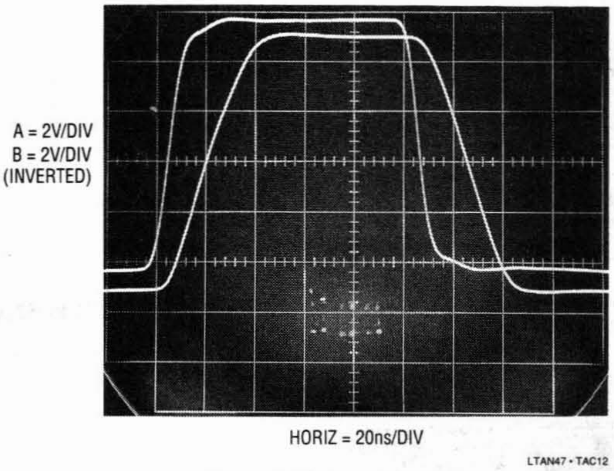


Figure C12. Lovely!

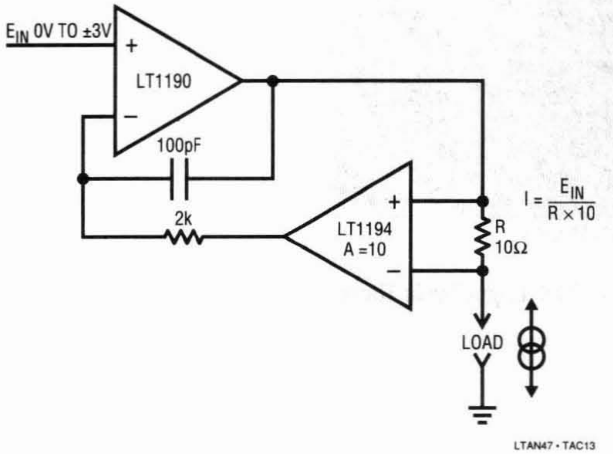

E_{IN} 0V TO ±3V
LT1190
100pF
2k
LT1194
A = 10
R
10Ω
$I = \frac{E_{IN}}{R \times 10}$
LOAD
LTAN47 • TAC13

Figure C13. Figure 140's Current Source. What Do the RC Components Do?

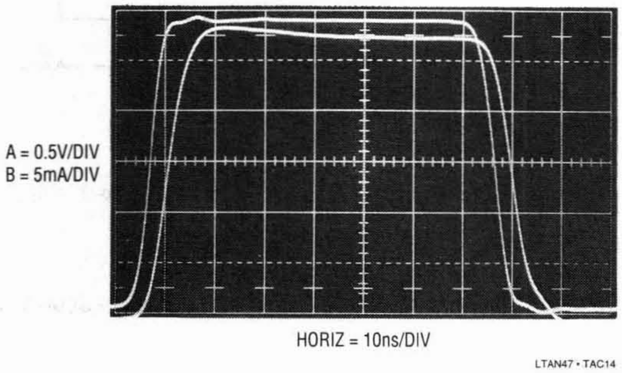


Figure C14. Response of the Current Source with the RC Components in Place

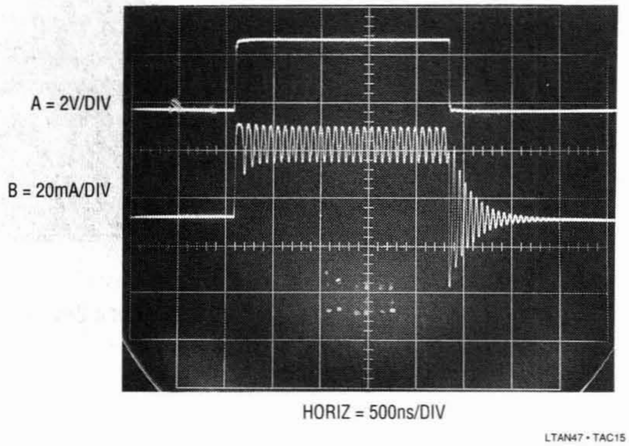


Figure C15. Removing the 100pF Capacitor Allows the Op Amp to See Phase Shifted Feedback, Causing Oscillation. Put that 100pF Back In!

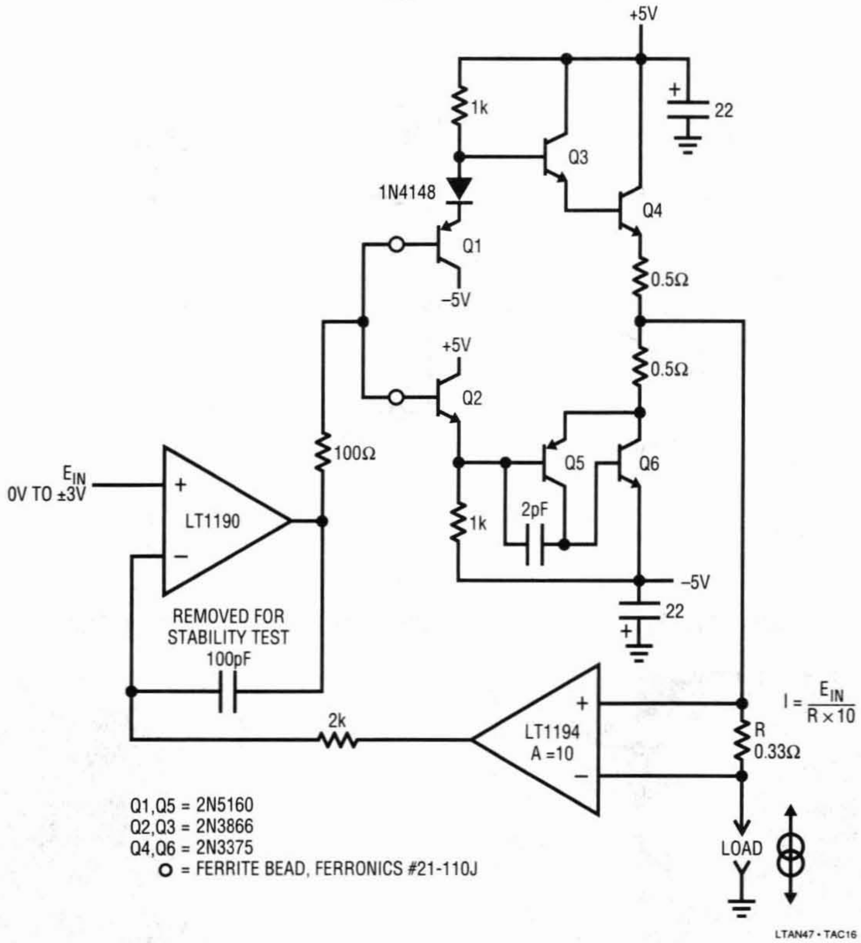

+5V
1k
22
Q3
1N4148
Q4
Q1
−5V
0.5Ω
+5V
0.5Ω
Q2
100Ω
Q5
Q6
E_{IN}
0V TO ±3V
LT1190
1k
2pF
−5V
22
REMOVED FOR
STABILITY TEST
100pF
$I = \frac{E_{IN}}{R \times 10}$
2k
LT1194
A =10
R
0.33Ω
Q1,Q5 = 2N5160
Q2,Q3 = 2N3866
Q4,Q6 = 2N3375
O = FERRITE BEAD, FERRONICS #21-110J
LOAD
LTAN47 • TAC16

Figure C16. Text Figure 142's High Power Current Source. When the 100pF Capacitor is Removed, 10MHz Loop Oscillations Result

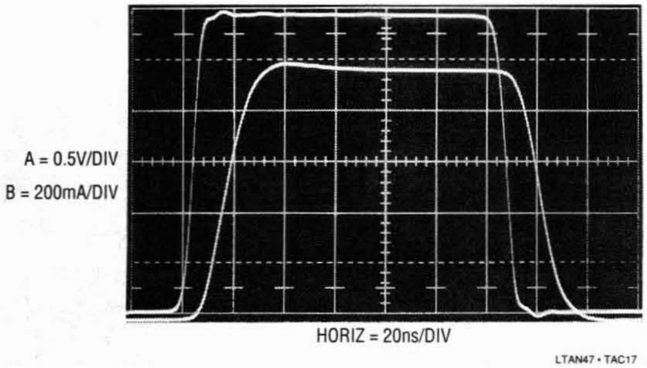


Figure C17. Much Better. Leave that 100pF Capacitor in There!

APPENDIX D

Measuring Probe-Oscilloscope Response

Verifying the rise time limit of wideband test equipment set-ups is a difficult task. In particular, the end-to-end rise time of oscilloscope-probe combinations is often required to assure measurement integrity. Conceptually, a pulse generator with rise times substantially faster than the oscilloscope-probe combination can provide this information. Figure D1's circuit does this, providing a 1ns pulse with rise and fall times inside 350ps. Pulse amplitude is 10V with a 50Ω source impedance. This circuit, built into a small box and powered by a 1.5V battery, provides a simple, convenient way to verify the rise time capability of almost any oscilloscope-probe combination.

The LT1073 switching regulator and associated components supply the necessary high voltage. The LT1073 forms a flyback voltage boost regulator. Further voltage step-up is obtained from a diode-capacitor voltage step-up network. L1 periodically receives charge and its flyback discharge delivers high voltage events to the step-up network. A portion of the step-up network's DC output is fed back to the LT1073 via the 10M, 24k divider, closing a control loop.

The regulator's 90V output is applied to Q1 via the 1M-2pF combination. Q1, a 40V breakdown device, non-destructively avalanches when C1 charges high enough. The result is a quickly rising, very fast pulse across R4. C1 discharges, Q1's collector voltage falls and breakdown ceases. C1 then recharges until breakdown again occurs. This action causes free running oscillation at about 200kHz.[1,2] Figure D2 shows the output pulse. A 1GHz sampling oscilloscope (Tektronix 556 with 1S1 sampling plug-in) measures the pulse at 10V high with about a 1ns base. Rise time is 350ps, with fall time also indicating 350ps. There is a slight hint of ring after the falling edge, but it is well controlled. The figures may actually be faster, as the 1S1 is specified with a 350ps limit.[3]

Q1 may require selection to get avalanche behavior. Such behavior, while characteristic of the device specified, is not guaranteed by the manufacturer. A sample of 50 Motorola 2N2369s, spread over a 12 year date code span, yielded 82%. All good devices switched in less than 650ps. C1 is selected for a 10V amplitude output. Value spread is typically 2pF-4pF. Ground plane type construction with

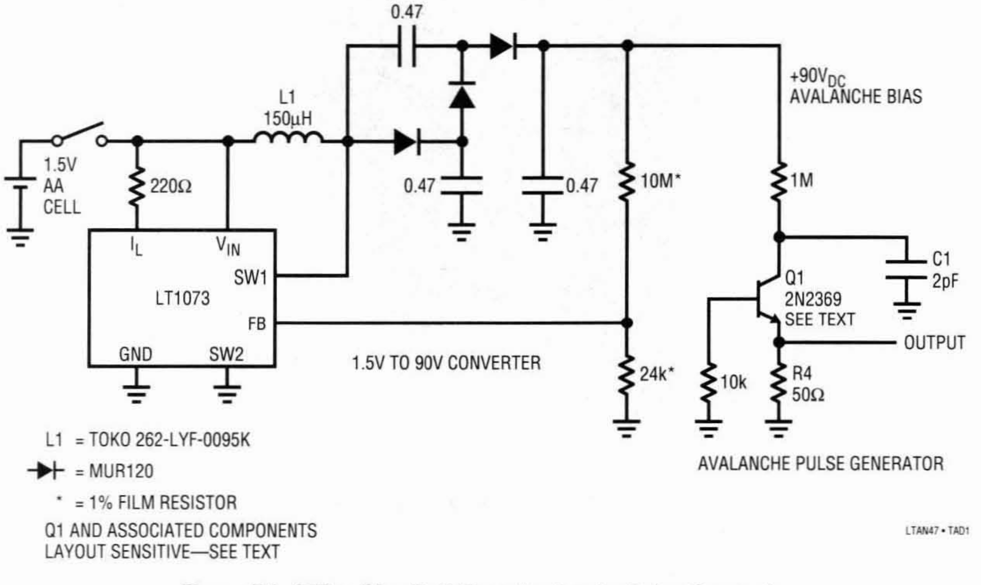


Figure D1. 350ps Rise/Fall Time Avalanche Pulse Generator

Note 1: This method of generating fast pulses borrows heavily from the Tektronix type 111 Pretrigger Pulse Generator. See References 8 and 25.

Note 2: This circuit replaces the tunnel diode based arrangement shown in AN13, Appendix D. While AN13's circuit works well, it generates a smaller, more irregularly shaped pulse and the tunnel diodes have become quite expensive.

Note 3: Just before going to press the pulse was measured at Hewlett-Packard Laboratories with a HP-54120B 12GHz sampling oscilloscope. Rise and fall times were 216ps and 232ps, respectively. Photo available on request.

high speed layout techniques are essential for good results from this circuit. Current drain from the 1.5V battery is about 5mA.

Figure D3 shows the physical construction of the actual generator. Power, supplied from a separate box, is fed into the generator's enclosure via a BNC connector. Q1 is mounted *directly* at the output BNC connector, with grounding and layout appropriate for wideband operation. Lead lengths, particularly Q1's and C1's, should be experimented with to get best output pulse purity. Figure D4 is the complete unit.

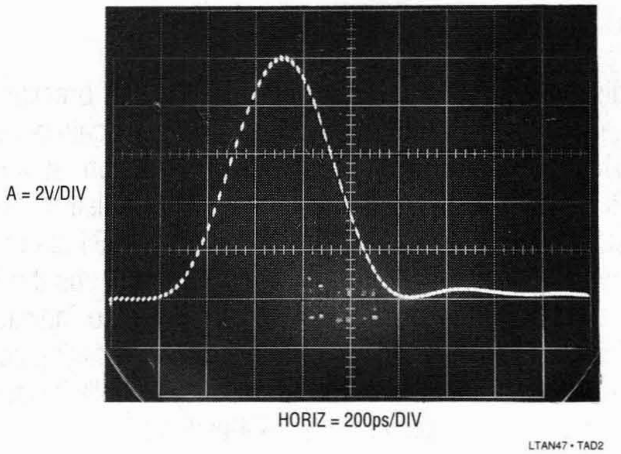


Figure D2. The Avalanche Pulse Generator's Output Monitored on a 1GHz Sampling Oscilloscope

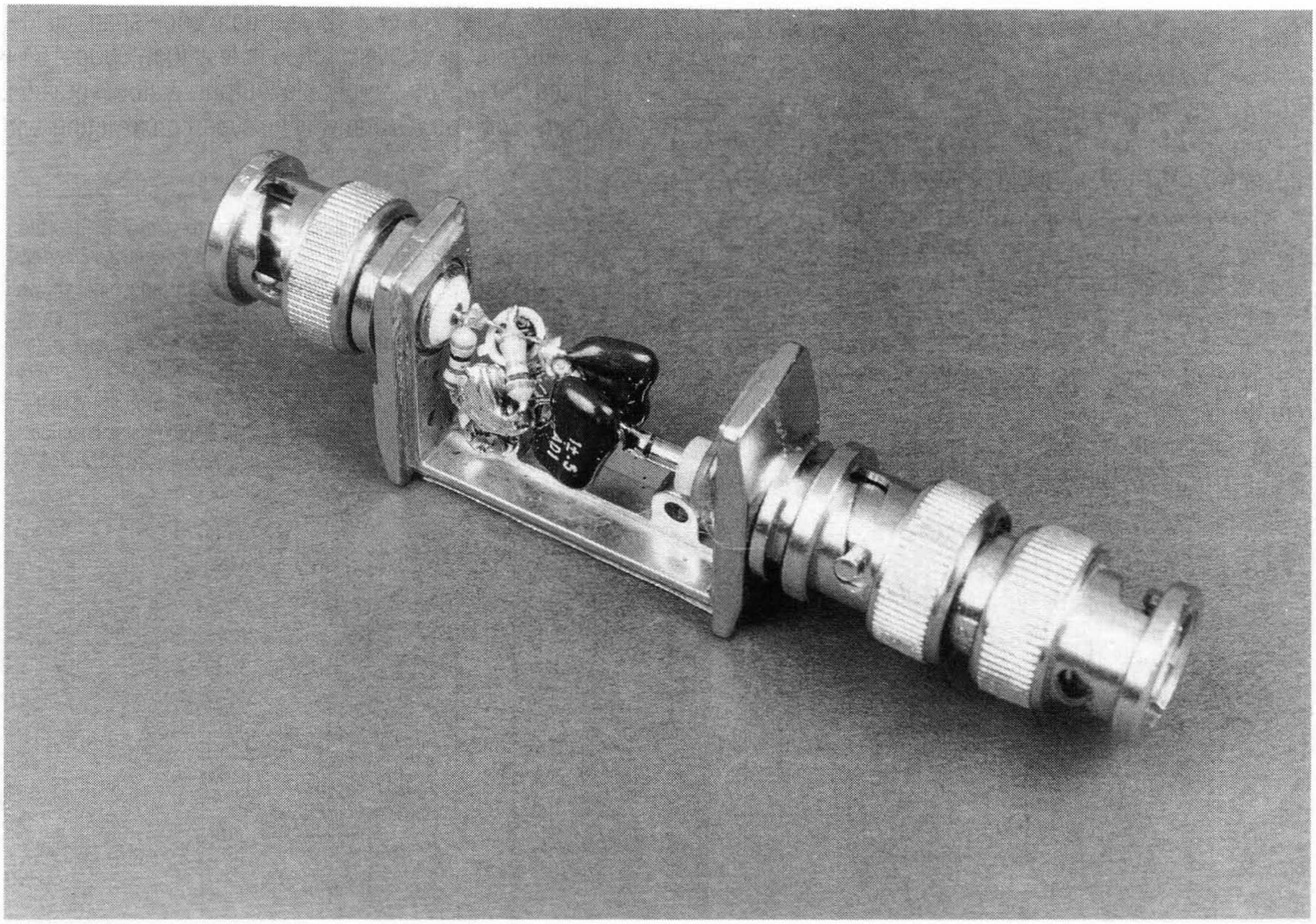
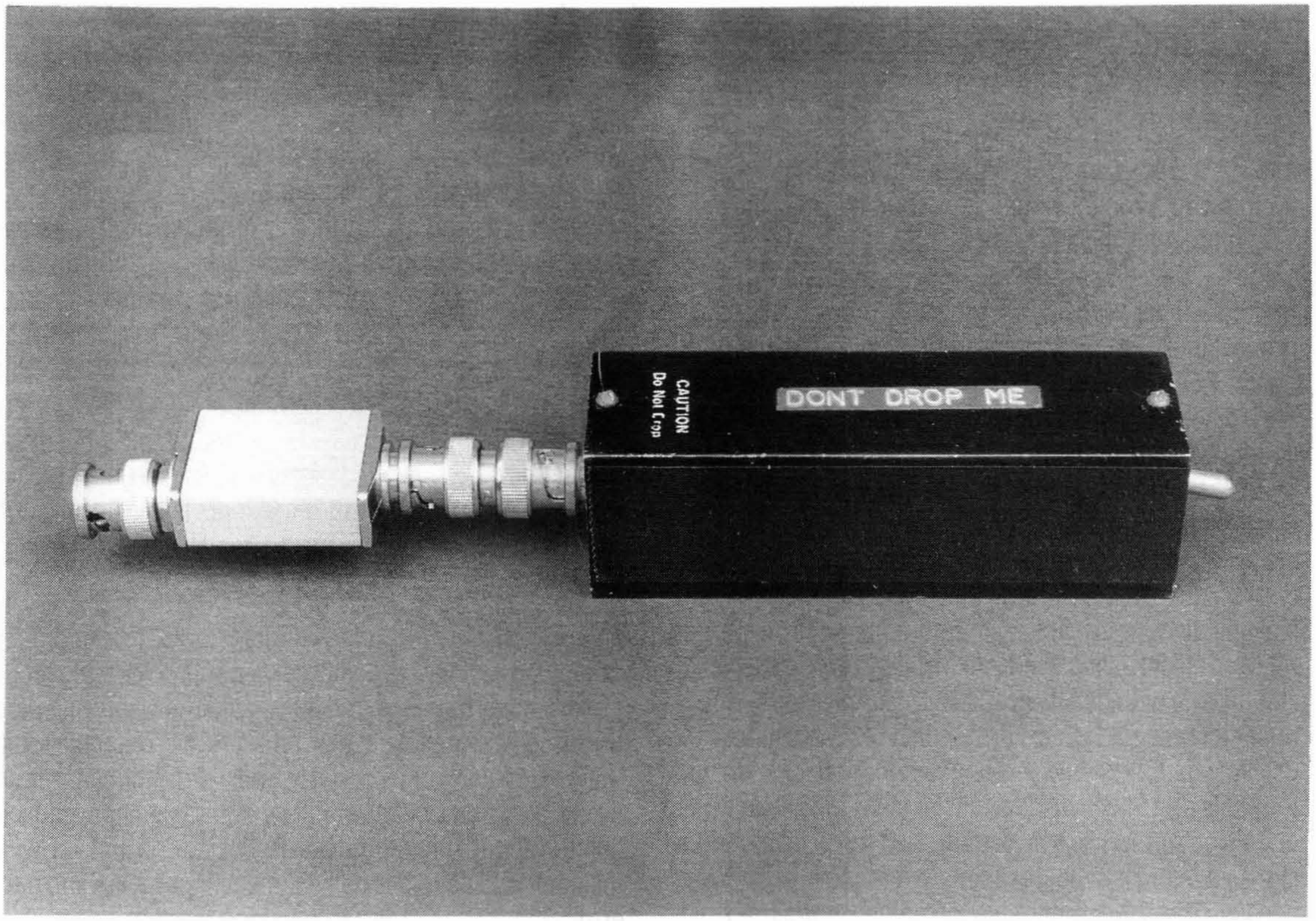


Figure D3. Details of the Avalanche Pulse Generator's Head. 90V$_{DC}$ Enters at Lower Right BNC, Pulse Exits at Top Left BNC. Note Short Lead Lengths Associated with Output


CAUTION
Do Not Crop
DONT DROP ME

LTAN47 • TAD4

Figure D4. The Packaged Avalanche Pulser. 1.5V-90V Converter is in the Black Box. Avalanche Head is at Left

APPENDIX E

An Ultra-Fast High Impedance Probe

Under most circumstances the 1pF-2pF input capacitance and 10MΩ resistance of FET probes is more than adequate for difficult probing situations. Occasionally, however, very high input resistance with high speed is needed. At some sacrifice in speed and input capacitance compared to commercial probes, it is possible to construct such a probe. Figure E1 shows schematic details. A1, a 350MHz hybrid FET buffer, forms the electrical core of the probe. This device is a low input capacitance, wideband FET source follower driving a fast bipolar output stage. The input of the probe goes to this device via a 51Ω resistor, reducing the possibility of oscillations in the follower input stage when the probe sees low AC impedance. A1's output drives a guard shield around the probe's input line, reducing effective input capacitance to about 4pF. A ground referred shield encircles the guard shield, reducing pickup and making high quality ground connections to the circuit under test easy. A1 drives the output BNC cable to feed the oscilloscope. Normally, it is undesirable to back terminate the cable at A1 because the oscilloscope will see only half of A1's output. While a back termination provides the best signal dynamics, the resulting attenuation is a heavy penalty. The RC damper shown can be trimmed for best edge response while maintaining an unattenuated output.

What can't be seen in the schematic is the probe's physical construction. Very careful construction is required to maintain low input capacitance, low bias current and wide bandwidth. The probe head is particularly critical. Every effort should be made to minimize the length of wire between A1's input and the probe tip. In our lab, we have found that discarded pieces of broken 10X probes, particularly attenuator boxes and probe heads, provide an excellent packaging basis for this probe.[1] Figure E2 shows the probe head. Note the compact packaging. Additionally, A1's package is arranged so that it's (not insubstantial) dissipated heat is transferred to the probe case body when the snap-on cover (shown in photo) is in place. This reduces A1's substrate temperature, keeping bias current down. A1's input is directly connected to the probe head to minimize parasitic capacitance. The power supply for A1, located in a separate enclosure, is fed in through separate wires. A1's output is delivered to the oscilloscope via conventional BNC hardware.

Figure E3 shows the probe output (Trace B) responding to an input (Trace A) as monitored on a 350MHz oscilloscope (Tektronix 485). Measured specifications for our version of this probe include a rise time of 6ns, 6ns delay and 350MHz bandwidth. The delay time contribution is about evenly split between the amplifier and cable. Input capacitance is about 4pF without the probe hook tip and 7pF with the hook tip. Input bias current measured 400pA and gain error about 5%. (A1 is an open loop device.)

---

[1] **Note 1:** This is not to encourage or even accept the breakage of probes. The author regards the breakage of oscilloscope probes as the lowest possible human activity. The sole exception to this condemnation is poor quality probes, which should be destroyed as soon as their deficiencies are discovered.

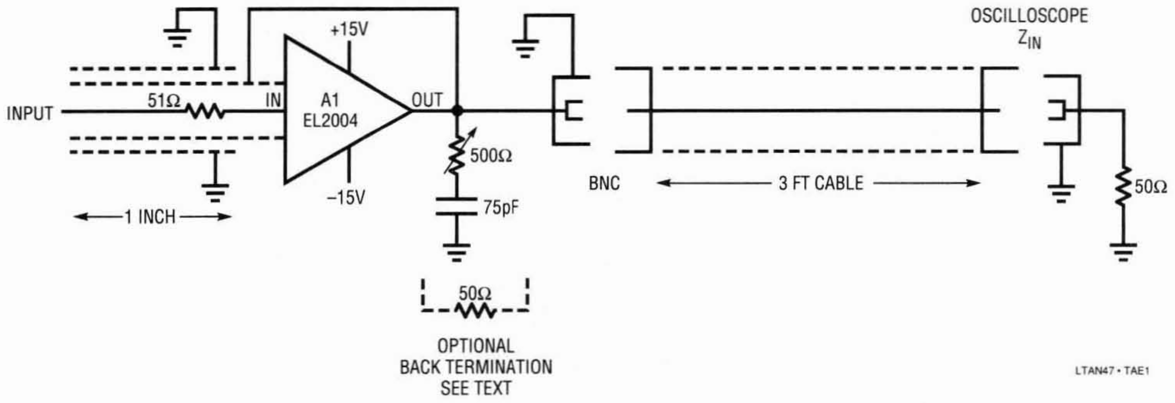
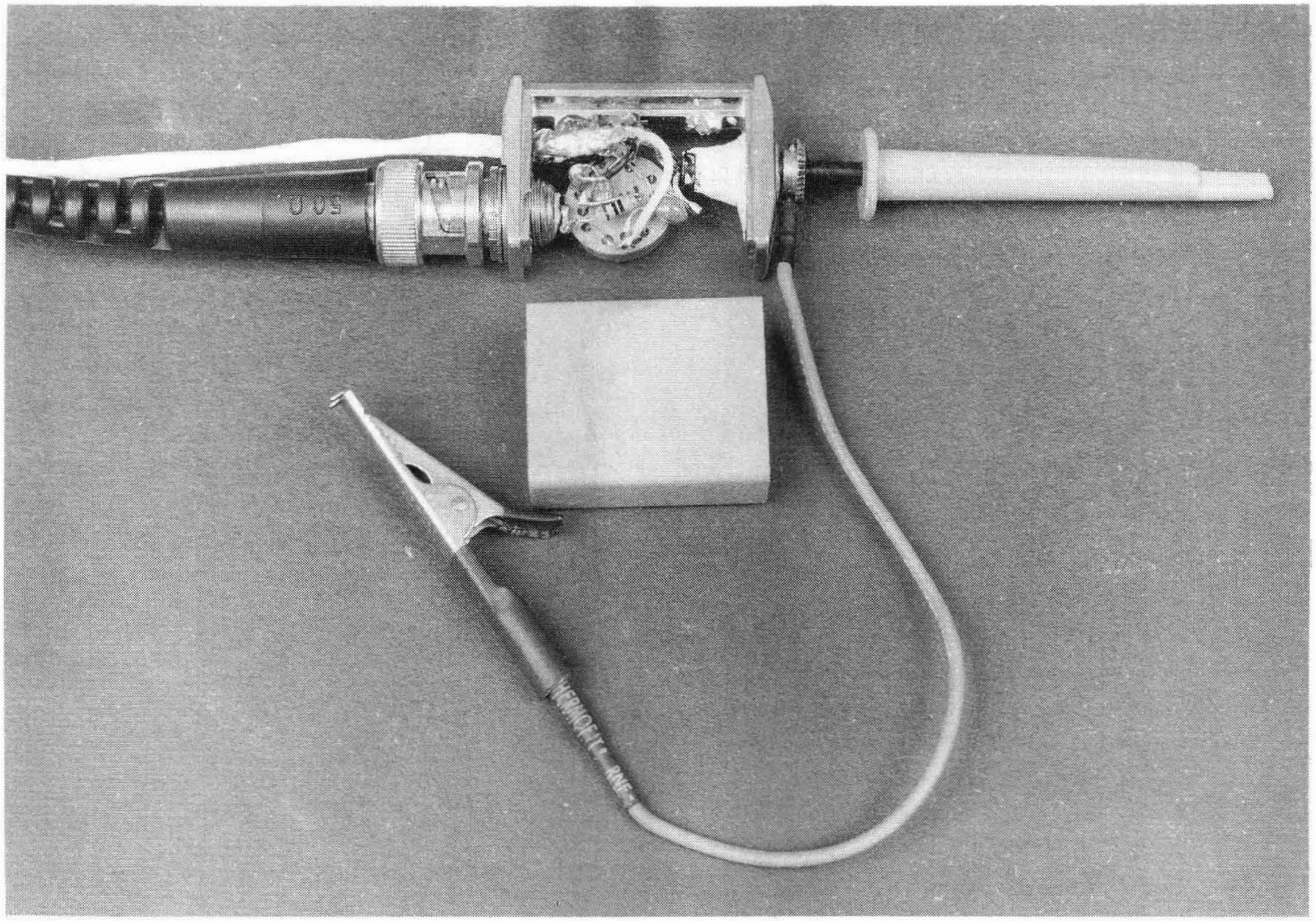
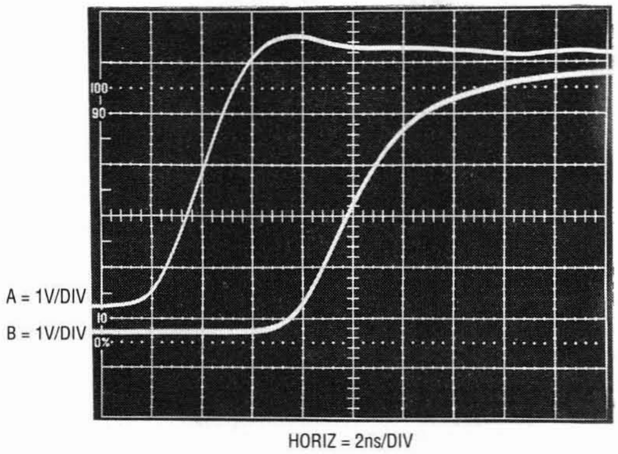


Figure E1. Ultra Fast Buffer Probe Schematic



LTAN47 • TAE2

Figure E2. Physical Layout of Ultra Fast Buffer Probe



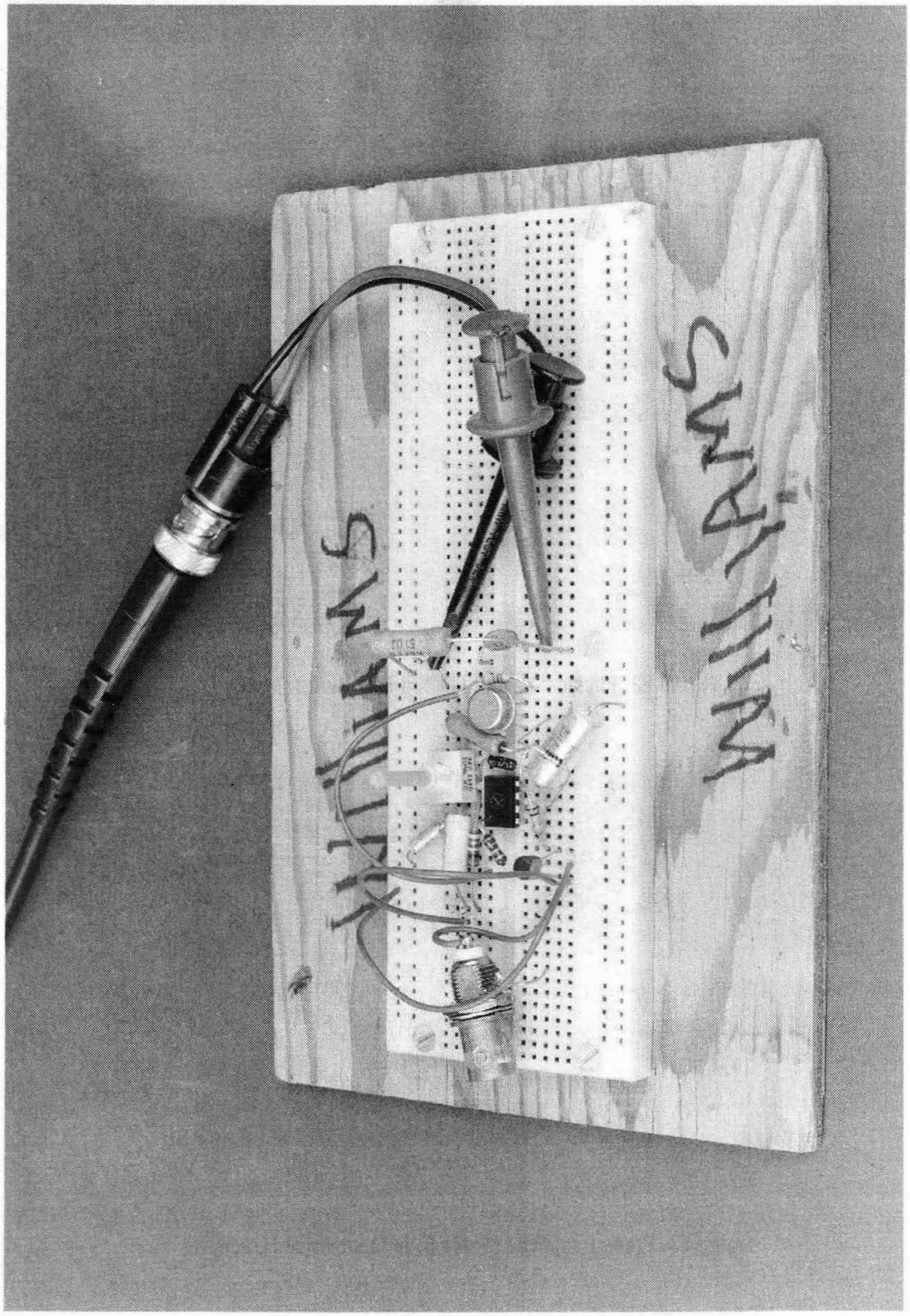
LTAN47 • TAE3

Figure E3. Probe Response (Trace B) to Input Pulse (Trace A)

APPENDIX F

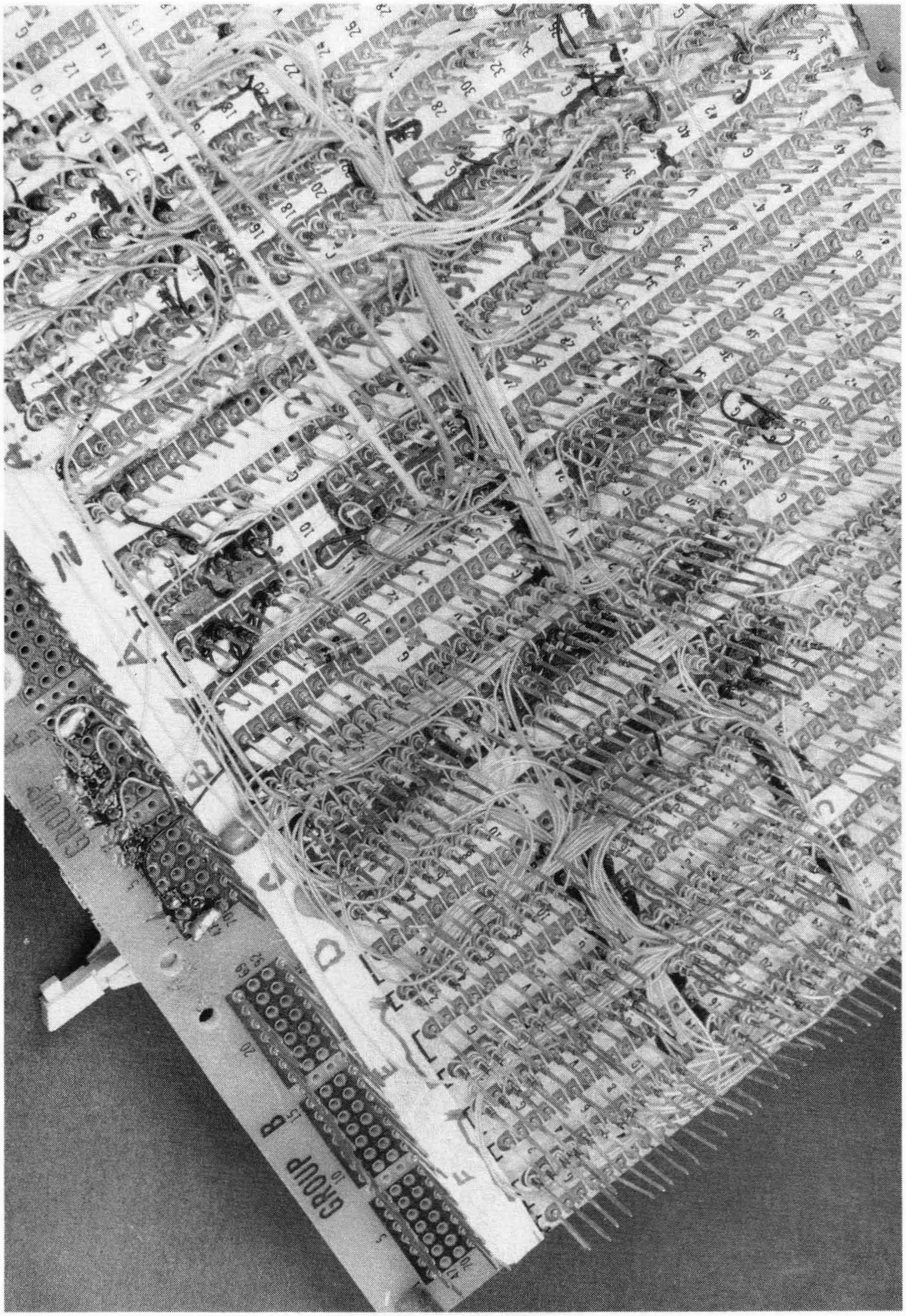
Additional Comments on Breadboarding

This section contains, in visual form, commentary on some of the breadboards of the circuits described in the text. The breadboards appear in roughly corresponding order to their text presentation and comments are brief but hopefully helpful. The bit pushers have commented software; why not commented hardware?



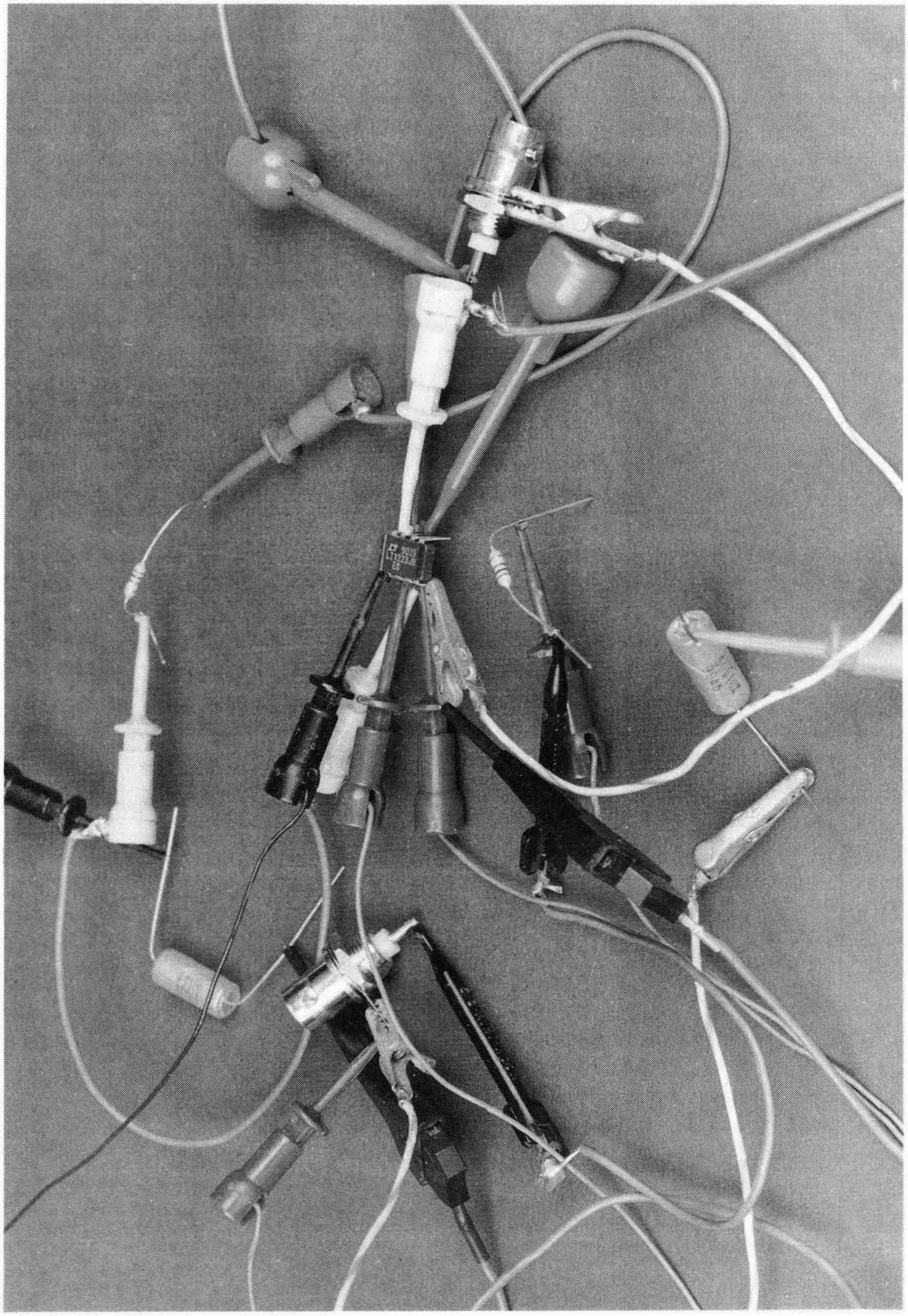
LTAN47 • TAF1

Figure F1. No


GROUP
B
GROUP

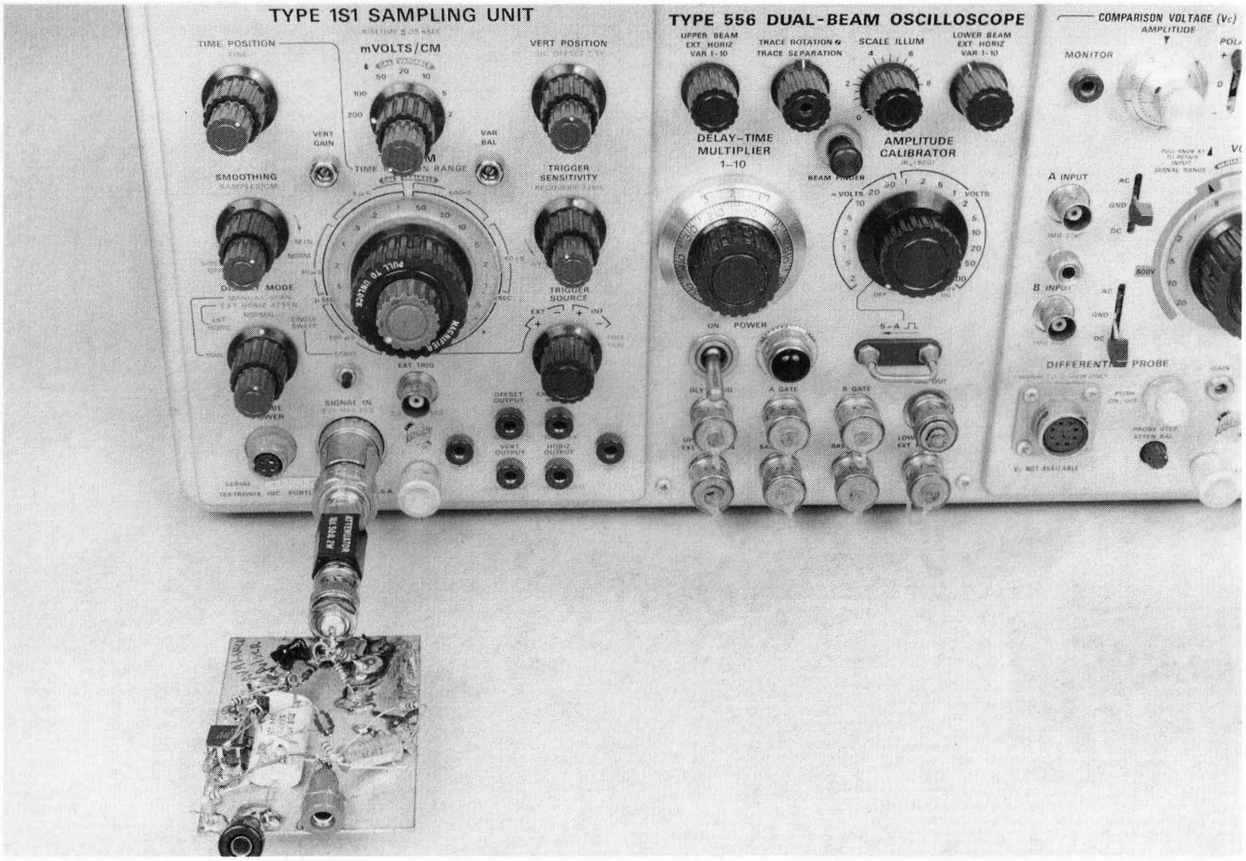
LTAN47 • TAF2

Figure F2. No



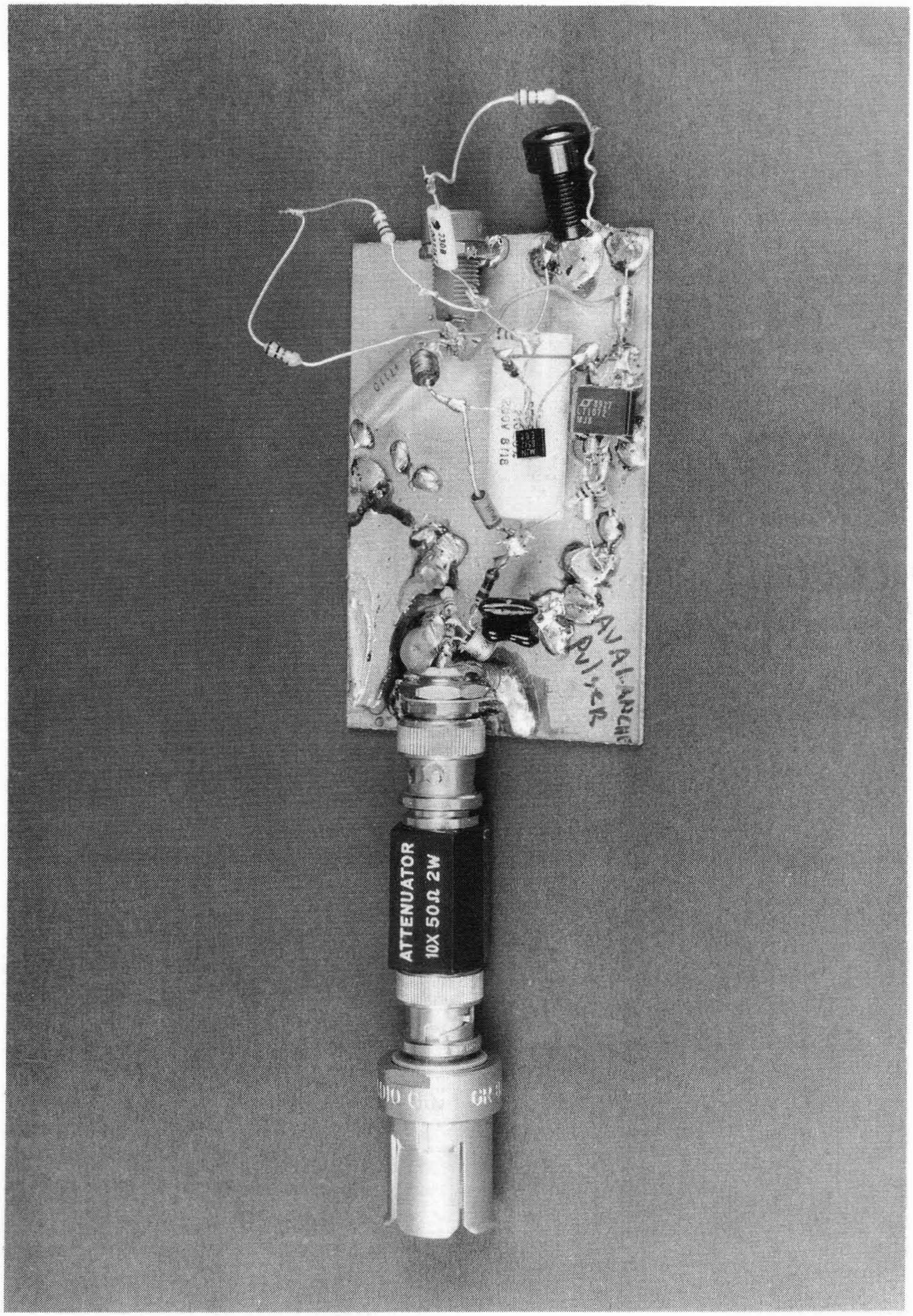
LTAN47 • TAF3

Figure F3. No


TYPE 1S1 SAMPLING UNIT
TIME POSITION
mVOLTS/CM
VERT POSITION
VERT GAIN
VAR BAL
SMOOTHING
TRIGGER SENSITIVITY
TRIGGER SOURCE
PULL TO UNLOCK
MAGNIFIER
EXT TRIG
SIGNAL IN
OFFSET OUTPUT
VERT OUTPUT
HORIZ OUTPUT
TEKTRONIX, INC.
TYPE 556 DUAL-BEAM OSCILLOSCOPE
UPPER BEAM EXT HORIZ VAR 1-10
TRACE ROTATION
TRACE SEPARATION
SCALE ILLUM
LOWER BEAM EXT HORIZ VAR 1-10
DELAY-TIME MULTIPLIER 1-10
BEAM FINDER
AMPLITUDE CALIBRATOR
mVOLTS
VOLTS
ON POWER
A GATE
B GATE
OUT
COMPARISON VOLTAGE (Vc)
AMPLITUDE
MONITOR
A INPUT
B INPUT
AC
GND
DC
DIFFERENTIAL PROBE
GAIN
V_c NOT AVAILABLE
ATTENUATOR

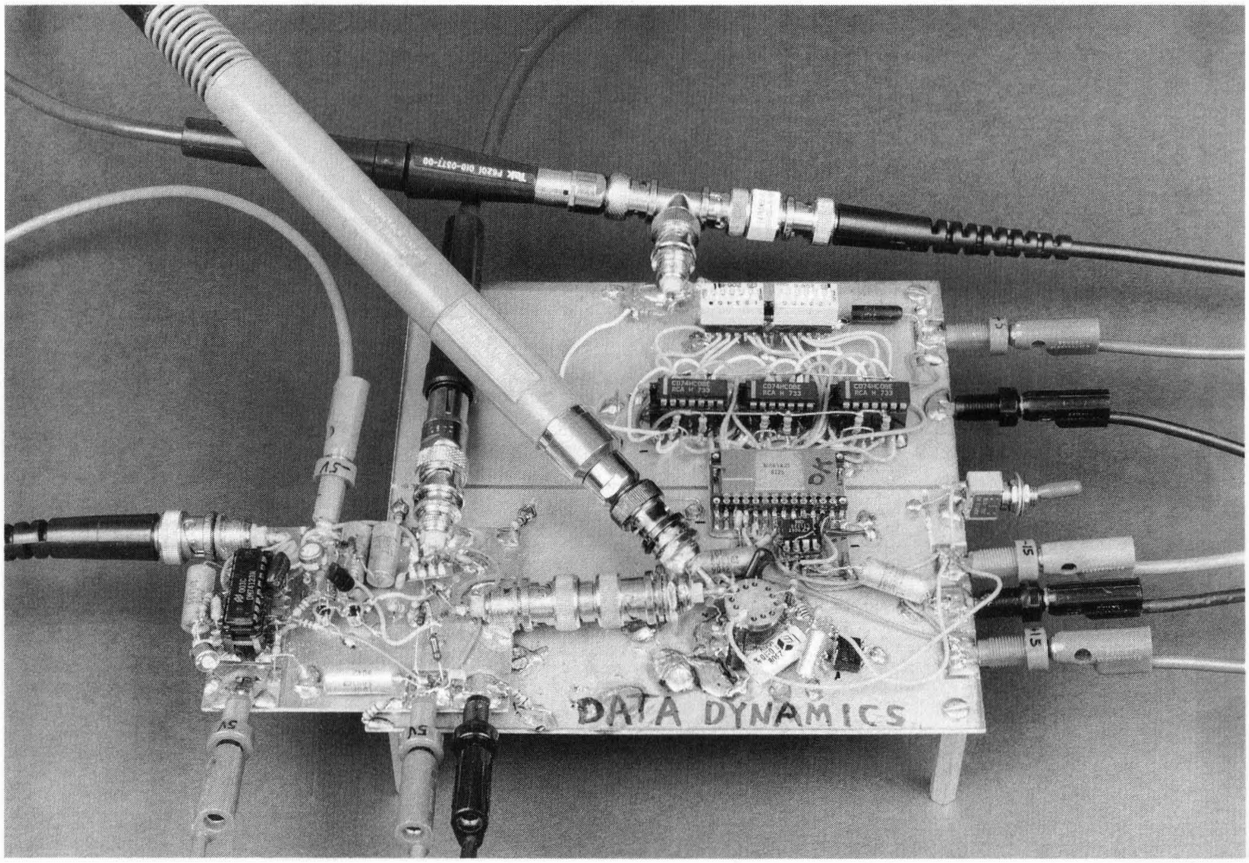
LTAN47 • TAF4

Figure F4. Prototype Avalanche Pulser Under Test. Direct Connection to Oscilloscope Eliminates Cable or Probe Effects


ATTENUATOR
10X 50Ω 2W
AVALANCHE
Pulser

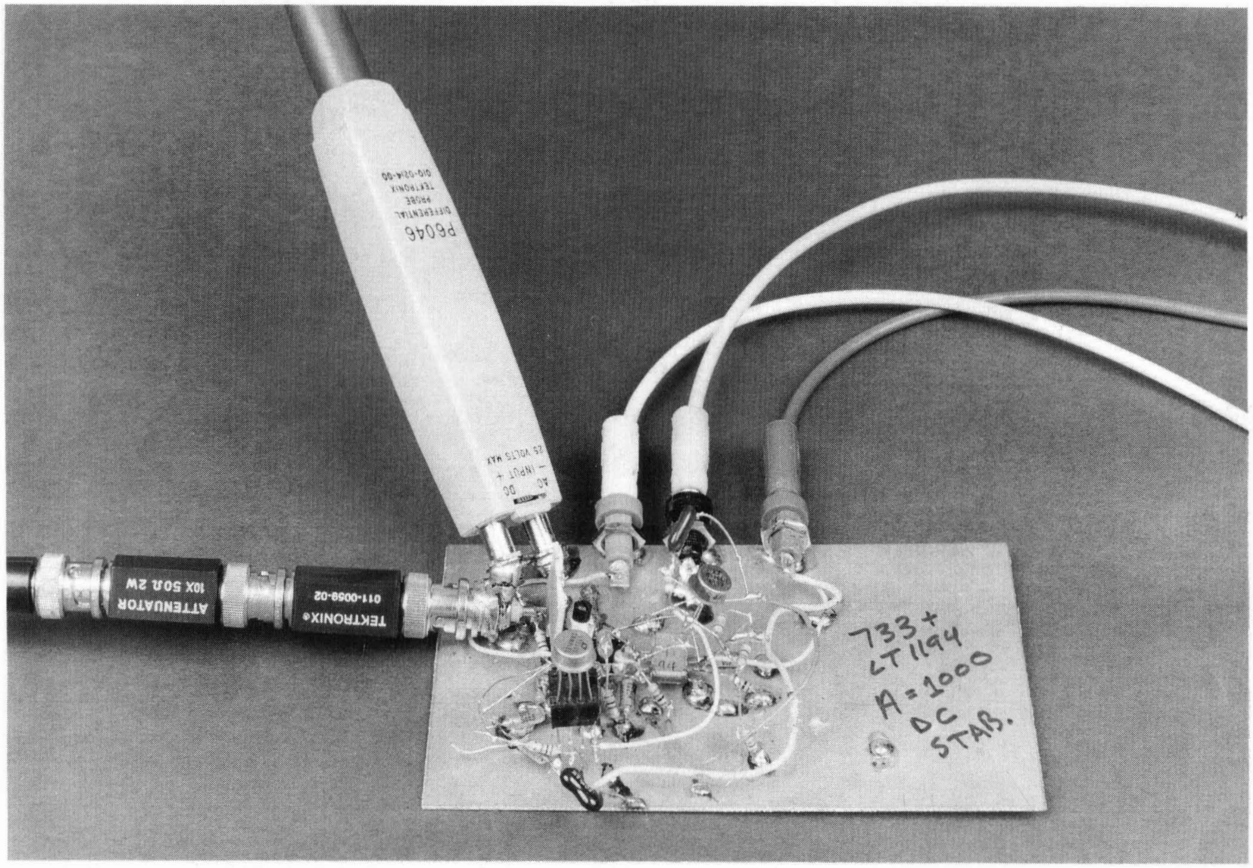
LTAN47 • TAF5

Figure F5. Close-Up of Prototype Avalanche Pulse Generator. DC Bias Generator (Right Side of Board) is Carelessly Wired, but Pulse Forming Circuitry (Left Side of Board, by BNC Connector) is Carefully and Tightly Wired



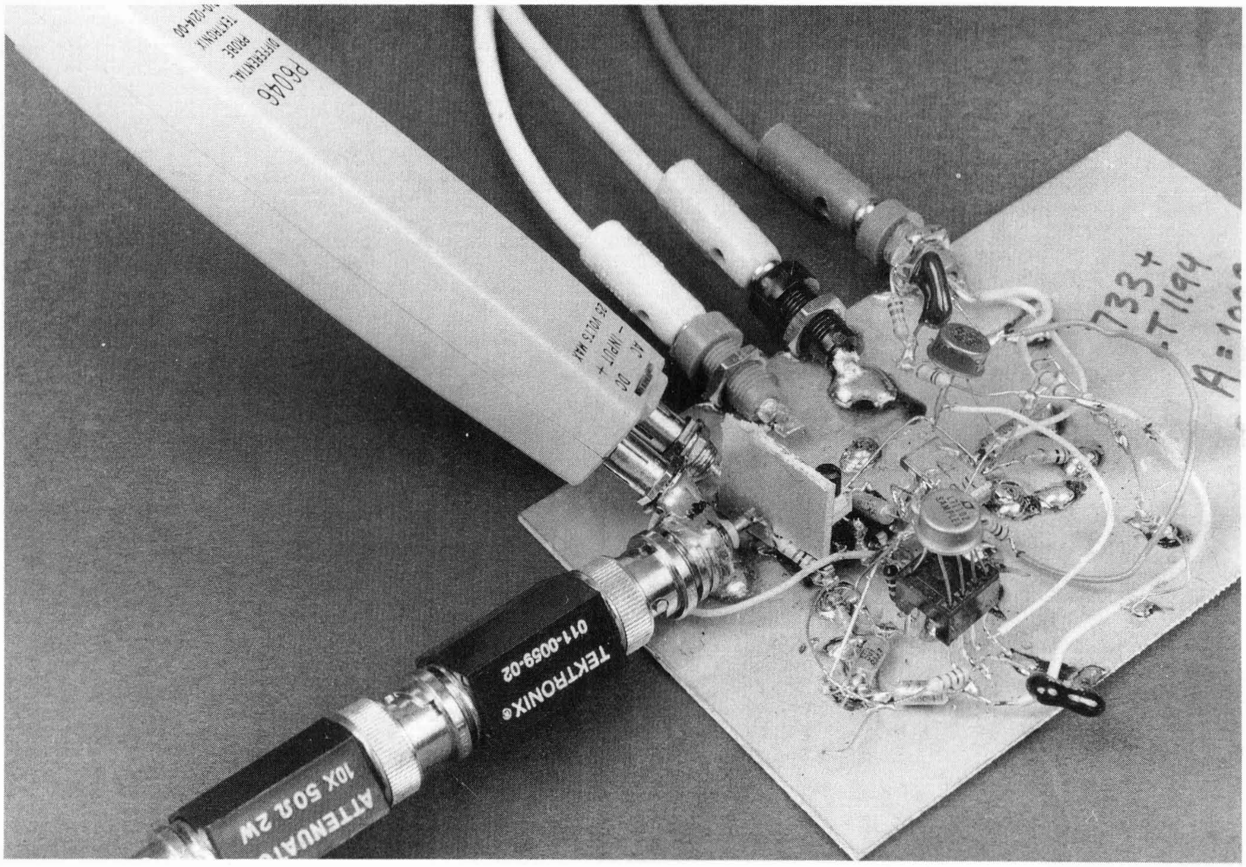
LTAN47 • TAF6

Figure F6. The Settling Time Test Fixture Described in Appendix B. DAC and Amplifier are in Center Right of Photo. Note Break in Clad Separating Analog and Digital Grounds and Attention to Layout in Switching Bridge (Lower Left). Switching Bridge is Returned Separately to Ground — Its Board is Mechanically Stood-Off From Main Board by 10MΩ Resistors. Output Section, Driving the Large P6032 Follower Probe, is at Lower Right


733+
LT1194
A=1000
DC
STAB.
P6046
ATTENUATOR
10X 50Ω 2W
TEKTRONIX
011-0059-02

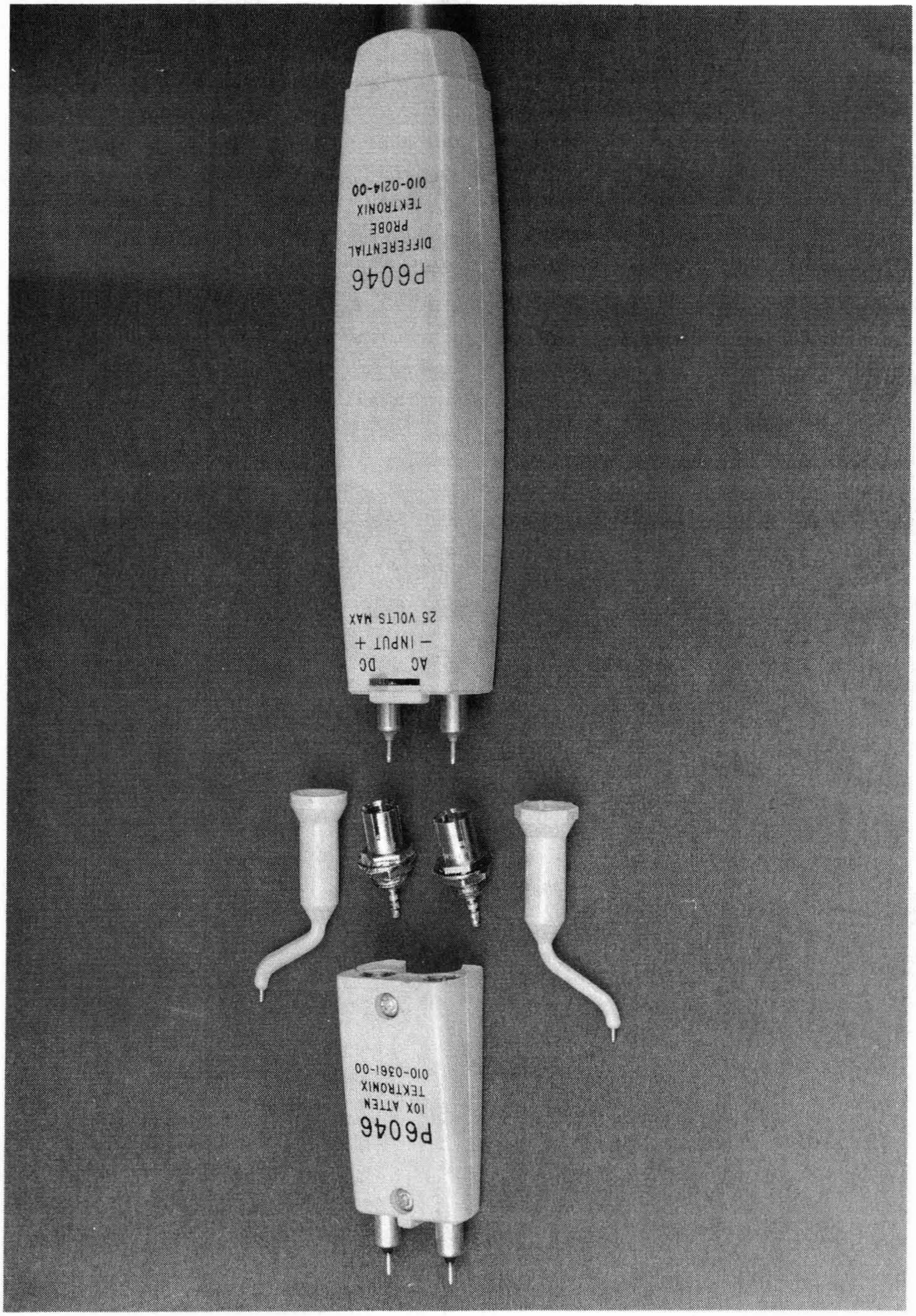
LTAN47 • TAF7

Figure F7. The X1000 38MHz Differential Amplifier. DC and Low Frequency Electronics use Sockets (Foreground) and Air Wire Techniques (Center Right) for Easy and Fast Breadboarding. Wideband Circuitry Hugs the Ground Plane, and is Clustered Near the Input BNC


P6046
DIFFERENTIAL
PROBE
TEKTRONIX
TEKTRONIX®
011-0059-02
10X 50Ω 2W
ATTENUATO
733+
LT1194
A=1000

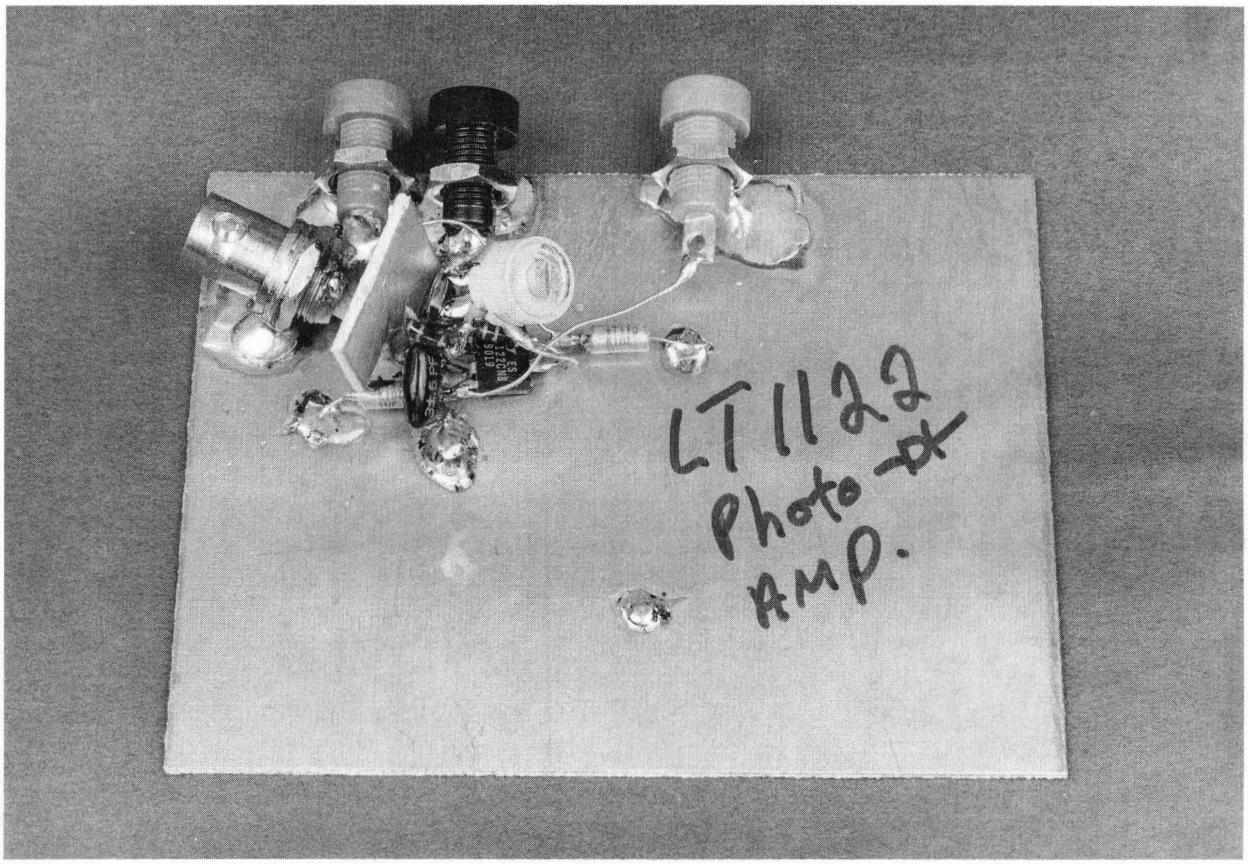
LTAN47 • TAF8

Figure F8. Input Detail of X1000 Differential Amplifier. Clad Shield (Center Right) Prevents BNC Radiation from Corrupting Low Level Circuitry. Differential Probe Verifies Fidelity of 2.5mV Pulse Out of the X100 Attenuator Stacked Sections. Note DIP Packages Hugging Ground Plane, While Cans Operating at Low Frequency are Carelessly Wired


P6046
DIFFERENTIAL
PROBE
TEKTRONIX
010-0214-00
25 VOLTS MAX
– INPUT +
AC
DC
P6046
10X ATTEN
TEKTRONIX
010-0361-00

LTAN47 • TAF9

Figure F9. The Differential Probe and Its 10X Attenuator. Offset Probe Tips are Convenient for Making Differential Connections, but Sockets Maintain a True Coaxial Environment and are Preferred



LTAN47 • TAF10

Figure F10. The Photodiode Amplifier Layout Emphasizes Low Capacitance at Amplifier (Located Below Trimmer Capacitor, Photo Center Upper Left). Vertical Guard Shield Breaks Up BNC Radiation; was Used When Photo Input was Simulated with a Pulse Generator

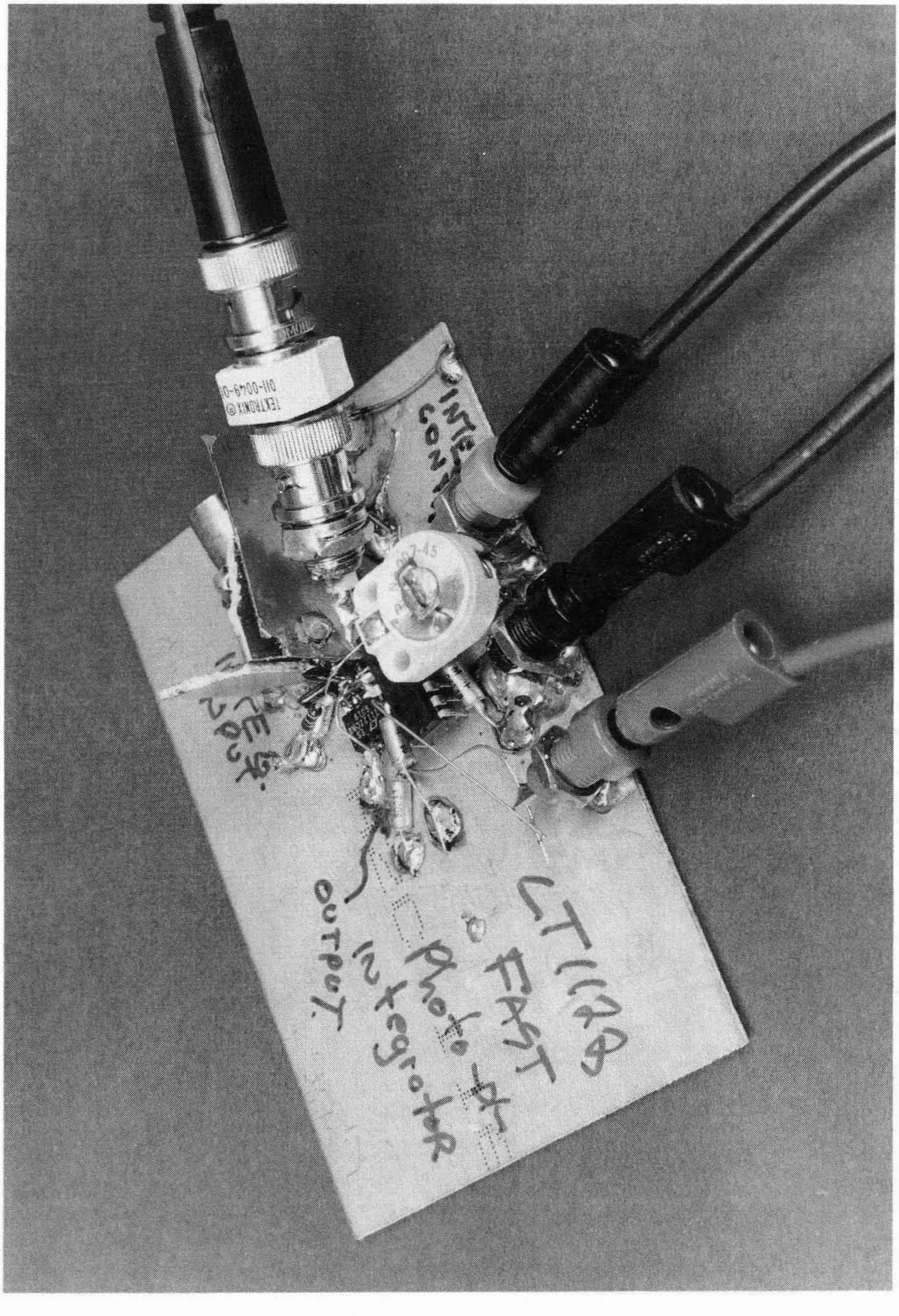
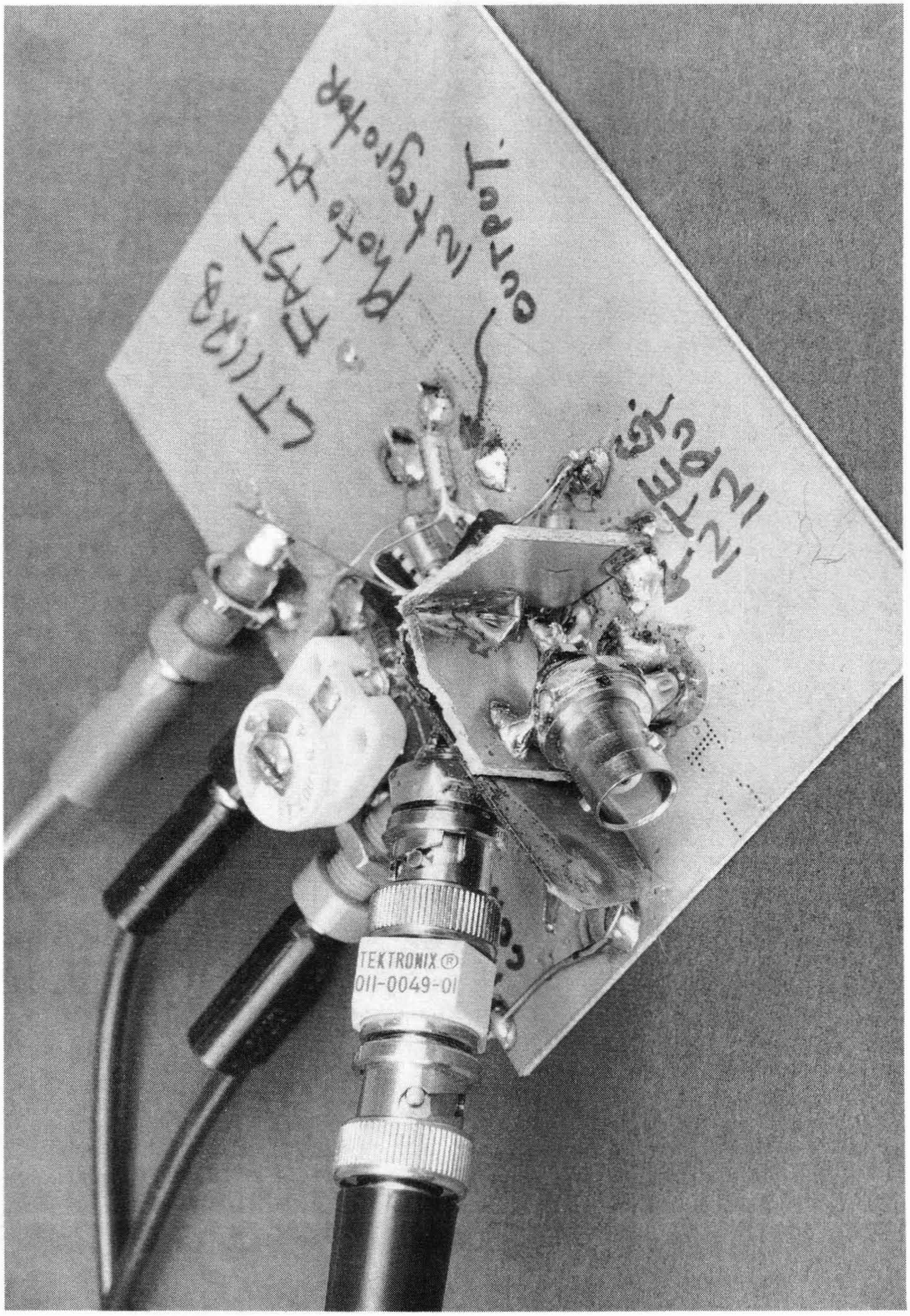
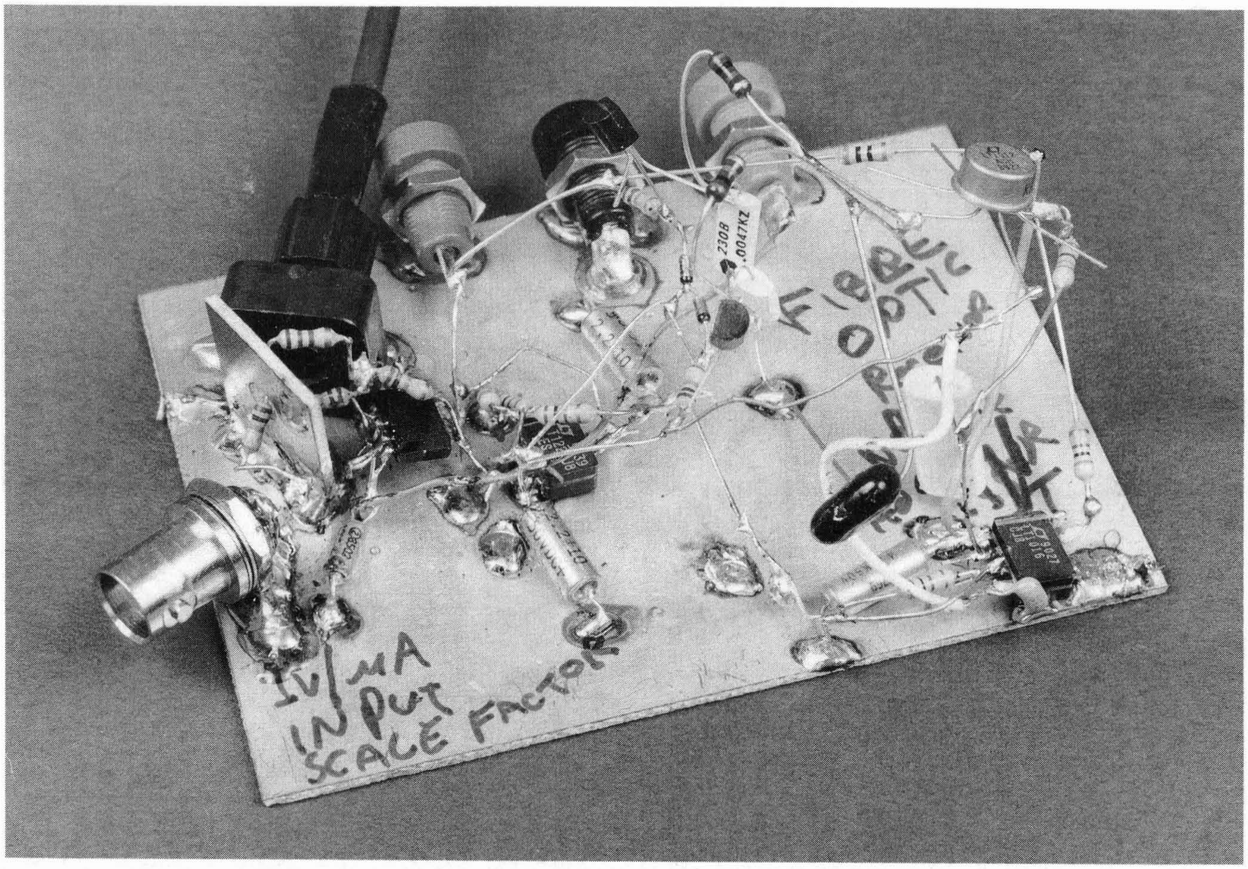

LTAN47 • TAF11
TEKTRONIX
011-0049-0
INTE
CONT
LT1128
FAST
Photo-dx
Integrator
output

Figure F11. Fast Photo Integrator Under Test with Pulse Generator Simulating a Photo Input. BNC Radiation is Controlled with Extensive Shielding at Integrator Input (Just Visible Upper Center). Control Input (Cable Connected BNC) is Less Critical; Does Not Require Shielding


LT1133
FAST
Photo Int
12 Integrator
output
TEKTRONIX ®
011-0049-01

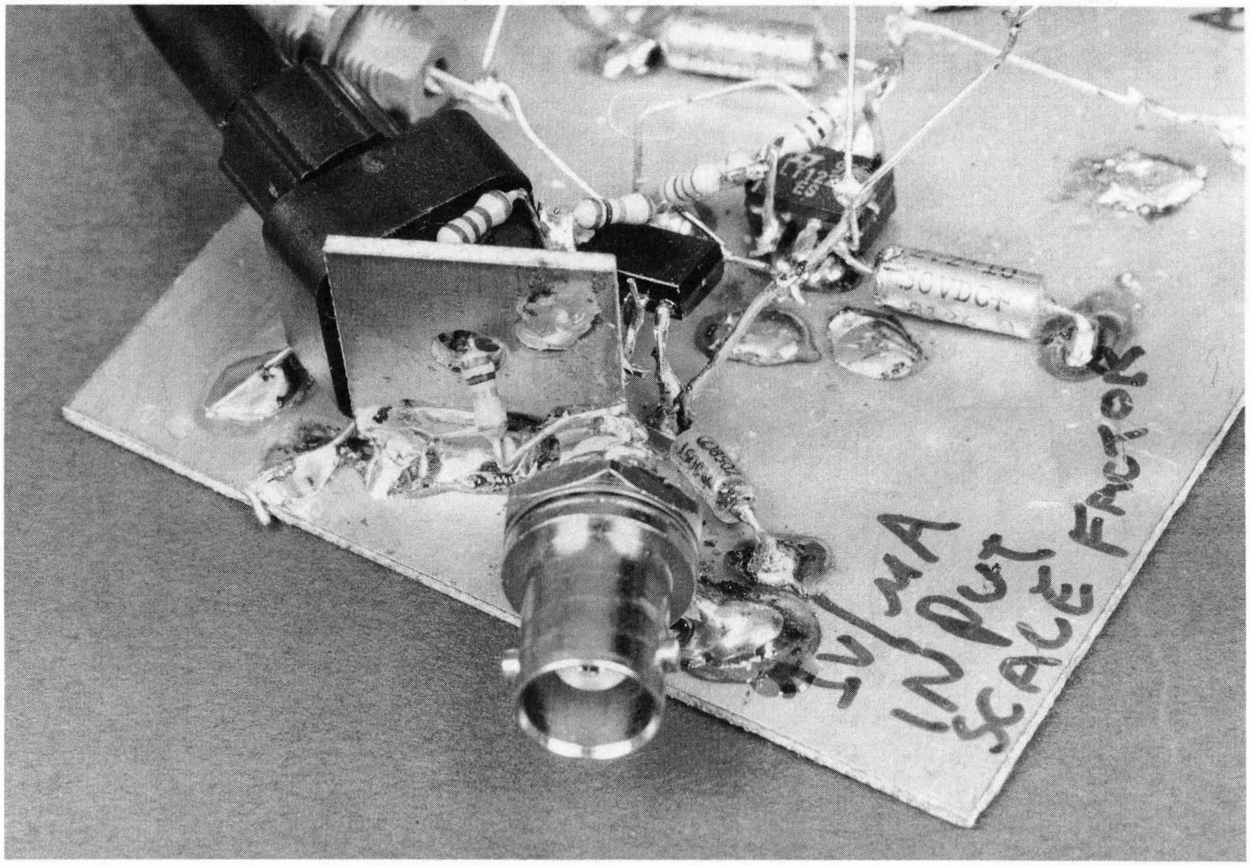
LTAN47 • TAF12

Figure F12. Photo Integrator Details. Integrator Input BNC is Fully Shielded From Integrator Amp — 1pF Coupling From BNC Output to Summing Point will Cause Excessive Peaking. Amplifier and Switch ICs are Just Visible


1V/MA
INPUT
SCALE FACTOR
FIBER
OPTIC
2308
.0047KZ

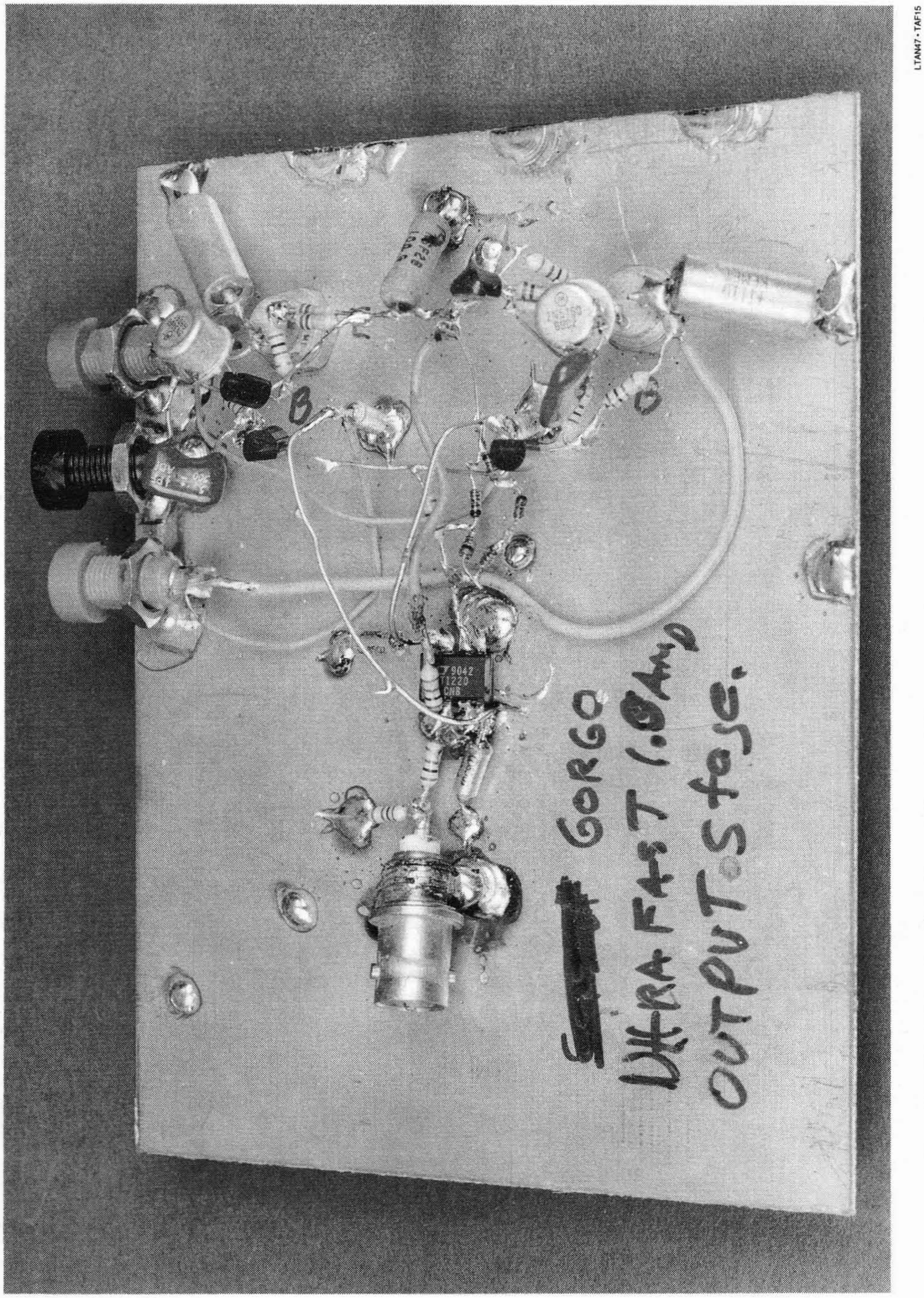
LTAN47 • TAF13

Figure F13. The Adaptive Trigger Fiber Optic Receiver. BNC Photo-Simulation Input and Fiber Optic Line Both Connected. Low Frequency Wiring is Haphazardly Constructed While High Frequency Sections are Tight and Hug the Ground Plane. Note Vertical Shield at Photo-Simulation Input BNC



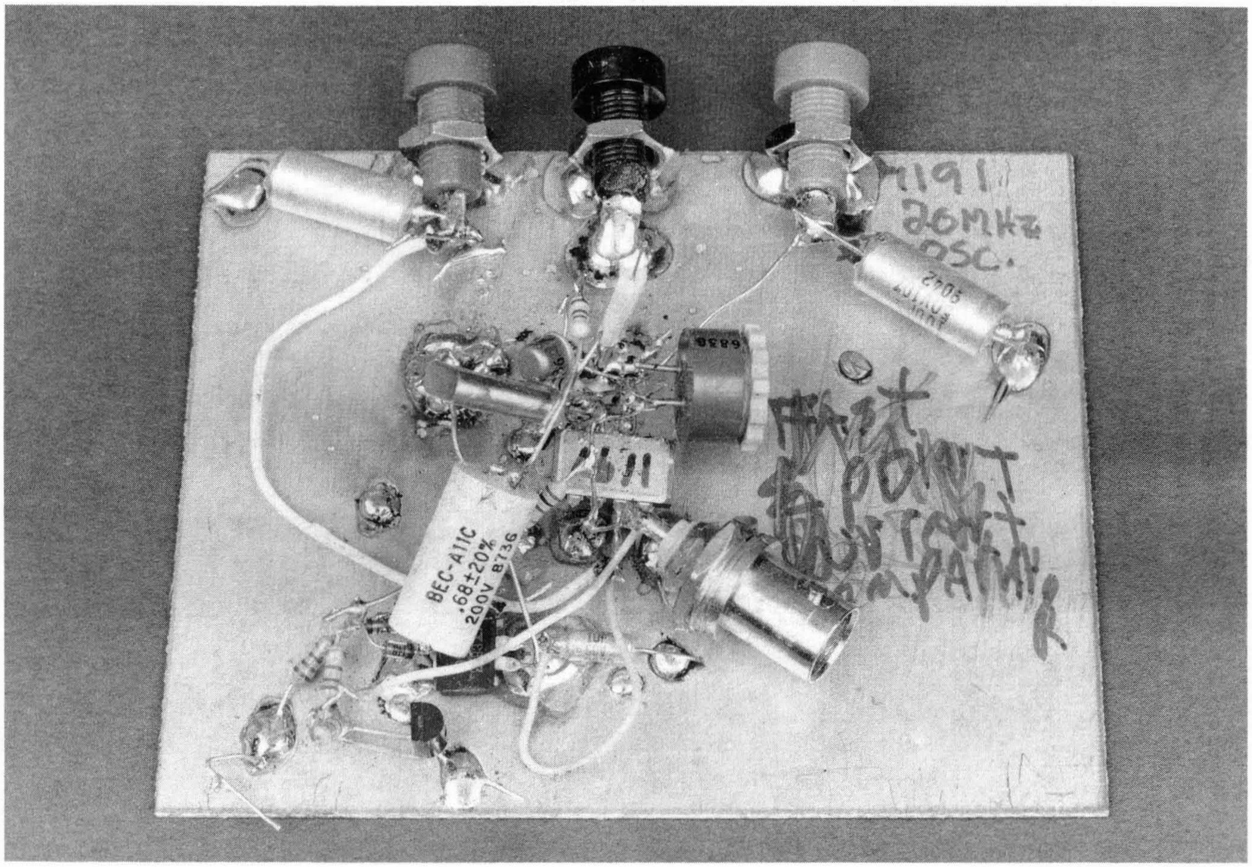
LTAN47 • TAF14

Figure F14. Detail of the Fiber Optic Receiver's Photo-Simulation BNC Input. Resistor From BNC is Routed Through a Small Hole in Vertical Shield, Minimizing Capacitance. Another Resistor on the Shield's Other Side Divides Effects of Residual Capacitance to Keep Summing Point Clean


GORGO
ULTRA FAST 1.0 AMP
OUTPUT STAGE.
B

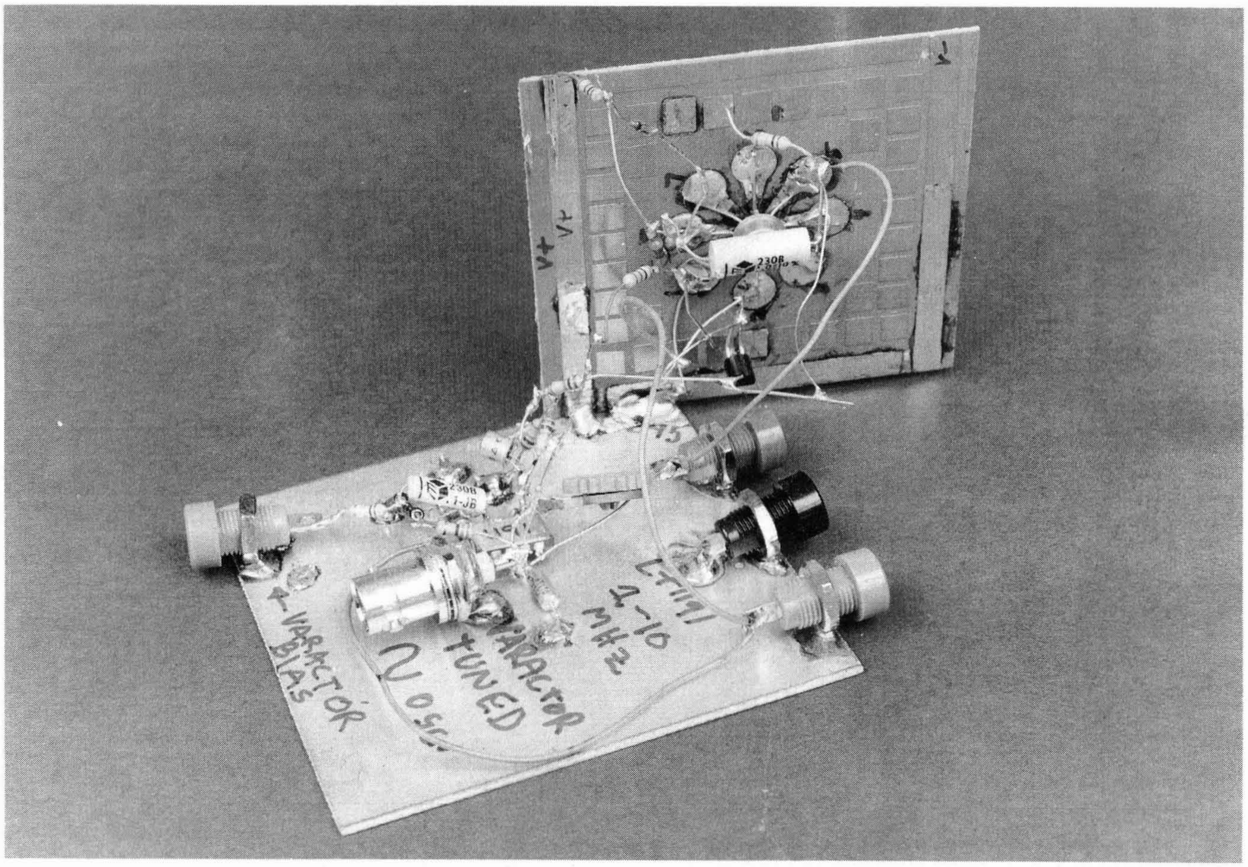
LTAN47 • TAF15

Figure F15. The 1A Booster. Note Heavy Bypassing Right at the Output Power Transistors (Both Stud-Mounted to Clad). Local Compensation Capacitors (Right Side Upper and Lower) Have Short Leads


20MHz
OSC.
BEC-A11C
.68±20%
200V B736

LTAN47 • TAF16

Figure F16. 20MHz Sine Wave Crystal Oscillation. DC-AGC Section is at Lower Left, Oscillator is in Center. Control FET is Located at Oscillator Amplifier. Slow Gate Control Signal Arrives via Long-Leaded Resistor, (Photo Center Upper Left)


LT1191
2-10
MHz
VARACTOR
TUNED
∿ OSC
+ VARACTOR
BIAS
V+
V+

LTAN47 • TAF17

Figure F17. The Varactor Tuned Wien Bridge. DC-AGC Section is on Vertical Board — High Frequency Section Hugs the Ground Plane. Control FET (Center Left), Located at Oscillator, is Biased From a Long Line Originating on AGC Board. Note FET Gate Resistor is Located at FET, Not DC Board. Oscillator Output Receives Reverse Treatment

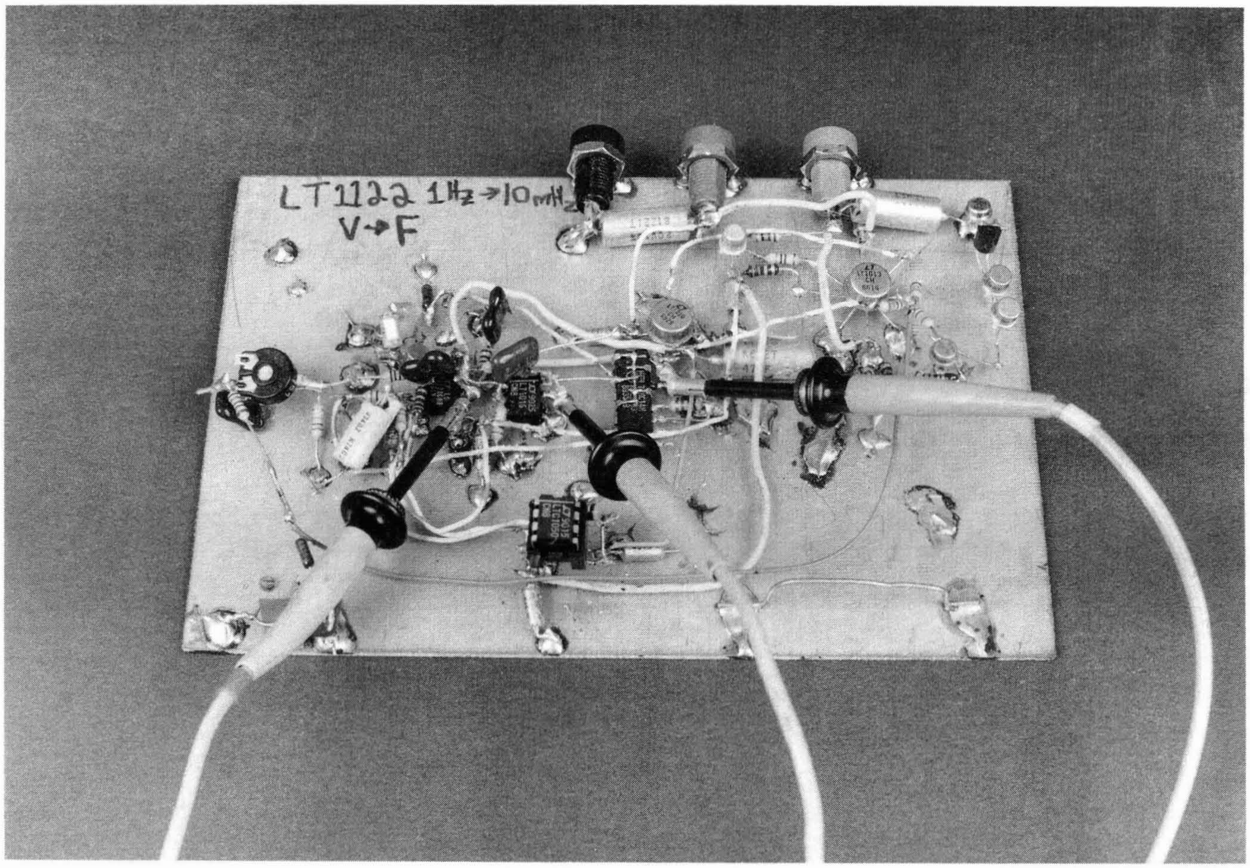
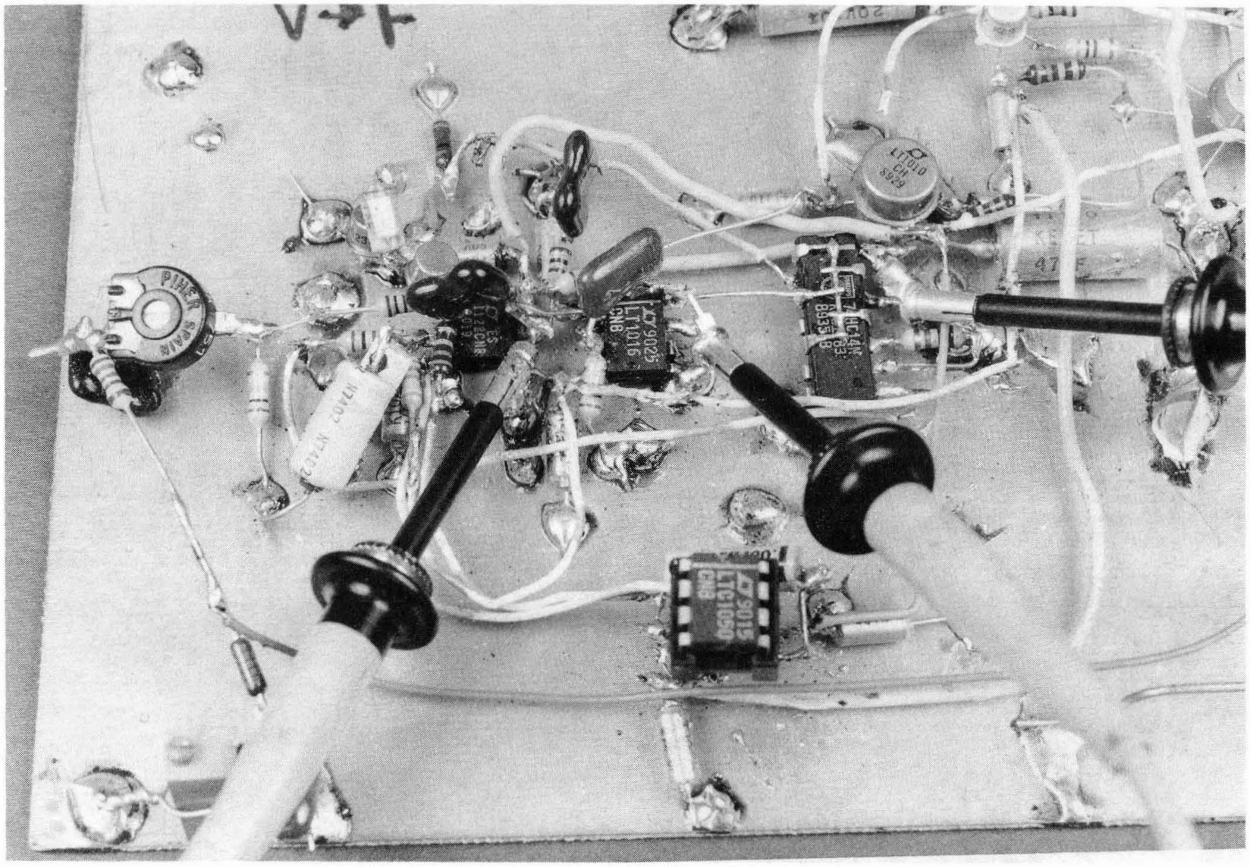
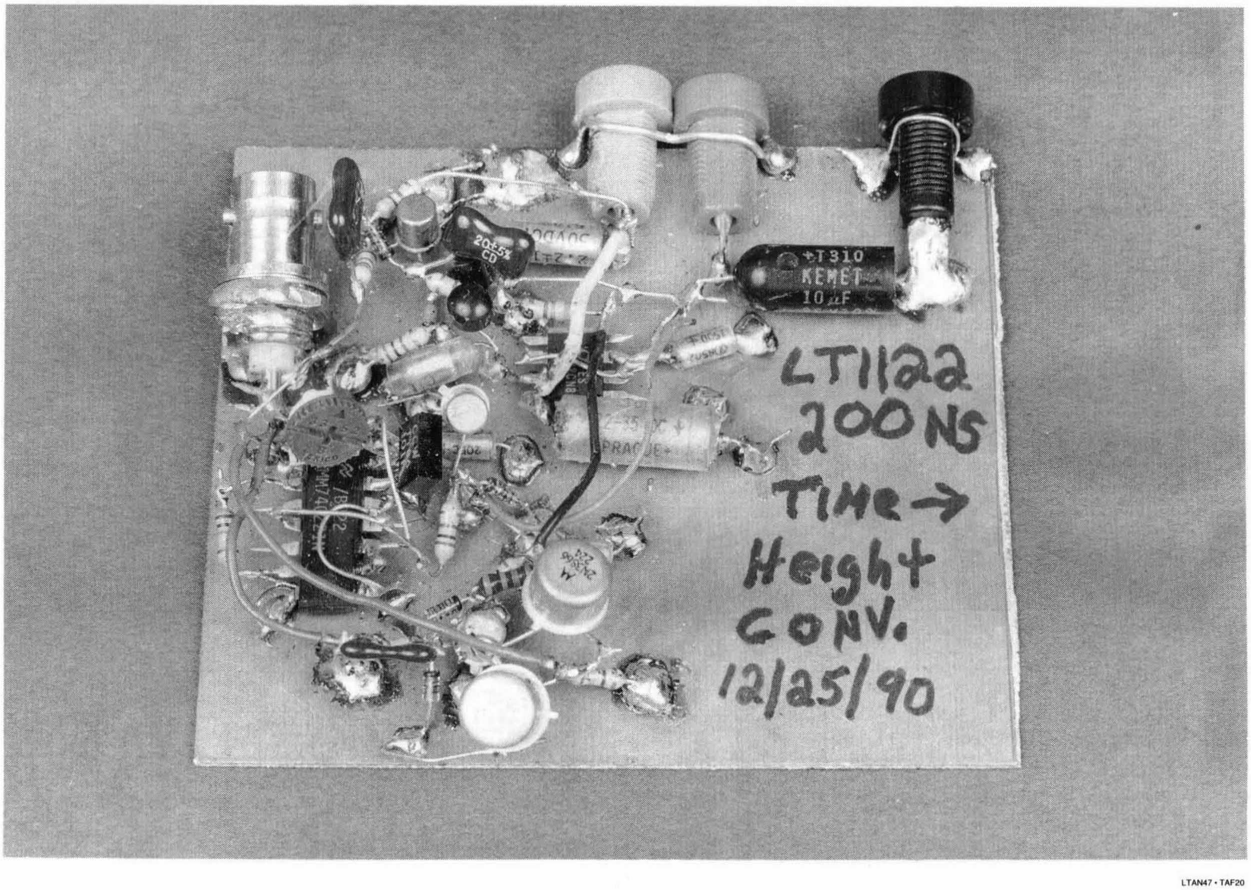


Figure F18. The 1Hz-10MHz V to F Breadboard with Probes Attached. DC Servo Amplifier is Socketed, with Long Leads. Reference Section, Starting at Breadboard (Upper Right), Works Toward Reference Switch (Large DIP at Board Center). Note Very Tight Layout in Amplifier-Comparator Region (Board Left Center)


+V
PIHER
GAIN
LT9025
LT1016
CN8
LT9015
LTC1050
CN8
LT1010
CH
8929

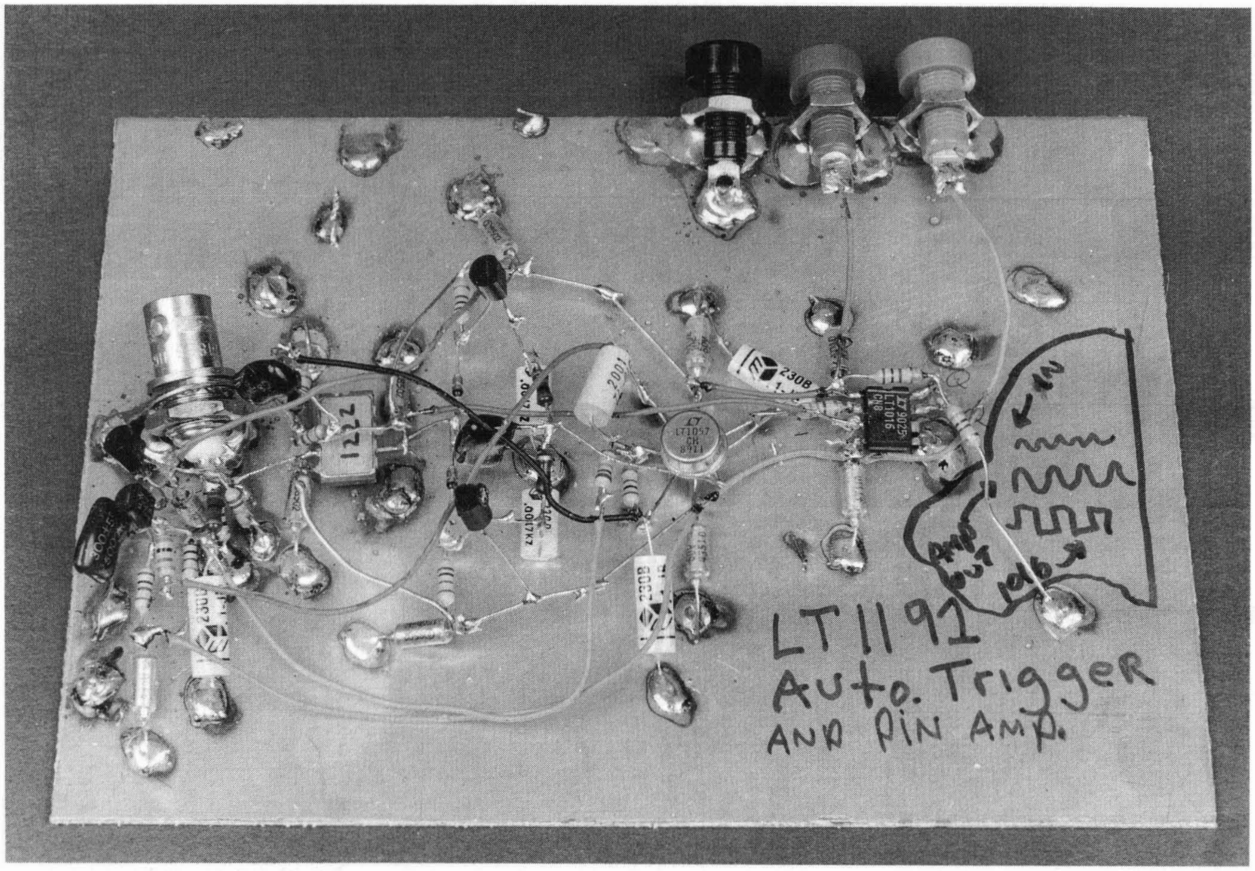
LTAN47 • TAF19

Figure F19. Details of 1Hz-10Mhz V to F High Speed Section. LT1122 Integrator is Just Visible Under its Associated Discrete Components. Summing Point (Left Side of Amplifier) is Layout's Electrical Center. LT1016 Wiring is Also Very Tight Except for its Output Which Goes to Reference Switch. DC Servo Amplifier Sleeps in its Socket. Note Probe Tip Connectors


T310
KEMET
10 µF
20±5%
CD
LT1122
200NS
Time →
Height
CONV.
12/25/90

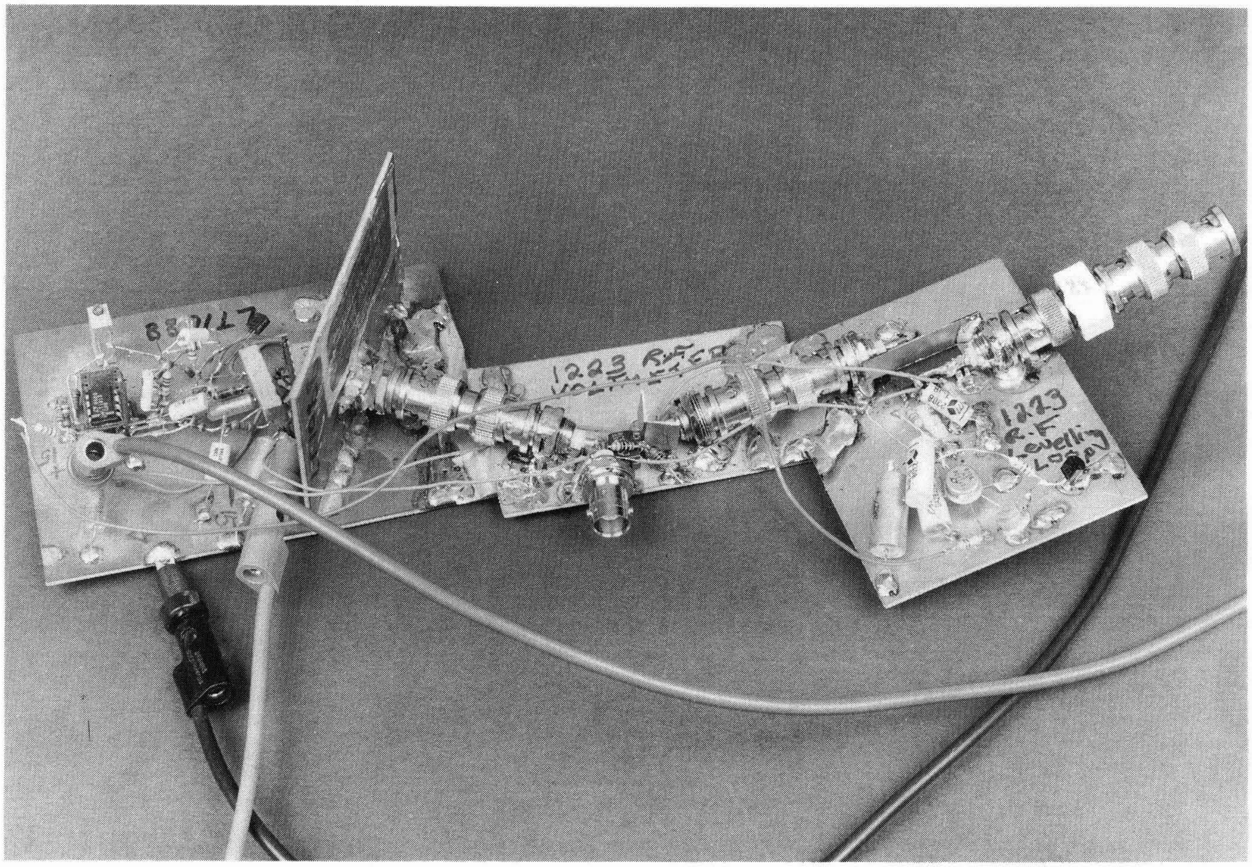
LTAN47 • TAF20

Figure F20. The Time-to-Height Converter. Switched Current Source, (Board Center Left), has Very Tight Layout. Follower Amplifier is at Board Upper Center. Major Components (in Order from Top to Bottom), Include Current Source Switch Transistor, Current Source Transistor (Black Case), Integrator Capacitor (Silver) and Reset Transistor. Note Short Connection to Amplifier Input Pin


LT1191
Auto. Trigger
AND PIN AMP.
IN
AMP OUT
1016
LT1016
LT1057

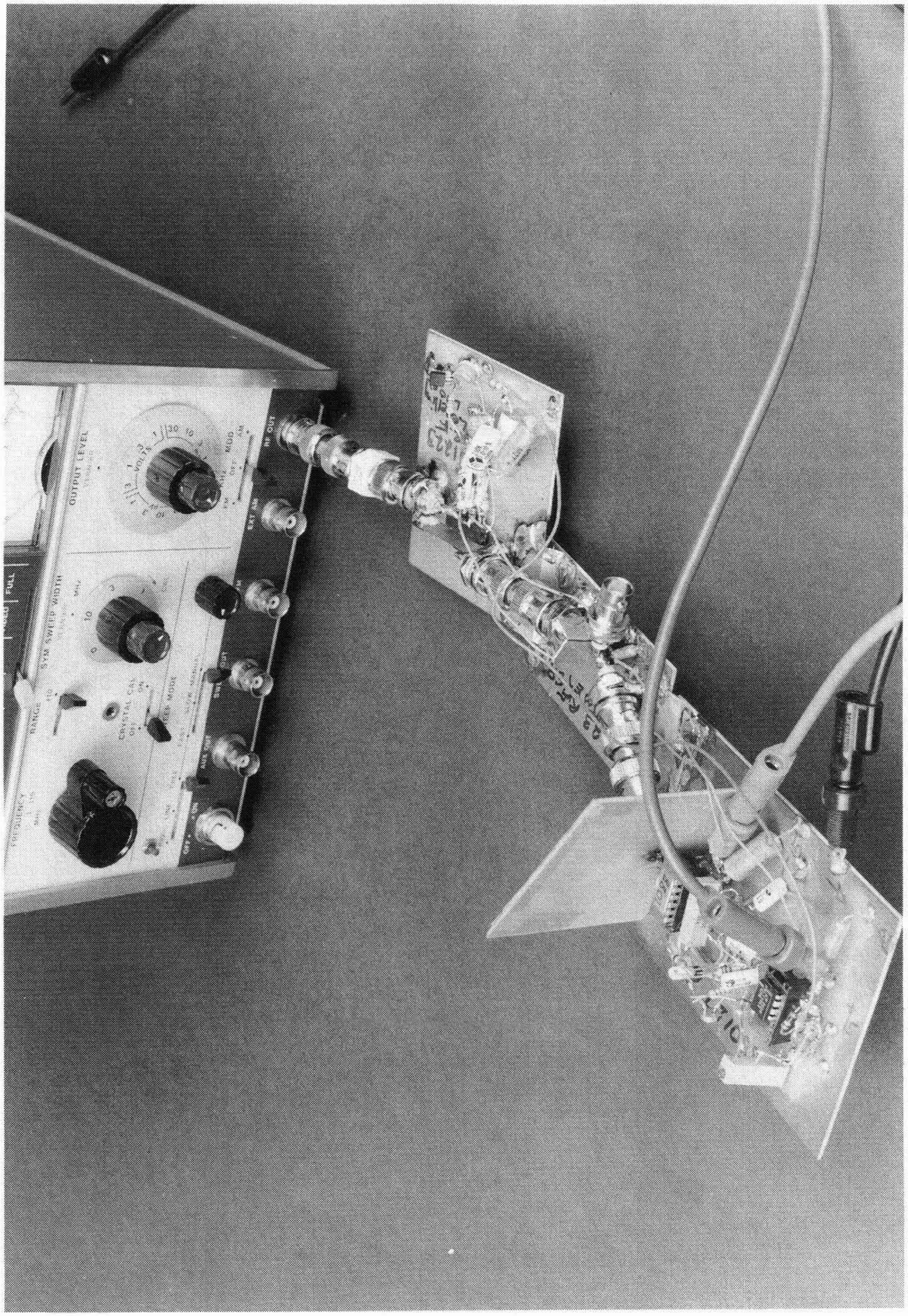
LTAN47 • TAF21

Figure F21. The Automatic Trigger. Low Frequency Automatic Level Section is Spread Out, (Right Side of Board). Wideband Circuitry Hugs Ground Plane and is Located Near Input BNC. Amplifier's Low Impedance, Fast Output Feeds LT1016 Output Comparator Over a Relatively Long Wire Run, Routed Through Insensitive Section of DC Circuitry



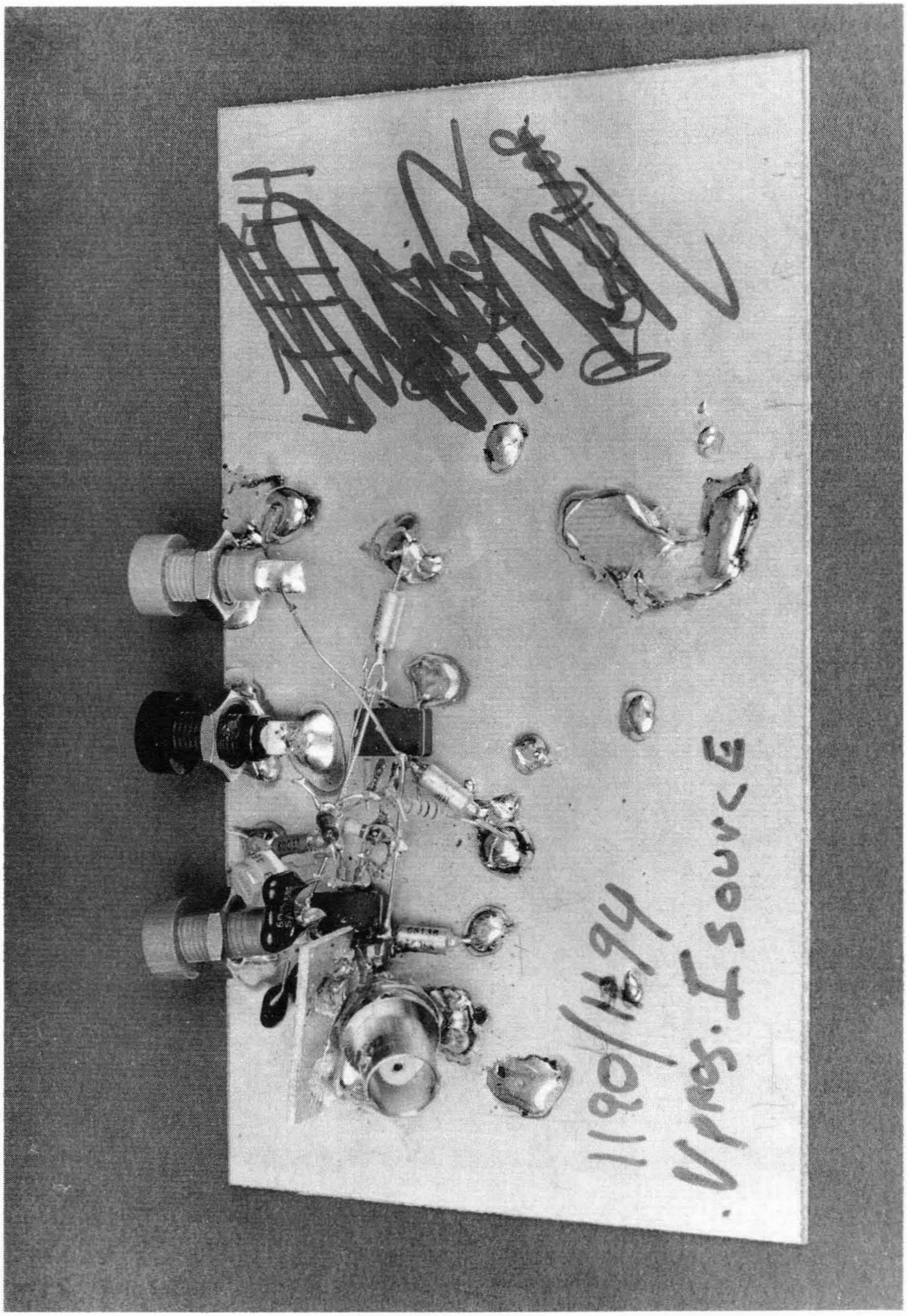
LTAN47 • TAF22

Figure F22. The RF Leveling Loop. The RMS to DC Converter (Left Board) was Built First, Then the RF Pre-Amp (Center Board) and Finally the Multiplier-Servo Board. Each Board's Performance was Verified Before Joining Them. Note Copper Tape Maintaining Ground Plane Integrity Between Boards


OUTPUT LEVEL
VOLTS
SYM SWEEP WIDTH
MHz
RANGE
CRYSTAL CAL
OFF ON
FREQUENCY
RF OUT
EXT AM

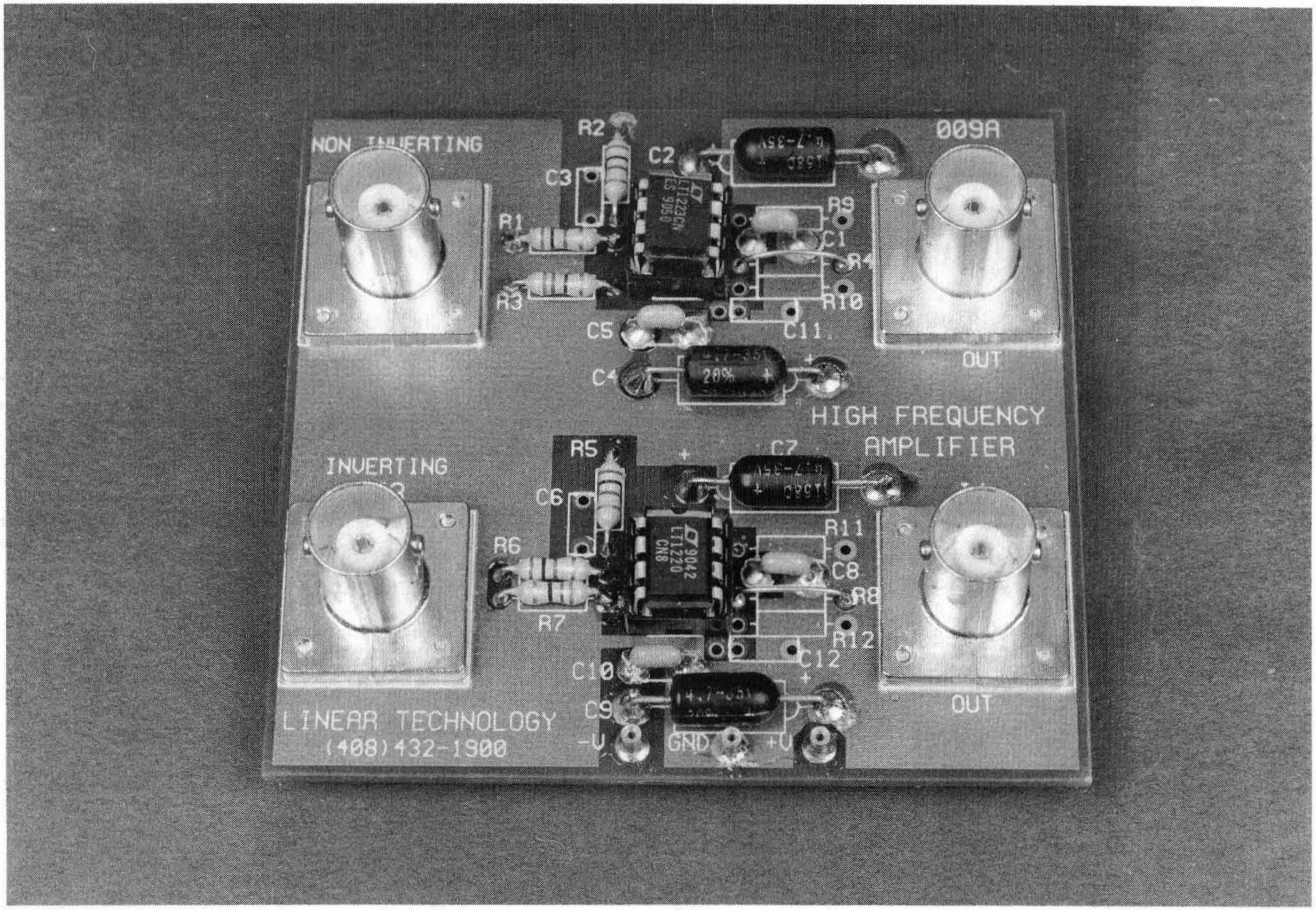
LTAN47 • TAF23

Figure F23. RF Leveling Loop Attached Directly to the Test Generator. Cable Uncertainties are Eliminated Because There is No Cable



LTAN47 • TAF24

Figure F24. The Voltage Controlled Current Source. Vertical Shield (Upper Left) Absorbs Input BNC Radiation. Amplifier-Loop Compensation Components are Located Directly at Amplifier (Behind Shield)


NON INVERTING
INVERTING
OUT
OUT
009A
HIGH FREQUENCY
AMPLIFIER
LINEAR TECHNOLOGY
(408) 432-1900
LT1223CN
LT1220
CN8
R1
R2
R3
R4
R5
R6
R7
R8
R9
R10
R11
R12
C1
C2
C3
C4
C5
C6
C7
C8
C9
C10
C11
C12
-V
GND
+V

LTAN47 • TAF25

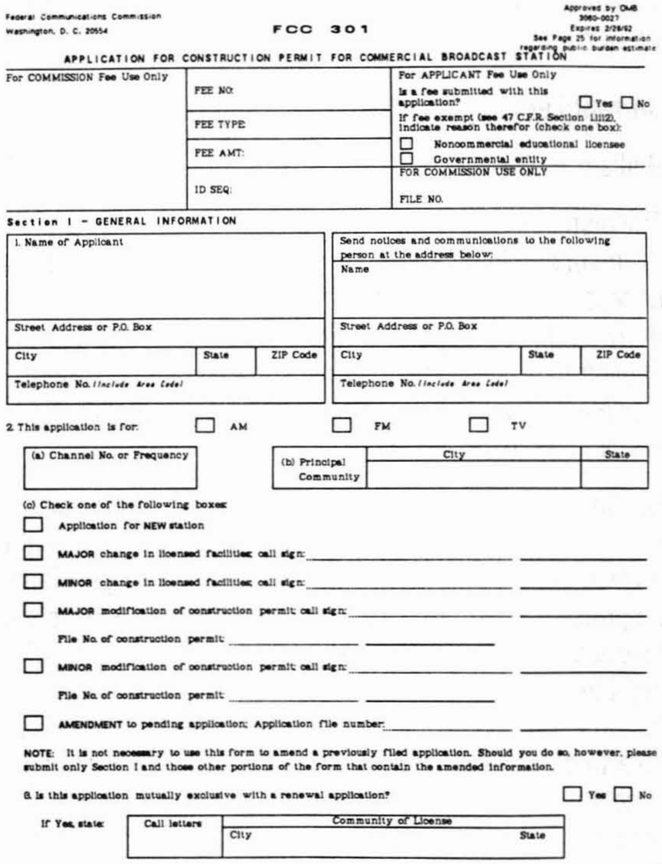
Figure F25. The Good Life. The High Frequency Amplifier Demonstration Board Discussed in Appendix I. Sockets are a Compromise Between Best Performance and Flexibility

APPENDIX G

FCC Licensing and Construction Permit Applications for Commerical AM Broadcasting Stations

In accordance with the application for Figure 116's circuit, and our law-abiding nature, find facsimiles of the appropriate FCC applications below. The complete forms are available by writing to:

Federal Communications Commission
Washington, D.C. 20554



Federal Communications Commission
Washington, D. C. 20554

FCC 301

Approved by OMB
3060-0027
Expires 2/28/92
See Page 25 for information regarding public burden estimate

APPLICATION FOR CONSTRUCTION PERMIT FOR COMMERCIAL BROADCAST STATION

For COMMISSION Fee Use Only

FEE NO:

FEE TYPE:

FEE AMT:

ID SEQ:

For APPLICANT Fee Use Only

Is a fee submitted with this application? ☐ Yes ☐ No

If fee exempt (see 47 C.F.R. Section 1.1112), indicate reason therefor (check one box):

☐ Noncommercial educational licensee

☐ Governmental entity

FOR COMMISSION USE ONLY

FILE NO.

Section I – GENERAL INFORMATION

1. Name of Applicant

Street Address or P.O. Box

City | State | ZIP Code

Telephone No. (Include Area Code)

Send notices and communications to the following person at the address below:

Name

Street Address or P.O. Box

City | State | ZIP Code

Telephone No. (Include Area Code)

2. This application is for: ☐ AM ☐ FM ☐ TV

(a) Channel No. or Frequency

(b) Principal Community | City | State

(c) Check one of the following boxes:

☐ Application for NEW station

☐ MAJOR change in licensed facilities; call sign: ________ ________

☐ MINOR change in licensed facilities; call sign: ________ ________

☐ MAJOR modification of construction permit; call sign: ________ ________

File No. of construction permit: ________ ________

☐ MINOR modification of construction permit; call sign: ________ ________

File No. of construction permit: ________ ________

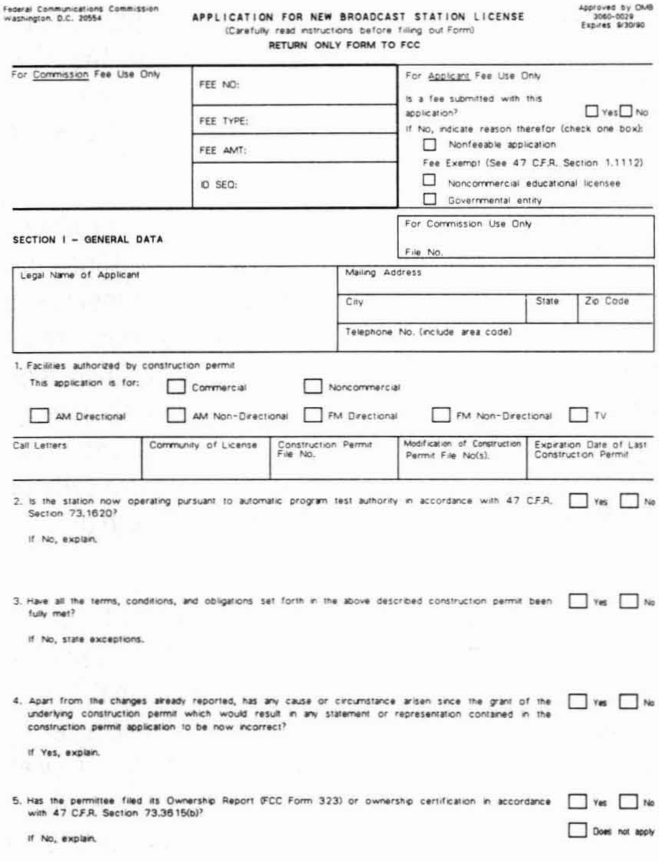
☐ AMENDMENT to pending application; Application file number: ________ ________

NOTE: It is not necessary to use this form to amend a previously filed application. Should you do so, however, please submit only Section I and those other portions of the form that contain the amended information.

3. Is this application mutually exclusive with a renewal application? ☐ Yes ☐ No

If Yes, state: Call letters | Community of License: City | State

Figure G1



Federal Communications Commission
Washington, D.C. 20554

APPLICATION FOR NEW BROADCAST STATION LICENSE
(Carefully read instructions before filling out Form)
RETURN ONLY FORM TO FCC

Approved by OMB
3060-0029
Expires 9/30/90

For Commission Fee Use Only

FEE NO:

FEE TYPE:

FEE AMT:

ID SEQ:

For Applicant Fee Use Only

Is a fee submitted with this application? ☐ Yes ☐ No

If No, indicate reason therefor (check one box):

☐ Nonfeeable application

Fee Exempt (See 47 C.F.R. Section 1.1112)

☐ Noncommercial educational licensee

☐ Governmental entity

SECTION I – GENERAL DATA

For Commission Use Only

File No.

Legal Name of Applicant

Mailing Address

City | State | Zip Code

Telephone No. (include area code)

1. Facilities authorized by construction permit

This application is for: ☐ Commercial ☐ Noncommercial

☐ AM Directional ☐ AM Non-Directional ☐ FM Directional ☐ FM Non-Directional ☐ TV

Call Letters	Community of License	Construction Permit File No.	Modification of Construction Permit File No(s).	Expiration Date of Last Construction Permit

2. Is the station now operating pursuant to automatic program test authority in accordance with 47 C.F.R. Section 73.1620? ☐ Yes ☐ No

If No, explain.

3. Have all the terms, conditions, and obligations set forth in the above described construction permit been fully met? ☐ Yes ☐ No

If No, state exceptions.

4. Apart from the changes already reported, has any cause or circumstance arisen since the grant of the underlying construction permit which would result in any statement or representation contained in the construction permit application to be now incorrect? ☐ Yes ☐ No

If Yes, explain.

5. Has the permittee filed its Ownership Report (FCC Form 323) or ownership certification in accordance with 47 C.F.R. Section 73.3615(b)? ☐ Yes ☐ No ☐ Does not apply

If No, explain.

Figure G2

Figure G1-G2. The FCC Forms Appropriate for Figure 116's Circuit

APPENDIX H

About Current Feedback

Contrary to some enthusiastic marketing claims, current feedback isn't new. In fact, it is much older than "normal" voltage feedback, which has been so popularized by op amps. The current feedback connection is *at least* 50 years old, and probably much older. William R. Hewlett used it in 1939 to construct his now famous sine wave oscillator.[1] "Cathode feedback" was widely applied in RF and wideband instrument design throughout the 30's, 40's and 50's. It was a favorite form of feedback, if for no other reason than there wasn't any place else left to feed back to!

In the early 1950's G.A. Philbrick Researches introduced the K2-W, the first commercially available packaged operational amplifier. This device, with its high impedance differential inputs, permitted the voltage type feedback so common today. Although low frequency instrumentation types were quick to utilize the increased utility afforded by high impedance feedback nodes, RF and wideband designers hardly noticed. They continued to use cathode feedback, called (what else?) emitter feedback in the new transistor form.

Numerous examples of the continued use of current feedback in RF and wideband instruments are found in designs dating from the 1950's to the present.[2] With ostensibly easier to use voltage type feedback a reality during this period, particularly as monolithic devices became cheaper, why did discrete current feedback continue to be used? The reason for the continued popularity of current techniques was (and is) bandwidth. Current feedback is simply much faster. Additionally, within limits, a current feedback based amplifier's bandwidth does not degrade as closed loop gain is increased. This is a significant advantage over voltage feedback amplifiers, where bandwidth falls as closed loop gain is increased.

Relatively recently, current based designs have become available as general purpose, easy to use monolithic and hybrid devices. This brings high speed capability to a much wider audience, hopefully opening up new applications. So, while the technique is not new, marketing claims notwithstanding, the opportunity is. Although current based designs have poorer DC performance than voltage amplifiers, their bandwidth advantage is undeniable. What's the magic?

Current Feedback Basics

William H. Gross

The distinctions of how current feedback amplifiers differ from voltage feedback amplifiers are not obvious at first, because, from the outside, the differences can be subtle. Both amplifier types use a similar symbol, and can be applied on a first order basis using the same equations. However, their behavior in terms of gain bandwidth tradeoffs and large signal response is another story.

Unlike voltage feedback amplifiers, small signal bandwidth in a current feedback amplifier isn't a straight inverse function of closed loop gain, and large signal response is closer to ideal. Both benefits are because the feedback resistors determine the amount of current driving the amplifier's internal compensation capacitor. In fact, the amplifier's feedback resistor (R_f) from output to inverting input works with internal junction capacitances to set the closed loop bandwidth. Even though the gain set resistor (R_g) from inverting input to ground works with the R_f to set the voltage gain, just as in a voltage feedback op amp, the closed loop bandwidth does not change. The explanation of this is fairly straightforward. The equivalent gain bandwidth product of the CFA is set by the Thevenin equivalent resistance at the inverting input and the internal compensation capacitor. If R_f is held constant and gain changed with R_g, the Thevenin resistance changes by the same amount as the gain. From an overall loop standpoint, this change in feedback attenuation will produce a change in noise gain, and a proportionate reduction of open loop bandwidth (as in a conventional op amp). With current feedback, however, the key point is that changes in Thevenin resistance also produce compensatory changes in open loop bandwidth, unlike a conventional fixed gain bandwidth amplifier. As a result, the net closed loop bandwidth of a current-fed-back amplifier remains the same for various closed loop gains.

---

[1] **Note 1:** See Appendix C, "The Wien Bridge and Mr. Hewlett", in Reference 19. See also References 20 through 24 and 46.

[2] **Note 2:** See the "General Electric Transistor Manual", published by G.E. in 1964. See also operating and service manuals for the Hewlett-Packard 3400A RMS Voltmeter, 1120A FET probe, and the Tektronix P6042 current probe.

Figure H1 shows the LT1223 voltage gain vs frequency for five gain settings driving 100Ω. Shown for comparison is a plot of the fixed 100MHz gain bandwidth limitation that a voltage feedback amplifier would have. It is obvious that for gains greater than one, the LT1223 provides 3-20 times more bandwidth.

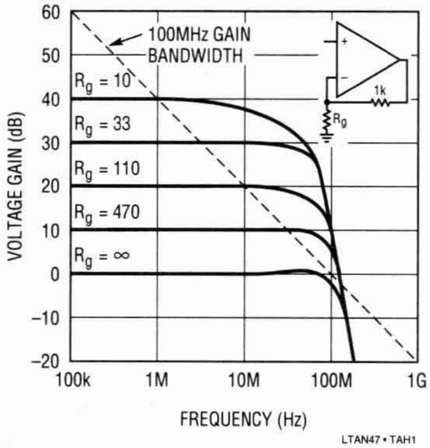


Figure H1. Voltage Gain vs Frequency for Current Feedback Amplifier (Family of Curves) and a Conventional Voltage Amplifier (Straight Line)

Because the feedback resistor determines the compensation of the LT1223, bandwidth and transient response can be optimized for almost every application. When operating on ±15V supplies, R_f should be 1kΩ or more for stability, but on ±5V, the minimum value is 680Ω, because the junction capacitors increase with lower voltage. For either case, larger feedback resistors can also be used, but will slow down the LT1223 (which may be desirable in some applications).

The LT1223 delivers excellent slew rate and bandwidth with better DC performance than previous current feedback amplifiers (CFAs). On ±15V supplies with a 1k feedback resistor, the small signal bandwidth is 100MHz into a 400Ω load and 75MHz into 100Ω. The input will follow slew rates of 250V/µs with the output generating over 500V/µs, and output slew rate is well over 1000V/µs for large input overdrive. Input offset voltage is 3mV (max), and input bias current is 3µA (max). A 10kΩ pot, connected to pins 1 and 5 with wiper to V^+, provides optional offset trimming. This trim shifts inverting input current about ±10µA, effectively producing input voltage offset.

The LT1223 also has shutdown control, available at pin 8. Pulling more than 200µA from pin 8 drops the supply current to less than 3mA, and puts the output into a high impedance state. The easy way to force shutdown is to ground pin 8 using an open collector (drain) logic stage. An internal resistor limits current, allowing direct interfacing with no additional parts. When pin 8 is open, the LT1223 operates normally.

The difference in operating characteristics between op amps and CFAs result in slight differences in common circuit configurations. Figure H2 summarizes some popular circuit types, showing differences between op amps and CFAs. Gain can be set with either R_{IN} or R_f in an op amp, while a CFA's feedback resistor (R_f) is fixed. Op amp bandwidth is controllable with a feedback capacitor; for a CFA, bandwidth must be limited at the input. A feedback capacitor is never used. In an integrator, the 1k resistor must be included in the CFA so its negative input sees the optimal impedance. Finally, (not shown) there is no correlation between bias currents of a CFA's inputs. Because of this, source impedance matching will not improve DC accuracy. Matching input source impedances aids offset performance in op amps that do not have internal bias current cancellation.

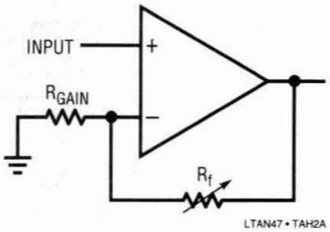
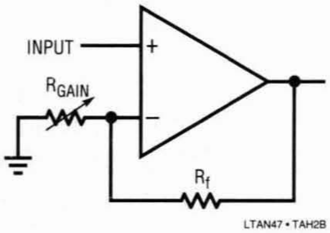
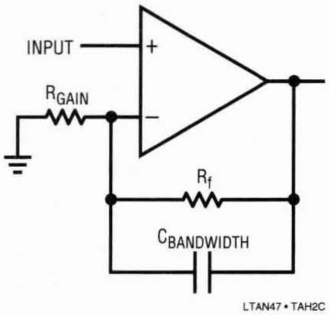
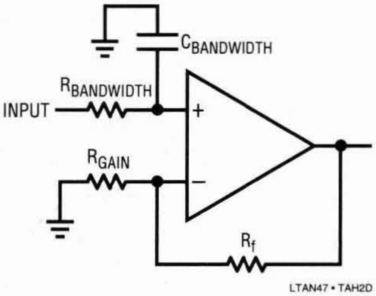
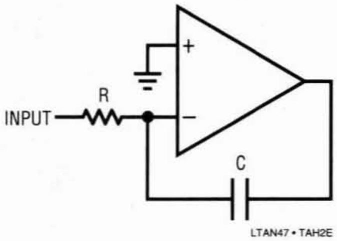
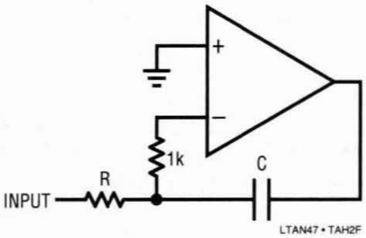
CIRCUIT TYPE	VOLTAGE FEEDBACK OP AMP	CURRENT FEEDBACK AMPLIFIER
SETTING GAIN	 INPUT + – R_{GAIN} R_f LTAN47 • TAH2A	 INPUT + – RGAIN Rf LTAN47 • TAH2B
LIMITING BANDWIDTH	 INPUT + – RGAIN Rf CBANDWIDTH LTAN47 • TAH2C	 CBANDWIDTH RBANDWIDTH INPUT + – RGAIN Rf LTAN47 • TAH2D
INTEGRATOR	 + – R INPUT C LTAN47 • TAH2E	 + – 1k R INPUT C LTAN47 • TAH2F

Figure H2. Some Practical Differences in Applying Current and Voltage Amplifiers

APPENDIX I

High Frequency Amplifier Evaluation Board

LTC demo board 009 (photo, Figure I1, schematic, Figure I2) is designed to simplify the evaluation of high speed operational amplifiers. It includes both an inverting and non-inverting circuit, and extra holes are provided to allow the use of board-mounted BNC or SMA connectors. The two circuits are independent with the exception of shared power supply and ground connections.

Layout is a primary contributor to the performance of any high speed amplifier. Poor layout techniques adversely affect the behavior of a finished circuit. Several important layout techniques, all used in demo board 009, are described below:

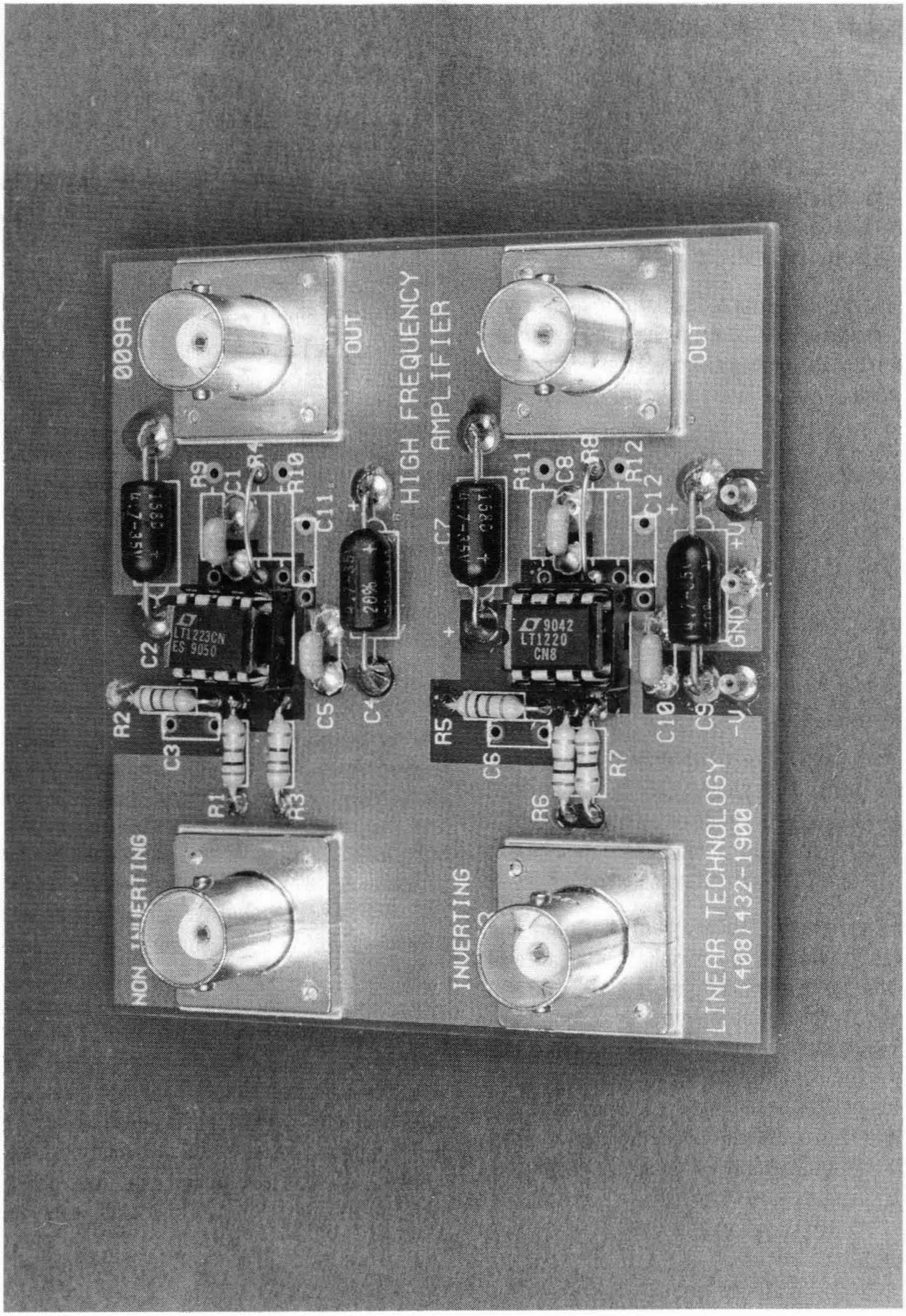
1. Top side ground plane. The primary task of a ground plane is to lower the impedance of ground connections. The inductance between any two points on a uniform sheet of copper is less than the inductance of a thin, straight trace of copper connecting the same two points. The ground plane approximates the characteristics of a copper sheet and lowers the impedance at key points in the circuit, such as the grounds of connectors and supply bypass capacitors.
2. Ground plane voids. Certain components and circuit nodes are very sensitive to stray capacitance. Two good examples are the summing node of the op amp and the feedback resistor. Voids are put in the ground plane in these areas to reduce stray ground capacitance.
3. Input/output matching. The width of the input and output traces is adjusted to a stripline impedance of 50Ω. Note that the terminating resistors (R3 and R7) are connected to the end of the input lines, not at the connector. While stripline techniques aren't absolutely necessary for the demo board, they are important on larger layouts where line lengths are longer. The short lines on the demo board can be terminated in 50Ω, 75Ω, or 93Ω without adversely affecting performance.
4. Separation of input and output grounds. Even though the ground plane exhibits a low impedance, input and output grounds are still separated. For example, the termination resistors (R3 and R7) and the gain-setting resistor (R1) are grounded in the vicinity of the input connector. Supply bypass capacitors (C1, C2, C4, C5, C7, C8, C9 and C10) are returned to ground in the vicinity of the output connectors.

The circuit board is designed to accommodate standard 8-pin miniDIP, single operational amplifiers such as the LT1190 and LT1220 families. Both voltage and current feedback types can be used. Pins 1, 5 and 8 are outfitted with extra holes for use in adjusting DC offsets, compensation, or, in the case of the LT1223 and LT1190/1/2, for shutting down the amplifier.

If a current feedback amplifier such as the LT1223 is being evaluated, omit C3/C6. R4 and R6 are included for impedance matching when driving low impedance lines. If the amplifier is supposed to drive the line directly, or if the load impedance is high, R4 and R8 can be replaced by jumpers. Similarly R10 and R12 can be used to establish a load at the output of the amplifier.

Low profile sockets may be used for the op amps to facilitate changing parts, but performance may be affected above 100MHz.

High speed operational amplifiers work best when their supply pins are bypassed with RF-quality capacitors. C1, C5, C8 and C10 should be 10nF disc ceramic or other capacitors with a self-resonant frequency greater than 10MHz. The polarized capacitors (C2, C4, C7, and C9) should be 1μF to 10μF tantalums. Most 10nF ceramics are self-resonant well above 10MHz and 4.7μF solid tantalums (axial leaded) are self-resonant at 1MHz or below. Lead lengths are critical; the self-resonant frequency of a 4.7μF tantalum drops by a factor of 2 when measured through 2" leads. Although a capacitor may become inductive at high frequencies, it is still an effective bypass component above resonance because the impedance is low.


HIGH FREQUENCY
AMPLIFIER
LINEAR TECHNOLOGY
(408)432-1900
NON INVERTING
INVERTING
OUT
OUT
LT1223CN
LT1220
CN8
+V
GND
-V

LTAN47 • TAI1

Figure I1. The Enticing LTC High Frequency Amplifier Demonstration Board. Sockets are Not Optimal, but Allow Trying Different Amplifiers

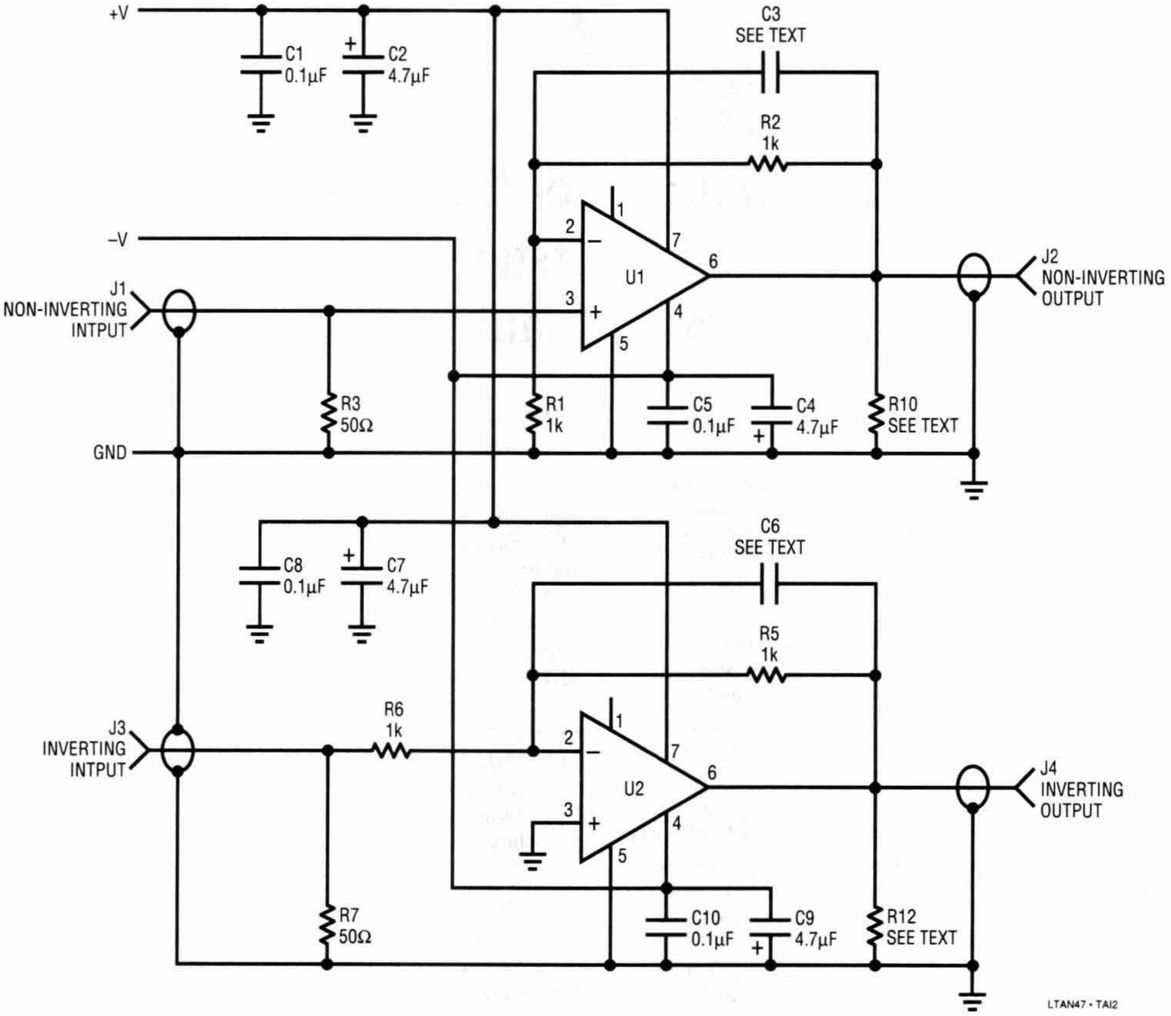

+V
C1
0.1µF
C2
4.7µF
C3
SEE TEXT
R2
1k
–V
J1
NON-INVERTING
INTPUT
U1
J2
NON-INVERTING
OUTPUT
R3
50Ω
R1
1k
C5
0.1µF
C4
4.7µF
R10
SEE TEXT
GND
C8
0.1µF
C7
4.7µF
C6
SEE TEXT
R5
1k
R6
1k
J3
INVERTING
INTPUT
U2
J4
INVERTING
OUTPUT
R7
50Ω
C10
0.1µF
C9
4.7µF
R12
SEE TEXT
LTAN47 • TAI2

Figure I2. High Frequency Amplifier Demonstration Board Schematic

APPENDIX J

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The Contributions of Edsel Murphy to the Understanding of the Behavior of Inanimate Objects

D. L. KLIPSTEIN

Abstract—**Consideration is given to the effects of the contributions of Edsel Murphy to the discipline of electronics engineering. His law is stated in both general and special form. Examples are presented to corroborate the author's thesis that the law is universally applicable.**

I. Introduction

IT HAS LONG BEEN the consideration of the author that the contributions of Edsel Murphy, specifically his general and special laws delineating the behavior of inanimate objects, have not been fully appreciated. It is deemed that this is, in large part, due to the inherent simplicity of the law itself.

It is the intent of the author to show, by references drawn from the literature, that the law of Murphy has produced numerous corollaries. It is hoped that by noting these examples, the reader may obtain a greater appreciation of Edsel Murphy, his law, and its ramifications in engineering and science.

As is well known to those versed in the state-of-the-art, Murphy's Law states that "If anything can go wrong, it will." Or, to state it in more exact mathematical form:

$$1 + 1 \text{ ☞ } 2 \tag{1}$$

where ☞ is the mathematical symbol for hardly ever.

Some authorities have held that Murphy's Law was first expounded by H. Cohen[1] when he stated that "If anything can go wrong, it will — during the demonstration." However, Cohen has made it clear that the broader scope of Murphy's general law obviously takes precedence.

To show the all-pervasive nature of Murphy's work, the author offers a small sample of the application of the law in electronics engineering.

II. General Engineering

II.1. A patent application will be preceded by one week by a similar application made by an independent worker.

II.2. The more innocuous a design change appears, the further its influence will extend.

II.3. All warranty and guarantee clauses become void upon payment of invoice.

II.4. The necessity of making a major design change increases as the fabrication of the system approaches completion.

II.5. Firmness of delivery dates is inversely proportional to the tightness of the schedule.

II.6. Dimensions will always be expressed in the least usable term. Velocity, for example, will be expressed in furlongs per fortnight.[2]

II.7. An important Instruction Manual or Operating Manual will have been discarded by the Receiving Department.

II.8. Suggestions made by the Value Analysis group will increase costs and reduce capabilities.

II.9. Original drawings will be mangled by the copying machine.[3]

III. Mathematics

III.1. In any given miscalculation, the fault will never be placed if more than one person is involved.

III.2. Any error that can creep in, will. It will be in the direction that will do the most damage to the calculation.

III.3. All constants are variables.

III.4. In any given computation, the figure that is most obviously correct will be the source of error.

III.5. A decimal will always be misplaced.

III.6. In a complex calculation, one factor from the numerator will always move into the denominator.

IV. Prototyping and Production

IV.1. Any wire cut to length will be too short.

IV.2. Tolerances will accumulate unidirectionally toward maximum difficulty of assembly.

IV.3. Identical units tested under identical conditions will not be identical in the field.

IV.4. The availability of a component is inversely proportional to the need for that component.

IV.5. If a project requires n components, there will be n-1 units in stock.[4]

IV.6. If a particular resistance is needed, that value will not be available. Further, it cannot be developed with any available series or parallel combination.[5]

IV.7. A dropped tool will land where it can do the most damage. (Also known as the law of selective gravitation.)

IV.8. A device selected at random from a group having 99% reliability, will be a member of the 1% group.

IV.9. When one connects a 3-phase line, the phase

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sequence will be wrong.[6]

IV.10. A motor will rotate in the wrong direction.[7]

IV.11. The probability of a dimension being omitted from a plan or drawing is directly proportional to its importance.

IV.12. Interchangeable parts won't.

IV.13. Probability of failure of a component, assembly, subsystem or system is inversely proportional to ease of repair or replacement.

IV.14. If a protoype functions perfectly, subsequent production units will malfunction.

IV.15. Components that must not and cannot be assembled improperly will be.

IV.16. A dc meter will be used on an overly sensitive range and will be wired in backwards.[8]

IV.17. The most delicate component will drop.[9]

IV.18. Graphic recorders will deposit more ink on humans than on paper.[10]

IV.19. If a circuit cannot fail, it will.[11]

IV.20. A fail-safe circuit will destroy others.[12]

IV.21. An instantaneous power-supply crowbar circuit will operate too late.[13]

IV.22. A transistor protected by a fast-acting fuse will protect the fuse by blowing first.[14]

IV.23. A self-starting oscillator won't.

IV.24. A crystal oscillator will oscillate at the wrong frequency — if it oscillates.

IV.25. A pnp transistor will be an npn.[15]

IV.26. A zero-temperature-coefficient capacitor used in a critical circuit will have a TC of –750 ppm/°C.

IV.27. A failure will not appear till a unit has passed Final Inspection.[16]

IV.28. A purchased component or instrument will meet its specs long enough, and only long enough, to pass Incoming Inspection.[17]

IV.29. If an obviously defective component is replaced in an instrument with an intermittent fault, the fault will reappear after the instrument is returned to service.[18]

IV.30. After the last of 16 mounting screws has been removed from an access cover, it will be discovered that the wrong access cover has been removed.[19]

IV.31. After an access cover has been secured by 16 hold-down screws, it will be discovered that the gasket has been omitted.[20]

IV.32. After an instrument has been fully assembled, extra components will be found on the bench.

IV.33. Hermetic seals will leak.

V. SPECIFYING

V.1. Specified environmental conditions will always be exceeded.

V.2. Any safety factor set as a result of practical experience will be exceeded.

V.3. Manufacturers' spec sheets will be incorrect by a factor of 0.5 or 2.0, depending on which multiplier gives the most optimistic value. For salesmen's claims these factors will be 0.1 or 10.0.

V.4. In an instrument or device characterized by a number of plus-or-minus errors, the total error will be the sum of all errors adding in the same direction.

V.5. In any given price estimate, cost of equipment will exceed estimate by a factor of 3.[21]

V.6. In specifications, Murphy's Law supersedes Ohm's.

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[5] — — — —, *loc cit.*
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[20] — — — —, *loc cit.*
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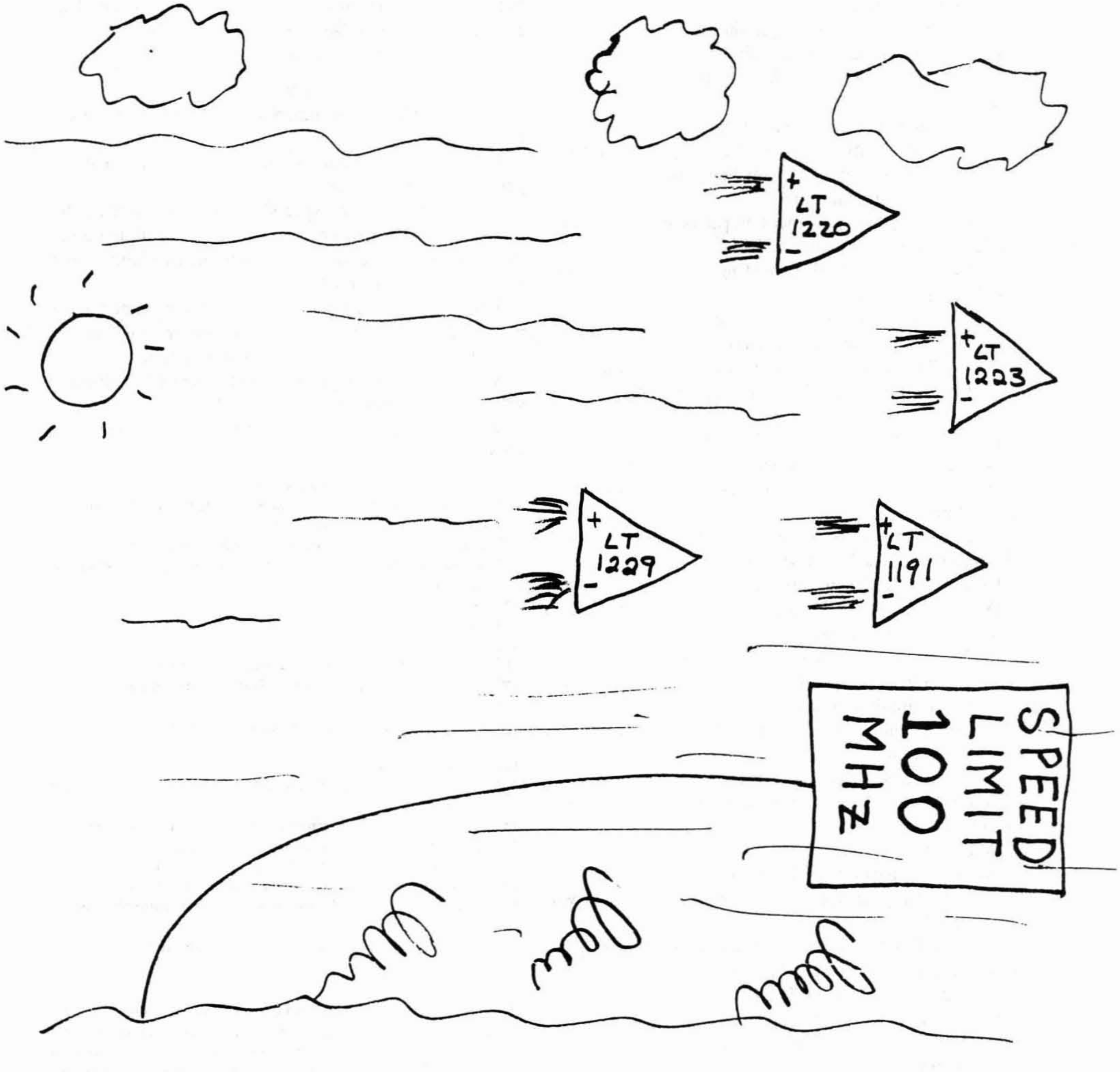
*In some cases where no reference is given, the source material was misplaced during preparation of this paper (another example of Murphy's Law). In accordance with the law, these misplaced documents will turn up on the date of publication of this paper.

The man who developed one of the most profound concepts of the twentieth century is practically unknown to most engineers. He is a victim of his own law. Destined for a secure place in the engineering hall of fame, something went wrong.

His real contribution lay not merely in the discovery of the law but more in its universality and in its impact. The law itself, though inherently simple, has formed a foundation on which future generations will build.


+ LT 1220 -
+ LT 1223 -
+ LT 1229 -
+ LT 1191 -
SPEED LIMIT 100 MHz

(I WISH This App. Note WENT AS FAST AS LTC Amplifiers)

'91

LINEAR TECHNOLOGY

Application Note 48

November 1991

Using the LTC Op Amp Macromodels

Getting the Most from SPICE and the LTC Library

Walt Jung

INTRODUCTION

This application note is an overview discussion of the Linear Technology SPICE macromodel library. It assumes little if any prior knowledge of this software library or its history. However, it does assume familiarity with both the analog simulation program SPICE (or one of its many derivatives), and modern day op amps, including bipolar, JFET, and MOSFET amplifier technologies.

Some Preliminary SPICE Facts of Life

In the past few years, SPICE simulations have really begun to capture a high level of attention on the part of analog circuit designers. Perhaps this is due to more affordable high performance computers, or perhaps the time for simulation is now upon us. In any event, the bottom line is that IC vendors are now making macromodels for op amps available to their customers.

For the analog circuit designer, there can be no better fate for simulations, viewing this situation in terms of which model to use. Designers no longer need worry about whether the third party supplier's model can really cut it. Speaking in terms of the ultimate potential, no one can know an actual part better than the people who designed and produced it, that is the original source IC vendor. The only possible caveat to this scenario is that the vendor supplying an op amp model needs to fully understand not only the real part, *but they must also understand SPICE and modeling issues.* Without both types of understanding firmly in place, the user can end up with a real part that works well and a model which doesn't. For such a case, simulation will be of little value; simulation runs to verify circuit performance won't match the actual part's bench performance.

Fortunately, this type of problem seems to be diminishing. If this were not so, the rapid increase in attention to models would not be taking place. However, all is not necessarily peaceful bliss for analog designs, and yes, we still need to actually build breadboards to check out circuit designs in the lab. The go-go project managers may say "Simulate it, we don't have time to fool with the breadboard and hand-built prototypes." Rarely will this ramrod approach be a truly wise move, now or in the future, except in specialized circumstances.

While it is certainly true that we are in the age of computers, and that they really do aid our tasks in many ways, that is simply not enough for all cases. SPICE (or any simulation tool) can only act upon the information fed into it to analyze a circuit. Model quality issues set aside for the moment, can you honestly say that you have fully sufficient characterization data for every single relevant connection point/load that your circuit will ever see? Do you understand *all* of the parasitic issues it will face? If you can say yes to all of these, then maybe all that you need is just a good op amp model, and SPICE. More likely, there will always be some uncertainties, so breadboarding will remain the only advisable choice for relatively complex circuits, particularly those never built before.

This then leaves a question of model quality and degree of functionality to be answered. Are the presently available models enough? Just how far can they be trusted for the types of simulations that are to be performed? Hopefully, most of these answers will be more apparent by the end of this note, as it contains many different examples. Nevertheless, no IC vendor (or other model supplier) is likely to ever stand up and say, "We guarantee this model when used with simulator ABC, and the simulated performance will be within X% of the actual part connected within a corresponding circuit."

Forget it, SPICE simply doesn't work that way, and likely never will. What SPICE *is* good for is predictive analysis, worst case limit testing, design feasibilities, etc. But even then it will always have limitations; it will never be any better than the information fed to it, and obviously this impacts macromodels as well as all other circuit elements. This may sound at first like a questionable reward, but bear in mind just how you can do a worst case design performance limit for a board with several dozen components. Traditionally, this has been not only difficult, it very often didn't get done at all (except by production line "hot patches"). Logically then, IC manufacturers offering macromodels place caveats and performance limitations on them, which should be understood by the user. These caveats don't make the models at all useless, but they do define the nature and extent of what they can achieve. The following model disclaimer is typical, and is excerpted from the LTC model library:

"This library of macromodels is being supplied to LTC users as an aid to circuit designs. While the models reflect reasonably close similarity to corresponding devices in performance terms, their use is not suggested as a replacement for breadboarding. Simulation should be used as a forerunner or a supplement to traditional lab testing.

Users should very carefully note the following factors regarding these models: Model performance in general will reflect typical baseline specs for a given device, and certain aspects of performance may not be modeled fully. While reasonable care has been taken in their preparation, we cannot be responsible for correct application on any and all computer systems. Model users are hereby notified that these models are supplied as is, with no direct or implied responsibility on the part of LTC for their operation within a customer circuit or system. Further, Linear Technology Corporation reserves the right to change these models without prior notice.

In all cases, the current data sheet information for a given real device is your final design guideline, and is the only actual performance guarantee. For further technical information, refer to individual device data sheets. Your feedback and suggestions on these (and future) models will be appreciated!"...

So, perhaps the first thing to understand about SPICE op amp macromodels is that they invariably come with caveats. Such are the op amp macromodel facts of life.

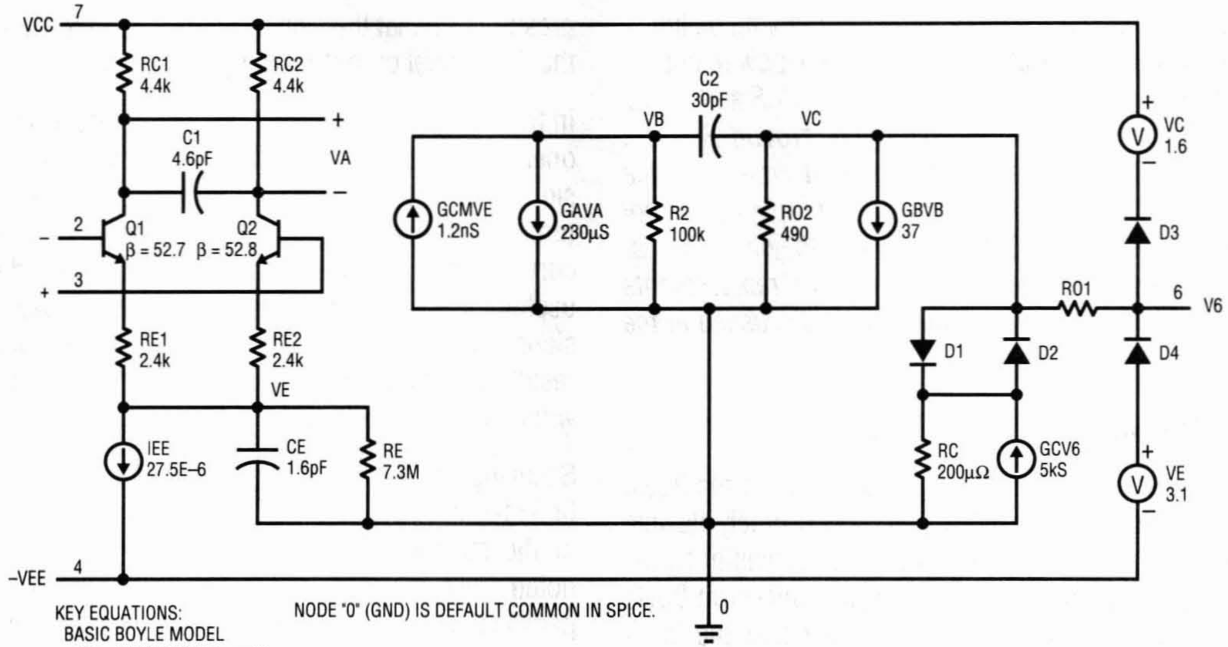
But, like many other things in design engineering, an op amp macromodel can be good or bad, dependent upon what you need to do with it. Indeed, circuit requirements differ, and either DC or AC considerations can drive a given application. At LTC, we feel that the *overall* performance of a macromodel is what can make or break it. Therefore, the op amp modeling has been directed towards getting maximum real world performance in the models, that is performance which in many ways is like the actual op amp device. But, it also means models which do not sacrifice general utility to maximize one single aspect of performance, AC, DC, or whatever.

A Background of SPICE Op Amp Macromodels

Circuit designers generally like to work quickly and efficiently with SPICE simulations, so the macromodel approach is fundamentally very attractive, for good reason. Rather than using a full set of transistors, macromodels use the various controlled sources supported within SPICE, and they also minimize/simplify P-N junctions as much as possible. This approach can increase simulation speed several fold over a full circuit using 30-40 actual transistor models. It can also work well (within its limitations) given a well designed macromodel.

Op amp macromodeling got its start about 15 years ago, in what is now a classic topological approach by Boyle, Cohn, Pederson, and Solomon.[1] The model topology described in this seminal work has now become known generically as the Boyle macromodel. With recent advances in computing hardware, modeling as a linear circuit design aid has taken off in the last few years. This of course has re-focused attention on modeling techniques in general, but the Boyle architecture in particular. Now, armed with better macromodels for their designs, analog circuit architects are able in many cases to move more quickly toward better designs.

Note 1: Boyle, G.R., Cohn, B.M., Pederson, D.O., Solomon, J.E., "Macromodeling of Integrated Circuit Operational Amplifiers," IEEE Journal of Solid-State Circuits, Vol. SC-9, # 6, December 1974.



KEY EQUATIONS:
BASIC BOYLE MODEL
SR = IEE/C2 (FOR β >> 1)
A_{VD} = (GA • R2) (GB • RO2)
GBP = 1/(2 • π • RC1 • C2)
V_{OS} = VT • LN (IS1/IS2)

NODE "0" (GND) IS DEFAULT COMMON IN SPICE.

LTAN48 • TA01

Figure 1. Boyle 741 Op Amp Macromodel

A Short Course on the Boyle Macromodel

While the Boyle model topology has become a default macromodel standard, it also has received criticism for op amp performance aspects it doesn't handle. Unfortunately, not all of this criticism has been well focused, or couched in a meaningful perspective. For example, many critics of the Boyle model often fault it *for what it doesn't do in its original or most basic form*, and simply ignore more recent enhancements (which, ironically, aren't so hard to find). One such case of Boyle based macromodels with many useful enhancements are those produced by the MicroSim Parts[2] program. And, as the following discussions show, the basic Boyle model has been usefully enhanced and expanded in other regards.

The Boyle macromodel is shown in Figure 1, essentially just as it was originally described in the 1974 paper. This example model is for a 741 op amp, which has a bipolar NPN input stage. The model parameters are noted in the figure, and when run, this macromodel duplicates the characteristics of the device quite well. Comparison of the actual parameters for the 741 as modeled can be done by a detailed contrast of the paper's appendix parameters, and those of this figure. Note that the typical op amp pin numbers have been added to tie this model more closely to a real device. As will later be apparent, this nodal convention is used throughout in the LTC amplifiers.

Listing 1 (see listings at end of application note) is a sample macromodel for an 8741 op amp. This model was produced by the LTC macromodel program for NPN op amps, with input data taken from the Boyle paper appendix (Note: there is no *actual* LTC "8741"; this particular model was done as an exercise). Comparison of the first portions of this model with the values of Figure 1 shows good correlation.[3]

Some of the key equations for the basic Boyle macromodel are noted in Figure 1, and they all can be found within the text of the paper itself. The key op amp parameters modeled are gain bandwidth product (GBP), slew rate (SR), phase margin, DC gain (A_{VD}), CMRR, input offset voltage (V_{OS}), input bias current (I_B), input offset current

---

Note 2: MicroSim, vendor of PSpice™, Probe™, and Parts™.
20 Fairbanks, Irvine, CA, 92718, (714) 770-3022.

Note 3: This comparison of the Listing 1 8741 macromodel with the Boyle original is valid only for the code within sections "INPUT" and portions of "INTERMEDIATE." As will be noticed, there are only slight differences here (due to rounding). Because of the different type of voltage/current limiting used in the LTC macromodel, there are major differences in gb, RO2, and those portions following, which show up as new code after "OUTPUT."

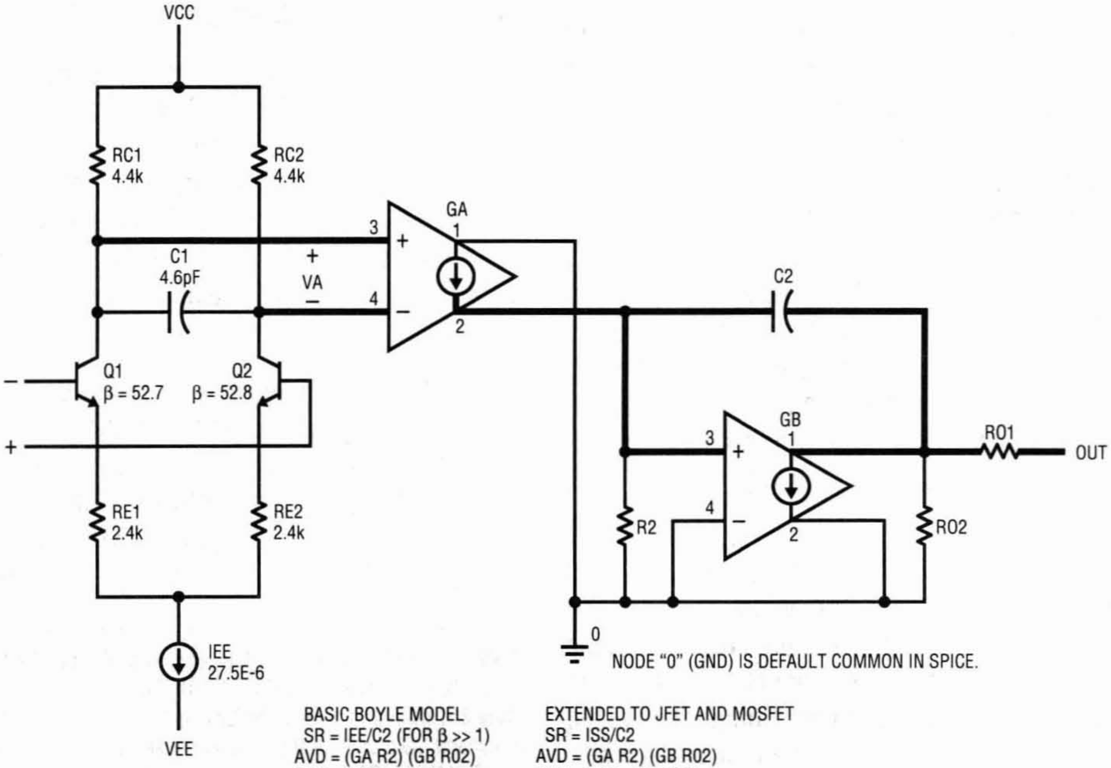
(I_{OS}), output current limiting (I_{SC}), output voltage limits (V_{SAT} ±), output resistance (R_{OUT}), and power supply quiescent current (I_Q). *(Note: The diode/VCCS and diode/voltage source elements of this figure around RO1 are associated with the voltage and current limiting of the original Boyle model. Inasmuch as these networks are not heavily used in the LTC macromodels, they are not discussed in any detail. The new LTC functional replacements for current and voltage limiting will be discussed in the following section).*

Gain-Normalized Input Stage Operation

There is a very important design distinction of the Boyle model topology which allows it to be extremely flexible with regard to adaptations to other input transistor types. Referring to Figure 2, a simplified schematic-form Boyle type model, this feature lies in the fact that the input differential transistor pair Q1/Q2 are, in fact, set by the macromodel design parameters to operate at a differential gain of unity. In the case of the bipolar types shown, the original Boyle design equations establish this by the presumption that the gain from the amplifier's ± inputs to the differential output VA is by definition unity.

In the original model, this unity gain, or gain-normalized operating condition for Q1/Q2 was provided by the inclusion of emitter resistances, RE1/RE2. These resistors force the differential topology to this gain (once given a current for IEE). This gain normalization step adds great usefulness to the model, in simplifying the design expressions for slew rate and gain bandwidth product. As a result, it leads to the substitution of other input devices within this architecture with relative ease.

Speaking more broadly, the input stage gain-normalization step provides specifically for implementing variants of the structure, without major topology changes. As noted, the original paper allowed for NPN or PNP bipolar pairs in the basic design equations. However, if the model topology is viewed more generally, a fundamental fact about it is that *virtually any differentially operated transconductance pair* can be used in the front end. From the signal point VA (the differential outputs of Q1/Q2), the



BASIC BOYLE MODEL
SR = IEE/C2 (FOR β >> 1)
AVD = (GA R2) (GB R02)
GBP = 1/(2 π RC1 C2)
V_{OS} = VT LN (IS1/IS2)

EXTENDED TO JFET AND MOSFET
SR = ISS/C2
AVD = (GA R2) (GB R02)
GBP = 1/(2 π RD1 C2)
V_{OS} = VT01- VT02

LTAN48 • TA02

Figure 2. Input Gain-Normalized Op Amp Macromodel

remaining path of the model can be essentially the same, with the basic design equations holding. For example, in the case of a PFET type amplifier, Q1/Q2 are replaced by P-channel FETs J1/J2; or for PMOS types, they become MOS devices M1/M2, and so on.

With other variations of this type of macromodel topology, provisions are made for transconductance adjustments to the stage, such that the differential pair used operates at unity gain. This can be either through the transconductance parameters of the transistors themselves, or via the associated degeneration resistances (RS1/RS2 for FET devices would correspond to the RE1/RE2 for bipolars). Of course, for whatever type of transconductance devices used, suitable biasing steps must be made.

Note that this general concept allows many variations of the original Boyle model to exist. The basic Boyle model design equations of Figure 1 then can be viewed to dictate the model's performance. This can easily be extended to include the various types mentioned. For example, as shown in the extended equations, the PFET and PMOS expression for SR will follow the same form, with I_{SS} replacing IEE. The corresponding expression for GBP in these amplifiers is similar, with RD1 substituting for RC1.

In creating a different input stage op amp, the different input transistor types are accommodated via the SPICE transistor model parameters of J1/J2, M1/M2, etc. The specific transistor model parameters of these devices then determine the amplifier input V_{OS}, I_B, and I_{OS}.

While this input stage gain normalization step makes the input flexible, it does have a basic trade-off. Because the input transistors are operated at current/gain levels generally unlike those used in the actual op amp, the noise properties are generally uncorrelated (note that a low noise op amp will have a very high voltage gain in the first stage, distinctly unlike this model). As a result of this, the input noise performance of a gain-normalized model will usually not track the real IC accurately. Please note however that this factor is *not* unique to Boyle type models, it is just as true for other models with input stage gain normalization.

THE LTC APPROACH TO SPICE OP AMP MACROMODELS

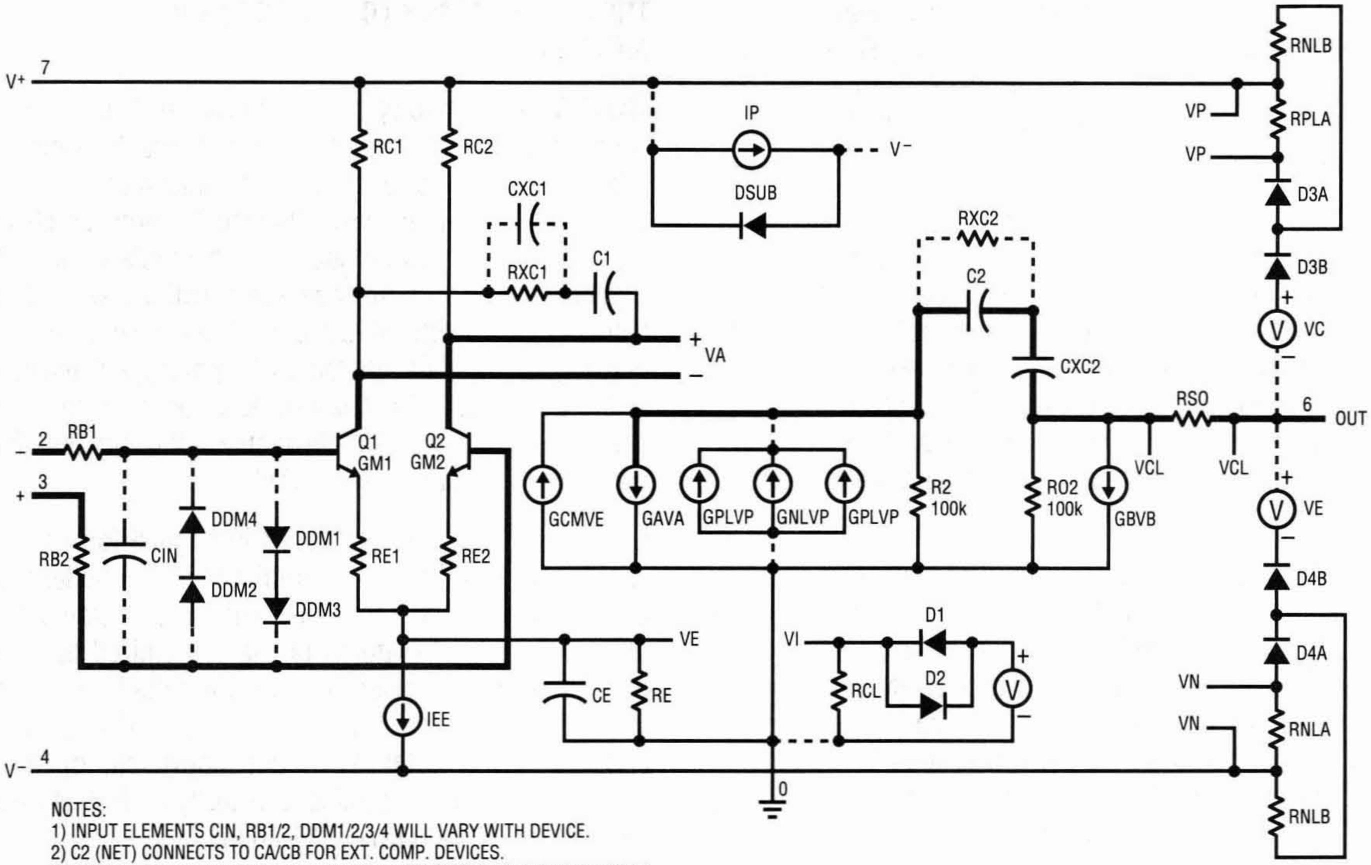
The LTC approach to op amp macromodels has been one aimed towards achieving design improvements within the models, but with a balanced array of simulation enhancements. Attention has been directed towards practical, useful op amp macromodels which emulate the LTC catalog devices in both their specifications as well as general functionality. This approach has been rooted in building on the Boyle macromodel topology, enhancing it where appropriate. To one degree or another, this has been done for each case of the family of the four amplifier macromodel topologies supported.

LTC macromodels are produced in original form by an appropriate member from a family of macromodel programs. These programs implement the algorithms and otherwise support features of the customized op amp macromodels. For a given program, the output consists of a SPICE compatible ASCII file, in the form of an op amp specific macromodel. With this approach, op amp macromodels can be produced virtually as fast as spec sheet definition data can be keyed in.

As noted, the program produces an ASCII macromodel, and Figure 3 is a header portion of a sample macromodel produced by one of the programs. Note that the header includes information in the form of SPICE comment lines (those lines* prefixed), in addition to the actual code of the macromodel itself. In this case the header is for the LT1022 (top line). On line two, the date/time stamp and the general model type are listed. In the next four lines all key specs as used within the model are recorded. This information comprises the macromodel specifications, and the format is generally consistent across the four families of

```
*
* Linear Technology LT1022 op amp model
* Written: 05-10-1990 15:08:03 Type: PFET input, internal comp.
* Typical specs:
* Vos=1.0E–04, Ib=1.0E–11, Ios=2.0E–12, GBP=8.0E+06Hz, Phase mar.= 45 deg,
* SR (low)=2.5E+01V/us, SR (high)=5.0E+01V/us, Av=112.0dB, CMRR= 92.0dB,
* Vsat(+)=1.8V, Vsat(–)=1.8V, Isc=+/–30mA, Rout= 50ohms, Iq= 5mA.
* (input cm clamp *optional*)
*
* Connections: + – V+V–0                                           LTAN48 • TA20
```

Figure 3. Header Portion Sample


V+
7
RC1
RC2
CXC1
RXC1
C1
IP
V−
DSUB
+
VA
−
RXC2
C2
CXC2
RNLB
VP
RPLA
VP
D3A
D3B
+
V
VC
−
RSO
6
OUT
VCL
VCL
2
RB1
−
3
+
Q1
GM1
Q2
GM2
RB2
CIN
DDM4
DDM2
DDM1
DDM3
RE1
RE2
GCMVE
GAVA
GPLVP
GNLVP
GPLVP
R2
100k
RO2
100k
GBVB
+
V
VE
−
D4B
D1
VE
VI
D2
RCL
+
V
−
D4A
VN
VN
RNLA
CE
RE
IEE
V−
4
0
RNLB

NOTES:
1) INPUT ELEMENTS CIN, RB1/2, DDM1/2/3/4 WILL VARY WITH DEVICE.
2) C2 (NET) CONNECTS TO CA/CB FOR EXT. COMP. DEVICES.
3) COMPENSATION ELEMENTS C1 (NET); C2 (NET) SHOWN IN EXTENDED FORM.
4) OUTPUT LIMITING WILL VARY WITH DEVICE.
5) DOTTED CIRCUITRY INDICATES ENHANCEMENTS.

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Figure 4A. Bipolar NPN Input Op Amp Macromodel (Simple)

macromodel types. An optional comment line completes the main part of the header. The macromodel header conveniently documents actual working parameters of the model.

Obviously, the programmed approach is an efficient method for generating new or revised macromodels for release to the public. It also has the important additional feature that it allows LTC application engineers to quickly respond to field requests for custom macromodel values for any parameter modeled.

THE LTC MACROMODEL FAMILY

As previously noted, the LTC macromodel families are comprised of four types of models. There are models for NPN and PNP bipolar input devices, for P-channel JFET input devices, and for PMOS FET input devices. While there are similarities across these four macromodel types, there are also unique distinctions within each. The following sections detail each of these macromodel types, illustrating the common overall features as well as those unique to each type of device.

The LTC Bipolar NPN Input Macromodels

Listing 2 (see listing at end of application note) is a macromodel of the LT1007 NPN bipolar op amp, which generally corresponds directly to the complete NPN macromodel schematic of Figure 4.[4] For clarity, the schematic is shown in two forms; the "simple" form in Figure 4A uses symbolic connections, while the "detailed" form in Figure 4B follows the actual listing.

This schematic appears busy, because of the fact that it shows all possible options of this NPN topology. While all

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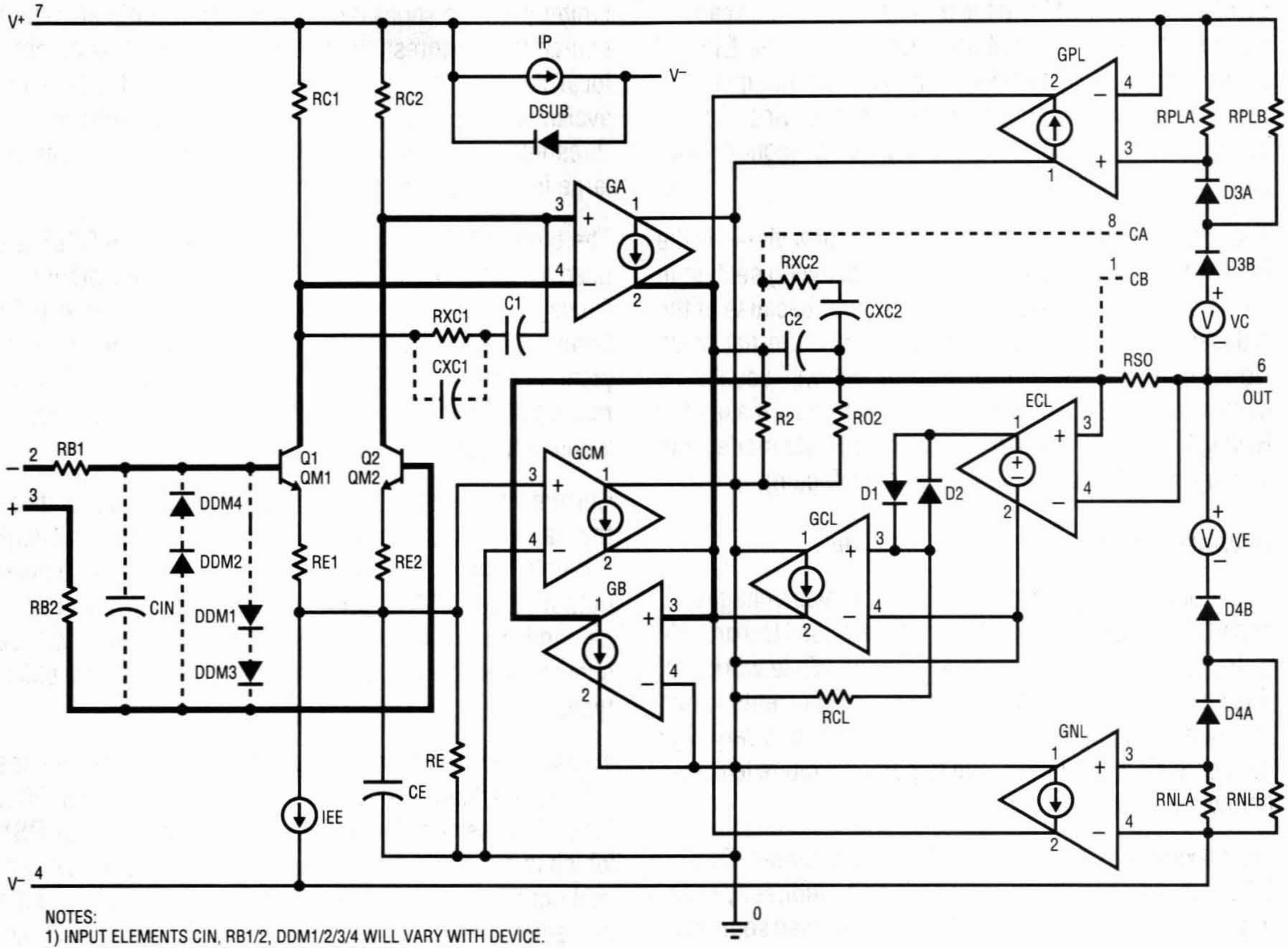
[4] **Note 4:** This generic schematic has no values for this NPN case, nor will those for the other amplifiers. Instead, actual values for the device under discussion are noted in the model listing.


V+ 7
IP
V–
DSUB
RC1
RC2
GA
GPL
RPLA
RPLB
D3A
D3B
VC
8 CA
1 CB
RXC2
CXC2
C2
RXC1
C1
CXC1
RSO
6 OUT
ECL
R2
RO2
GCM
Q1 QM1
Q2 QM2
2 RB1
–
+ 3
DDM4
DDM2
DDM1
DDM3
RB2
CIN
RE1
RE2
D1
D2
GCL
VE
GB
D4B
D4A
RCL
GNL
RE
CE
IEE
RNLA
RNLB
V– 4
0

NOTES:
1) INPUT ELEMENTS CIN, RB1/2, DDM1/2/3/4 WILL VARY WITH DEVICE.
2) C2 (NET) CONNECTS TO CA/CB FOR EXT. COMP. DEVICES.
3) COMPENSATION ELEMENTS C1 (NET); C2 (NET) SHOWN IN EXTENDED FORM.
4) OUTPUT LIMITING WILL VARY WITH DEVICE.
5) DOTTED CIRCUITRY INDICATES ENHANCEMENTS.

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Figure 4B. Bipolar NPN Input Op Amp Macromodel (Detailed)

of the possible options need not be present within a given device, most of them are in fact used in the case of the LT1007. With regard to the schematic as shown, the many device specific conditional details which this NPN macromodel can handle will be discussed in this context.

At the very front end of the model, there is optional use of differential input clamp diodes, with or without series resistance, etc., and similar comments apply to CIN. These model enhancements are employed specifically to closely mimic device characteristics. For example, with the (real) LT1007 and OP-27 type of device shown, a pair of two-diode differential clamps are used, DDM1-DDM4, but without a series resistance (RB1 = RB2 = 0). These options (and others) are shown dotted in Figure 4, to suggest the multiple possibilities, and will vary from one device type to another. Other DC enhancements used are a power consumption current source IP, to mimic DC current drain, and a reverse substrate diode, DSUB (which also can be given a breakdown voltage to simulate maximum supply voltage). Overall, the general intent is to make the macromodels behave more as their real IC counterparts, in these and other functional details.

Throughout this macromodel the main DC signal flow path is shown by the heavy lines, for clarity. Controlled sources GA and GB function as they do in Figure 1, as do passive components R2, RO2, C2, and C1. As is noted, both C1 and

C2 can be expanded from the original Boyle single capacitor, to more complex optional network(s). The LT1007 uses both of these networks, to simulate the multiple pole-zero roll-off characteristic of the actual device. This is covered in more detail in the following section, with performance examples.

The output stage of this model is entirely new vis-a-vis the Boyle model, and is discussed in the following section in terms of the new current/voltage limiters. Because of the reduced 1Ω value used for RSO (or RS), the net small signal output resistance of this model will usually be dominated by the value for RO2. This in turn makes the RO2 value higher, compared to a basic Boyle model, and it also makes GB larger (for the same DC gain).

Improved Voltage and Current Limiting

In the original Boyle model of Figure 1, bias voltages VE and VC along with diodes D3 and D4 were used to a provide brute-force type output voltage limiting. While workable, this scheme produces large internal limit currents within the model. It also can give rise to gain errors in very high gain precision amplifiers, due to parasitic diode leakages below the limiter threshold.

For maximum output current simulation, diodes D1 and D2 of Figure 1 provide current limiting by indirectly sensing the voltage drop across RO1 (the controlled source GC produces a replica of the output voltage across RC, which effectively places D1/D2 in parallel with RO1). When D1 or D2 conduct to start limiting, this also produces very large currents in limit, as well as some gain degradation below threshold.

In many macromodels, LTC has implemented new forms of voltage and current limiting. These schemes use buffered biased diodes, which allow both full amplifier gain below the limit thresholds, as well as accurate limit thresholds for output voltage and current. They are described now, and are used not only within many of the NPN macromodels, but throughout the family of models.

Voltage limiting in the new model of Figure 4B can be described for either the negative or positive swing, as they are similar. The positive swing limiter, which is composed of D3A, D3B, VC, RPLA, RPLB and GPL, will be described. This setup would appear at first as a modified brute-force limiter with two series diodes and a similar offset voltage source for the threshold. It is not however; it is in fact a local closed loop system, which depletes the total current available from source GA when the output voltage limit threshold is reached. This allows clean limiting, with no large internal currents.

The buffered biased diode D3A and resistance RPLB are used to control the leakage of D3B, which would otherwise cause gain errors for an amplifier of the LT1007/OP-27 family. This voltage limit technique was found to be justified for most op amps with DC gains of 120dB or more. With it active, the LT1007's 150dB gain is reached within a fraction of a dB.

Current limiting in this model is symmetrical, that is it has the same current limit level for both source and sink currents. This is typical of amplifiers which use bipolar output stages. CMOS output stages are often asymmetrical, and a modified form of this current limiter will be shown under the discussion of the PMOS input amplifier types.

To minimize loading effects of the current limiter, it uses a dedicated floating differential input buffer amplifier, ECL. This VCVS senses the voltage drop across RSO (or RS), which is directly proportional to output current. The current limit threshold is defined by the gain of ECL, and the characteristics of D1, D2, RCL, and GCL. In this instance, the local loop is closed when the amplified output of ECL drives RCL, through either D1 or D2. As was true in the case of the voltage limiter, when the limit threshold is reached the controlled source (in this case GCL) depletes all available current from GA. Again, this allows clean current limiting, with no large internal currents being produced.

Because of the buffering by ECL, this type of current limiter has very low errors when below its threshold. Not only are the errors low with regard to gain degradation, but the current limit is very accurate.

There is also a much more subtle advantage common to these two limiters, and that is the fact that they are achieved via a parallel feedback path. As such, they will by definition be transparent below threshold, a point already made above. However, a useful side advantage of this is that this macromodel can get along quite well in truth *without* either limiter (for special cases). In fact, they can be disabled for signal purposes very simply, by commenting out the controlled source driving GA, be it either GPL, GNL, or GCL. This can come in handy, if it should ever be necessary to troubleshoot a circuit and/or model for errors.

Caution!

Those who may be tempted to try this should of course know what they are about! Do bear in mind that a macromodel without any limiters is capable of very high voltages and/or currents! Perhaps a more significant bonus of this limiter design scheme is that special "turbo" forms of a given model can be saved, such as an LT1007 model sans limiters. This will greatly speed up analyses, *as long as the external circuit provides for a proper DC loop closure.*

Macromodel Embedded Models

At the bottom of each macromodel listing is a section titled MODELS, which does in fact define those transistor, diode, or any other models used local to the macromodel. In the case of the NPN LT1007 op amp, the NPN models for Q1/Q2 are, as noted, different in terms of IS and BF (current gain), for the following reasons.

V_{OS}, the input offset voltage of the amplifier input pair, is modeled by using two slightly different NPN transistor models, QM1 and QM2. The ratio of their two saturation currents will produce an offset voltage, V_{OS}, which is:

$$V_{OS} = kT/q * \ln(IS1/IS2)$$

With the ratios as shown in Listing 2, this produces the typical 20μV offset of the LT1007C.

Bias and offset currents are modeled by using a different BF for the two input pair halves, as:

$$BF1 = IC1/(I_B + (I_{OS}/2)) \text{ and } BF2 = IC2/(I_B - (I_{OS}/2))$$

The BF values shown for QM1 and QM2 are those which correspond to currents of I_B = 15nA and I_{OS} = 12nA (again for the LT1007C). The gains listed appear high, however this is a by-product of the fact that the actual LT1007 device uses bias current compensation, and the model accounts for this simply with a higher BF.

The remaining models used in the LT1007 are diodes used in various locations, with IS scaled as to the specific use.

Phase/Frequency Response Extensions

One performance area where op amp modeling has recently received strong attention is in regard to frequency response. The original Boyle model of Figure 1 has a dominant pole set by C2 and a secondary pole set by C1. Many op amps now popular have a much more complex phase/frequency response. As a result, using a basic Boyle model AC topology to simulate their transient response can be inaccurate for some applications.

Solutions to modeling additional poles and zeros can range from simple to complex, depending upon what overall trade-off the model designer chooses. For example, a number of sequential pole/zero stages can be added to a model for very fine emulation of small signal transients. In practice, this approach needs to be weighed carefully on an overall basis.

It is not under question here that it is possible to greatly improve upon a simple Boyle type models' phase/frequency response. However, what the macromodel user needs to know is not just how the AC response is improved, but also what is the price to be paid for it. The end results may or may not be worth the possible drawbacks, specifically potential penalties in terms of additional memory required, longer simulation times, and possible convergence issues. Of course these considerations are basic, and are applicable to any model, LTC types included. Nevertheless, it should be noted that these types of problems exaggerate very quickly with multiple amplifier simulations (such as in active filters). It is entirely possible to create more complex models which will not even run in larger multi-amp circuits, when used in standard PC environments with modest memory (~500K).

Alternately, an intermediate approach to modeling some additional poles and zeros can be taken, simply by extending the above mentioned two compensation caps of the basic Boyle model with additional network elements. It is

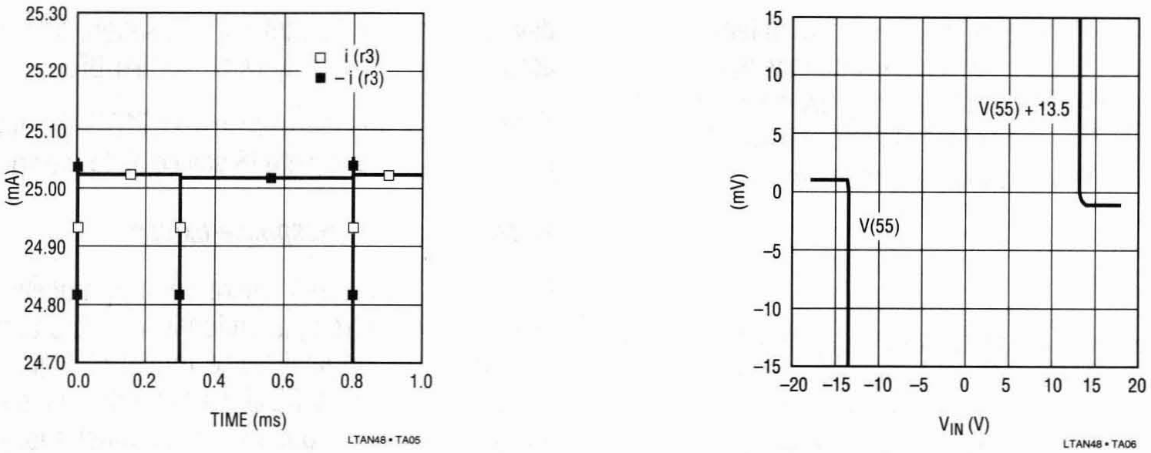

Figure 5A. LT1007 Test F6: I_{SC} (Open Loop, $V_S = \pm 15V$)

Figure 5B. LT1007 Test F7: V_{SAT} ($V_S = \pm 15V$)

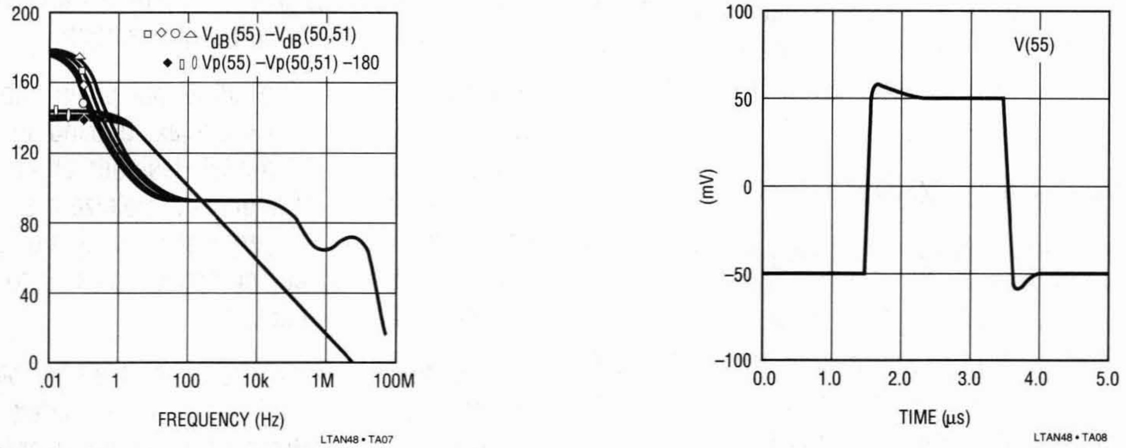

Figure 5C. LT1007 Test F8: Gain/Phase

Figure 5D. LT1007 Test F5: Transient Response

Figure 5. Composite Performance Points

this approach that LTC has used in Figure 4. For C1, RXC1/CXC1 can be added as one extension, while for C2, RXC2/CXC2 can be added. Speaking generally, these are part-specific options, with defaults (i.e., no extensions used) of only C1 and C2. Of course for the LT1007 under discussion a full set is used, as noted by Listing 2.

In contrast to arbitrary additional pole/zero stages, this method can be viewed as relatively limited, which in truth it is. However, it has the advantage of minimal added complexity, as no active stages are added to the model. It also has the fundamental virtue of working well within the overall Boyle topology, since it is an extension of it. Together, these controls allow more complex frequency responses to be simulated without additional active stages, with a net result of minimal simulation overhead increases. NPN model examples which use it are the LT1007/LT1037 families, the LT1028 and LT1115, and the OP-27/OP-37 families, but it is an option available with all device families.

NPN Macromodel Performance

At this point, some sample macromodel performance will be shown to illustrate key points. For these and the following SPICE displays, the macromodels used were taken directly from the current released LTC diskette. For the purposes of this application note, the models were edited into the form of the listings as shown herein (by editing out only the header and copyright notice sections for brevity). These files were then used in the various simulations. Unless specified otherwise, the test circuits use ±15V power supplies, and the op amp model tested has a (+) input node of (50), a (–) input node of (51), an *output of (55), and the signal source is applied to node (2). Unless otherwise specified, no SPICE option default changes were made in the CIR files used for the tests. A 16MHz IBM PC compatible computer was used under DOS 4.01, along with MicroSim's PSpice version 4.03 (DOS version). A ramdisk was used as the work disk in all simulations.*

The picture series of Figure 5 in composite form illustrates various performance points of the LT1007 macromodel.

In terms of the new limiting schemes employed, they are shown by Figure 5, in tests LT1007 F6 and F7. For display of short circuit current, test F6 operates the amplifier as a comparator (open loop) on ±15V supplies, with the output driving a low value resistor (10Ω). The display is a dual trace of the load current I(R3) and its mirror –I(R3). This allows both the ± current limits to be shown here, on an expanded ±1% scale. As can be noted, both the limits are well within 1% of the design current limit of 25mA.

For display of output voltage saturation, the amplifier is connected in a unity gain inverter on ±15V supplies, and driven with a –18V to +18V ramp. This overdrives the amplifier at input/output of more than ±13.5V, so the extremes of the input sweep can be used to evaluate output saturation. Both extremes of display are offset by the nominal limiting voltage of ±13.5V, so the error can be shown expanded around zero, with a range of ±1%. Both limits are well less than 1% in terms of error.

Gain and phase response of this particular model is interesting, as it clearly shows the effects of the C1/RXC1/CXC1 and C2/RXC2/CXC2 extensions to frequency response. Shown in Figure 5, test F8, is a composite plot of inverting mode gain/phase operating with ±15V supplies. The load resistance is varied as a parameter, in steps of 100k, 10k, 2k, and 1k. As shown, the gain varies slightly around the nominal 146dB for the various loads, as would be expected for a 70Ω output resistance. The phase response shows a multiple pole/zero characteristic just before unity gain crossover point, as does the real LT1007. While the macromodel display is not as dramatic in terms of phase change as the data sheet, it is still effective for its purpose.

Figure 5, test F5 is a small signal transient test with the LT1007 connected as a follower, emulating a corresponding data sheet photo. The test is a deceptively simple one, as most would think a voltage follower is a fairly straightforward circuit. Actually, it is a real stress test for an op amp macromodel, in terms of potential problems with convergence, memory usage, required simulation time, and so on. This particular simulation runs without any mishap whatsoever, in about 20s on a 16MHz 386 PC clone, using PSpice 4.03, with no tweaking of SPICE defaults. It also runs with no apparent problems, as one of the LTC demo simulations distributed on the SPICE macromodel diskette (using a demo PSpice version 3.06).[5]

These performance tests summarize those aspects of the LT1007 NPN macromodel previously discussed as new design features. It should be kept in mind that many of them can also appear in other models as well, but they will not necessarily be repeated with subsequent examples.

The LTC Bipolar PNP Input Macromodels

With bipolar PNP input stage op amps, a distinct application and functional difference is that they often are designed for single supply operation, often with supplies of 5V or less. In addition, they may also be designed for micropower applications, with current drains of 100μA per amplifier, or even less. LTC has a large number of such amplifiers, with the macromodels supporting them using either of two PNP model topologies.

The LTC PNP macromodels are, in some senses, similar to those using the NPN model topology. While it is true that there are similarities, since both are based on a Boyle model, there are also many practical differences. Speaking of those beyond the obvious polarity differences, the unique distinctions are largely due to functional characteristics of the various amplifiers modeled. And, they are in turn brought about by the single supply and/or micropower operational features previously mentioned. These differences are the thrust of the LTC modeling enhancements.

The LT1013 Family of Macromodels

In terms of historical accuracy, the family of LTC SPICE macromodels for op amps had its beginnings in 1988, with the release of macromodels for the PNP input op amps LT1013 and LT1014.[6] These models actually had their roots in the MicroSim Parts program, and Listing 3, the macromodel for the LT1013/LT1014, is the version available today. Close akin are derivative models for the LT1013A and the LT1013D. Also related to this model are those of the LT1006 family, including the LT1006, the LT1006A, and the LT1006S8.

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[5] **Note 5:** The "DEMO1007.CIR" file on the LTC SPICE diskette invites users to try this "simple" transient test with other models, to compare relative performance. It can be revealing for such a seemingly innocent test.

The enhancements that these models offer over the original Parts version are three-fold:

- One is the input common mode clamping circuitry (DCM1/DCM2 and VCMC);
- Two is the use of different models for input transistors Q1/Q2 (which allows input bias and offset currents, as well as offset voltage to be simulated);
- Three is the use of a controlled output saturation characteristic when operating near the negative supply rail.

Further discussion and performance examples of this specific model type are found in LTC Design Note 13.

The LT1078/LT1178 Families of Macromodels

More recent examples of LTC bipolar PNP input amplifiers are the two micropower families, the 45μA quiescent current/amplifier LT1078, LT1079, LT1077; and the lower power (15μA quiescent) LT1178 and LT1179. Figure 6 is a dual schematic of the macromodel topology used for these types of PNP op amps. It simulates all those features previously noted, and is discussed below. For the purpose of minimum repetition, only features which differ from models previously discussed are addressed here. Figure 6A is the simple version, while Figure 6B shows all detail, like the actual macromodel listing.

LTC single supply op amps have had a distinction of input phase reversal protection since the introduction of the LT1013/LT1014. This also includes more recent devices such as the LT1078 and LT1178 families. For simulation of this in the macromodel, diodes DCM1 and DCM2 provide

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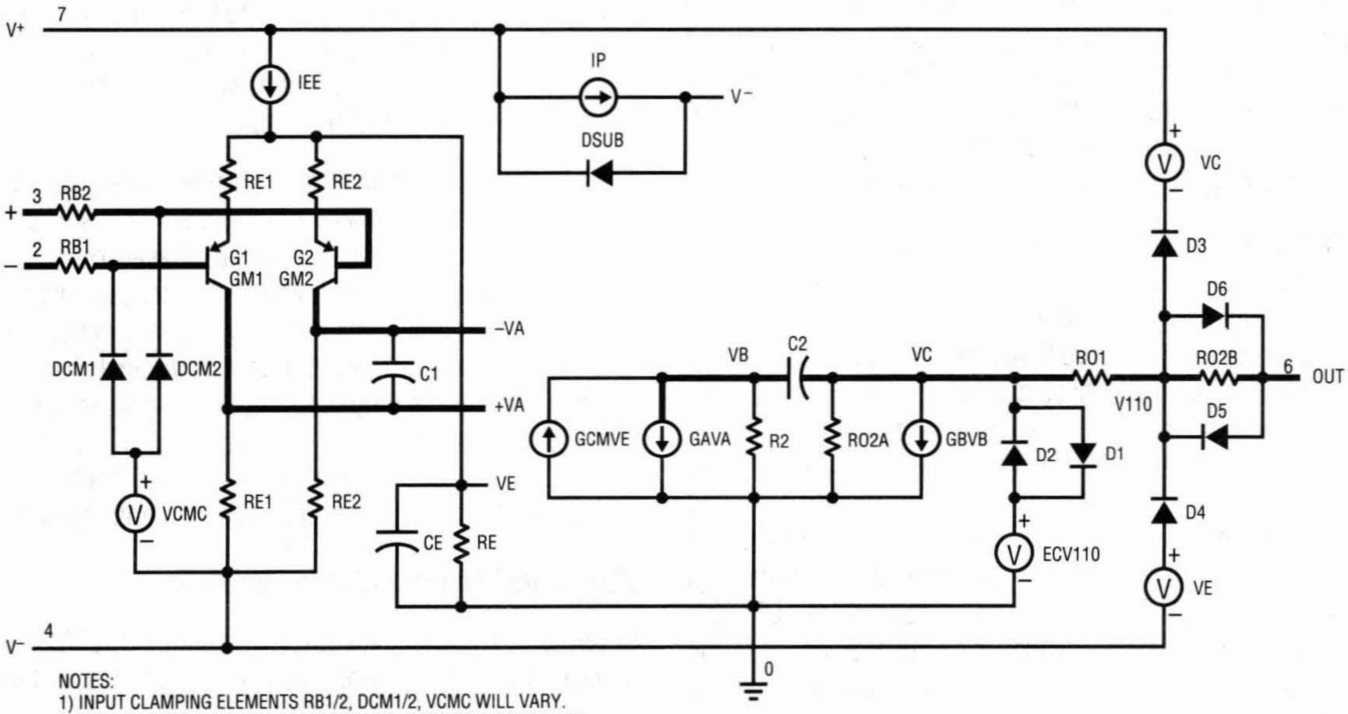
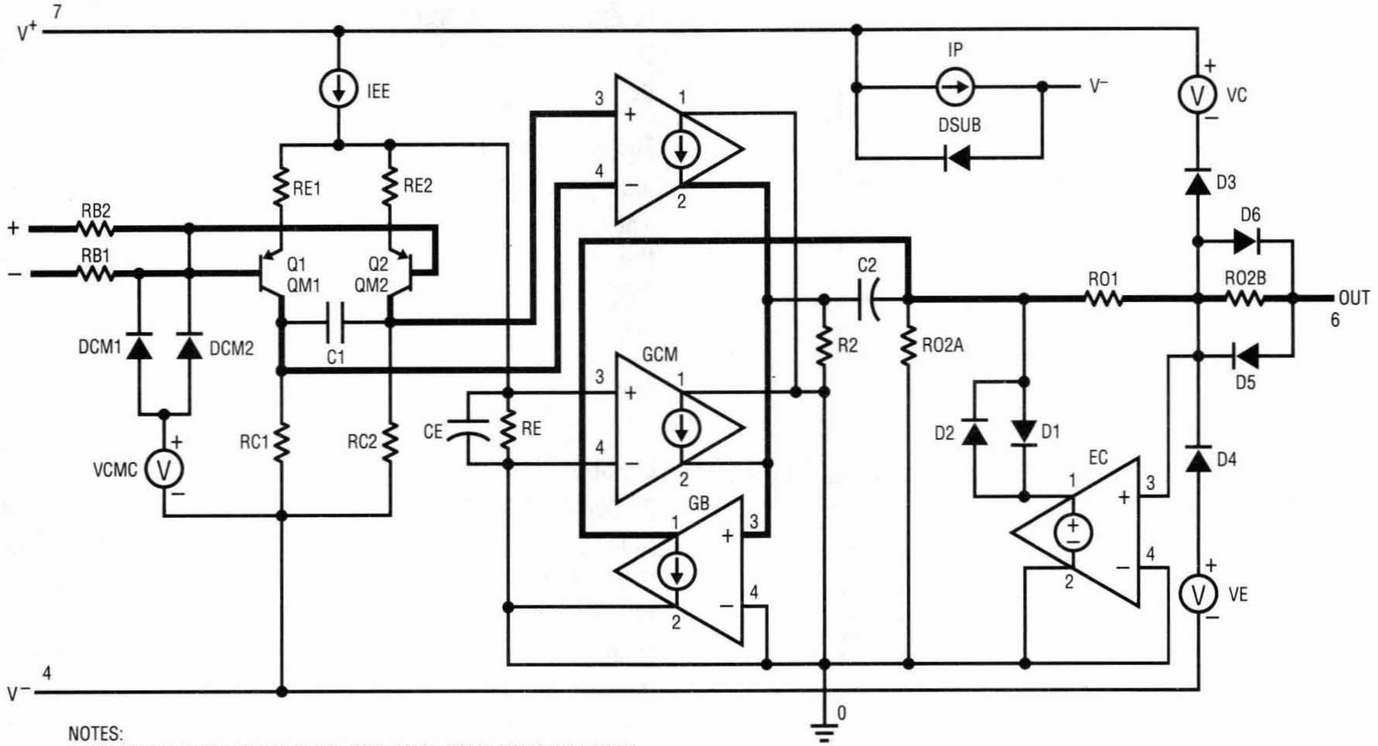
[6] Jung, W. G., "An LT1013 Op Amp Macromodel," Linear Technology Design Note # 13, July, 1988.



NOTES:
1) INPUT CLAMPING ELEMENTS RB1/2, DCM1/2, VCMC WILL VARY.
2) MICROPOWER DEVICES HAVE ADDITIONAL NETWORK, RO2B/D5/D6.
3) COMPENSATION ELEMENTS C1/C2 CAN BE EXTENDED.

Figure 6A. Bipolar PNP Input Op Amp Macromodel (Simple)



NOTES:
1. INPUT CLAMPING ELEMENTS RB1, RB2, DCM1, DCM2, VCMC WILL VARY
2. MICROPOWER DEVICES HAVE ADDITONAL NETWORK, RO2B, ROD5, ROD6.
3. COMPENSATION ELEMENTS C1 AND C2 CAN BE EXTENTED.

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Figure 6B. Bipolar PNP Input Op Amp Macromodel (Detailed)

a negative range input common clamp, for voltages applied to the Q1-Q2 inputs. With the two diodes referenced to a slightly positive common mode clamp voltage, VCMC, they are reverse biased for normal CM voltages. Note that the perspective here is with regard to the negative supply rail, which is also the negative CM limit for single-supply use.

In customizing a macromodel, the inclusion or exclusion of the clamp diodes is an option, as is the RB1/RB2 current limit resistor value, and VCMC. For these single supply devices, VCMC is typically 0.4V, which allows linear common mode response a few hundred mV below ground, just like the actual devices. Without this network, an LT1078 macromodel will (mis)behave just like typical 324/358 amplifiers, with input stage saturation when the inputs are taken below GND. This will be evident by an uncontrolled sign reversal at the output, or hard positive rail saturation.

A key feature added to this model specifically for micropower devices is the extra output network, RO2B and D5/D6. For ordinary dual supply applications, or even single supply uses where close simulation of output voltage saturation is not highly critical, this network isn't needed. However, for single supply op amps such as the LTC PNP input devices which feature active pulldown and linear negative swing operation, simulation to within a few mV of the negative rail is entirely possible. To properly simulate this, a model which displays characteristics similar to the real device when sinking current is needed, which is the function of this network.

LT1078 Macromodel Performance

The LT1078 is a device which illustrates all of the previously mentioned performance points. Its model, shown in Listing 4, can be compared to the schematic of Figure 6 for actual values. The composite pictures of Figure 7 illustrate various performance points.

In terms of CM protection, the model input diode clamp works effectively, as shown by Figure 7, test F3, an overdriven input, +5V single rail follower. Here, the DC input V(2) is swept from –5V to 6V. The displayed output

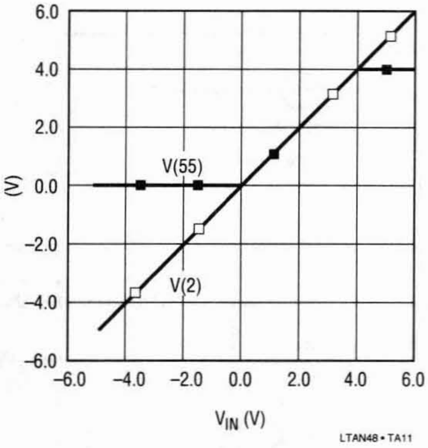


Figure 7A. LT1078 Test F3: +5V Supply, Overdriven Follower

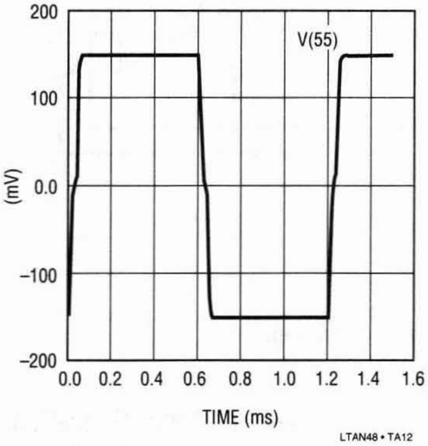


Figure 7B. LT1078 Test F6: I_{SC} (Open Loop, $V_S = \pm15V$)

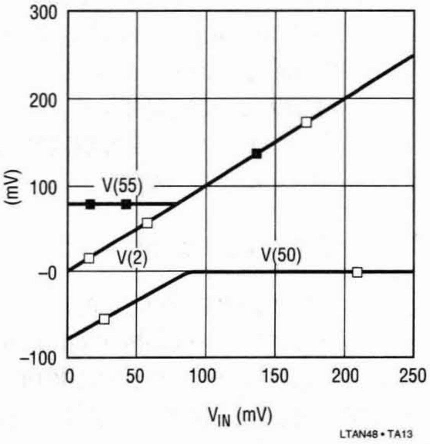


Figure 7C. LT1078 Test F7: Negative Saturation Characteristics

Figure 7. Composite Performance Points

is V(55), and as noted, it is clamped at 0V/4V limits, and there is no phase reversal when the input is taken well below GND (maximum input sink current is 5V/100k).

Figure 7, test F6 shows output voltage V(55) into a 10Ω load, as a test of output current limit. The ±limit levels are 150mV, which corresponds to ±15mA, as is specified for the model. This display also shows the effects of the R02B/D5/D6 Class B output stage used in the model, as is evident by the multiple slope rise/fall.

For a single supply micropower op amp, one of the more difficult aspects of model performance lies in simulating the supply rail saturation, while retaining the micropower performance and a relatively high maximum current output. For the LT1078 typical supply current is only 45μA, and the output resistance is a few kΩ. Yet, the device can also deliver ±15mA (just demonstrated). For the macromodel, the output Class B network allows concurrent micropower small signal characteristics, as well as this relatively high maximum current. The importance of the small signal characteristics come to play for single supply applications, where the output stage is called upon to sink current at output voltages near GND (or the V– rail).

The finer details of the output current sinking near the negative rail are shown in Figure 7, test F7. This test is for a voltage follower, with a DC input V(2) swept from 0V to 5V. The output stage of the model is required to sink 100μA, when the output voltage V(55) is close to GND. As can be noted, the model is linear with voltages above 100mV. For lower voltages, it saturates at about 80mV while sinking 100μA, as does the real LT1078.

The LTC P-Channel JFET (PFET) Macromodels

Historically speaking, the use of both junction and MOSFET transistor types within a Boyle type macromodel topology was described by Krajewska and Holmes, in an early enhancement to the Boyle model.[7] The Krajewska topology is a modified Boyle type model with either type of FET replacing the bipolars of the original model. This enhancement took advantage of the gain-normalization referred to previously.

Note 7: Krajewska, G., Holmes, F.E., "Macromodeling of FET/Bipolar Operational Amplifiers," IEEE Journal of Solid-State Circuits, Vol. SC-14, # 6, December 1979.

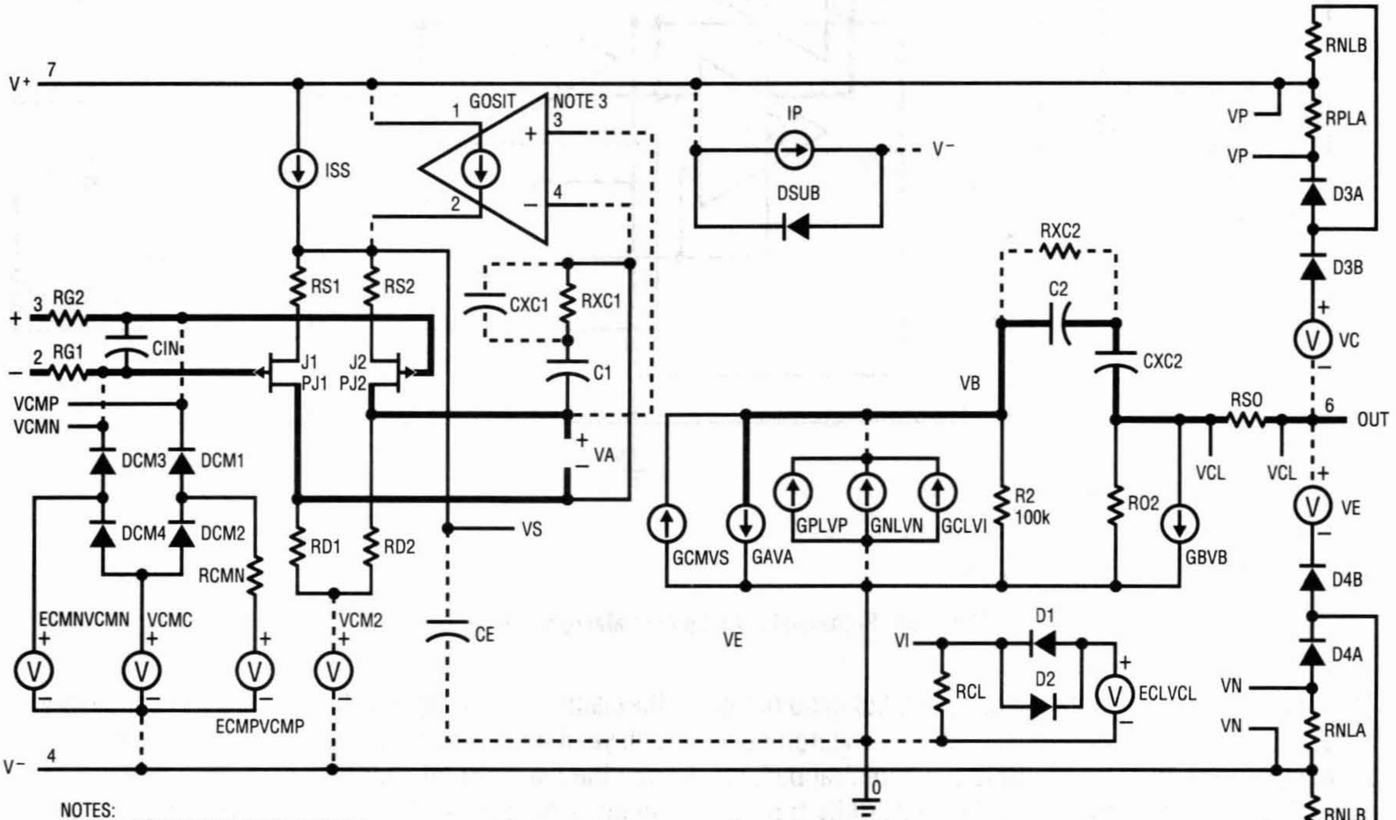
Junction FET input op amps make up an important part of the overall field of op amps, as they are capable of both medium to higher speed performance and have low DC errors. For modeling factors, LTC has chosen to realize a JFET amplifier type, specifically P-channel (PFET) input stage types, with part specific enhancements for the PFET macromodels.

The LTC PFET op amp macromodel is shown in schematic form in Figures 8A and 8B, (simple and detailed respectively). On an overall basis this model is fundamentally similar to that of Krajewska, but it has several adaptations added. It can in fact become one of the more complex models in the LTC library, when all features are used. The following discussions highlight the various enhancements beyond the basic Krajewska form of the Boyle model. Those model improvement areas previously discussed will not be covered in detail. The actual macromodel of an LT1056 (a representative LTC PFET op amp) is shown in Listing 5.

PFET Macromodel Features

At the input side of the PFET macromodel is the J1/J2 front end, which has a number of options possible within this stage. Input capacitance is simulated by C_{IN}, and series gate resistances RG1/RG2 are optionally added.

The optional buffered clamping network around DCM1-DCM4 is quite complex, and warrants some discussion. This circuit simulates the anti-phase reversal common mode clamping present in most (but not all) LTC PFET input amplifiers. In the actual parts which use it, this clamp becomes active whenever the input voltage approaches within 4V (or less) of the negative supply rail. This prevents the sign inversion typically seen in most PFET input op amps, when the negative CM range is exceeded.


V+
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NOTE 3
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V−
DSUB
RNLB
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RPLA
VP
D3A
D3B
VC
RXC2
C2
CXC2
VB
RSO
6
OUT
VCL
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VE
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RG2
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RG1
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CIN
RS1
RS2
CXC1
RXC1
C1
J1
PJ1
J2
PJ2
VA
VCMP
VCMN
DCM3
DCM1
DCM4
DCM2
RCMN
RD1
RD2
VS
ECMNVCMN
VCMC
VCM2
CE
ECMPVCMP
GCMVS
GAVA
GPLVP
GNLVN
GCLVI
R2
100k
RO2
GBVB
D4B
D1
D2
VI
RCL
ECLVCL
D4A
VN
VN
RNLA
RNLB
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4
0

NOTES:
1) SECTIONS SHOWN DOTTED OPTIONAL.
2) OUTPUT VOLTAGE/CURRENT LIMITING CAN VARY.
3) OPTIONAL CONTROLLED SOURCE FOR SR ASYMMETRY.
4) SOURCE RESISTANCE RS1/RS2 OPTIONAL.
5) COMPENSATION ELEMENTS C1/C2 CAN BE EXTENDED.

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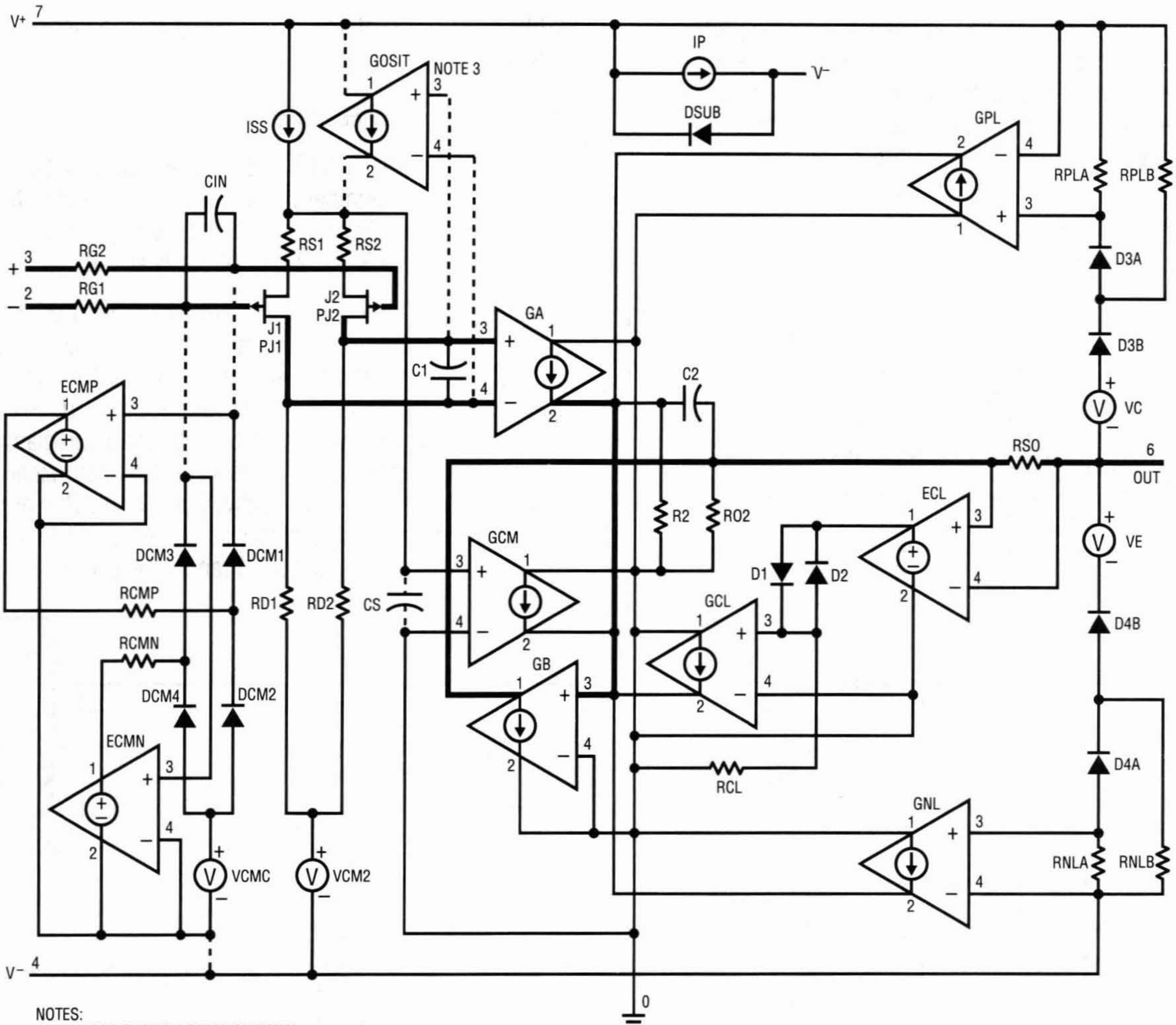
Figure 8A. P-Channel JFET Op Amp Macromodel (Simple)


V+ 7
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V–
DSUB
GPL
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CIN
RPLA
RPLB
RG2
RG1
RS1
RS2
D3A
J1
PJ1
J2
PJ2
GA
D3B
C1
C2
ECMP
VC
RSO
6
OUT
ECL
GCM
R2
RO2
VE
DCM3
DCM1
D1
D2
RCMP
RD1
RD2
CS
GCL
D4B
RCMN
GB
DCM4
DCM2
ECMN
D4A
RCL
GNL
RNLA
RNLB
VCMC
VCM2
V– 4
0
LTAN48 • TA15

NOTES:
1) SECTIONS SHOWN DOTTED OPTIONAL.
2) OUTPUT VOLTAGE/CURRENT LIMITING CAN VARY.
3) OPTIONAL CONTROLLED SOURCE FOR SR ASYMMETRY.
4) SOURCE RESISTANCE RS1/RS2 OPTIONAL.
5) COMPENSATION ELEMENTS C1/C2 CAN BE EXTENDED.

Figure 8B. P-Channel JFET Op Amp Macromodel (Detailed)

The circuit appears moderately complex, but is so out of necessity. For high performance in this macromodel, clamping diodes DCM1 and DCM3 are bootstrapped, for lowest leakage. VCVS followers ECMP and ECMN, through resistances RCMP and RCMN, reduce the voltage seen by these two diodes to a zero potential for inputs where the clamp is *not* active. This is necessary to preserve the low pA bias currents of J1/J2, for normal operating range CM voltages (when the clamp is back biased). In other words, the clamp must clamp effectively below its voltage threshold, yet it must not introduce leakage errors which would ruin the bias current characteristics seen at the op amp input(s). Actually the bootstrapping is quite effective, with DCM1 and DCM3 introducing a pA or less of error.

As noted, this circuit is an option with all LTC PFET input amplifiers which employ a 356 type topology, which includes the LT1056, LT1057, LT1058, LT1022, and older industry standard parts such as the LF156-LF356 series, the OP-15/OP-16 series, and the related duals. Since the clamp circuit is only needed for simulations which need to explore overvoltage CM inputs, it comes commented out within the respective model files.

P-channel JFETs J1/J2 have individual model characteristics calculated to yield an input stage unity gain, gate currents consistent with the I_B/I_{OS} of the amplifier modeled, and the V_{OS} characteristics of the op amp. All of these are as defined by models JM1 and JM2, respectively. For the gain-normalization of the input stage, the JFET transconductance parameter BETA is adjusted for J1/J2, to provide unity gain. Alternatively, source resistances RS1/ RS2 can be used for gain normalization. This option is one that can be exercised at the time the model is created (in the interest of simplicity however, no present models use these resistances). V_{OS} is modeled simply as the difference in the V_{TO} for the two models.

A subtle detail which may not be obvious is the (optional) use of voltage source VCM2, which appears within the LT1056 model (and similar topologies). This bias voltage simulates negative input range change of V_{OS}, characteristic of these amplifiers.

In the inner stages of the model, overall gain and frequency response capability characteristics are similar to the NPN prototype discussed previously, and extensions to both C1 and C2 can optionally be used. These extensions are not used with the LT1056.

As noted in the discussion of gain-normalization, the basic equations which govern this model are quite close to the original Boyle expressions, with the adaptations for different circuit references. These are summarized in Figure 2. The SR of the Figure 8 model is set by the tail current of J1/J2 and C2 for the most simple JFET amplifier cases. However, many P-channel JFET op amps are *not* just simple cases, in the sense that they don't slew symmetrically. For asymmetric slewing JFET amplifiers, the optional circuitry used is described in detail in the Appendix, and it employs the VCCS GOSIT, connected as shown. JFET amplifiers which have symmetric SR characteristics use a more straightforward signal path, where the SR is simply ISS/C2.

The remainder of this model (the output stage with enhanced voltage/current limiters) is similar to the NPN macromodel.

PFET Macromodel Performance

The performance of the LT1056 device, illustrated in the composite pictures of Figure 9, shows many of the key behavior points of this model type.

One of the rather unique aspects of the 355/356 and other family relation PFET op amps is the asymmetrical slewing. With the LT1056, this pattern of behavior is shown in Figure 9, test F1. This test, for a voltage follower on ±15V supplies, slews twice as fast for negative going swings as for positive. The measured rates are +14V/μs, –28V/μs, and the SPICE result here compares well with the data sheet. This transient test runs in around 25s, with minor PSpice power supply ramping to find a bias point.[8] (A .IC command for node 55 minimized the bias iterations, but was not essential).

The demonstration of the voltage clamping circuit and its effect on input currents is shown in Figure 9, test F3. In this test the LT1056 is overdriven as a voltage follower, with a DC sweep input of –15V to +15V. The three part display shows input/output linearity (left), amplifier bias current (middle), and clamping current in the circuit's 10k input resistor (right). For this specific test, the LT1056 model was edited to uncomment the "CMCLAMP" section and activate the limiter.

In the left plot of Figure 9, test F3, the LT1056 shows only low errors due to gain and CM, until the limits are reached. Note that the positive limit is due to the LT1056 output swing limit at positive 13.2V (the negative output limit is –13.2). However, the negative range limit of this follower is due to the *input clamp*, and occurs nearly 2V sooner, just under –11V. This is the clamp threshold of 4V (relative to –15V). In the middle plot, the bias current of J1 is stable

---

[8] **Note 8:** The PSpice simulator used in these tests has an internal bias point seek algorithm to aid in convergence. This routine lowers/raises the supplies to find a suitable biasing condition for the circuit. The necessity for this will vary circuit by circuit, but in general amplifier circuits with initial input conditions which start at some extreme (such as –10V, in this case) can be slower in biasing. A ".IC" command can be used to minimize this, if desired.

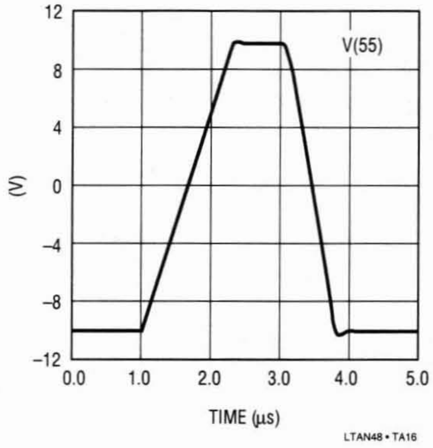

Figure 9A. LT1056 Test F1: Asymmetric Slew Rate

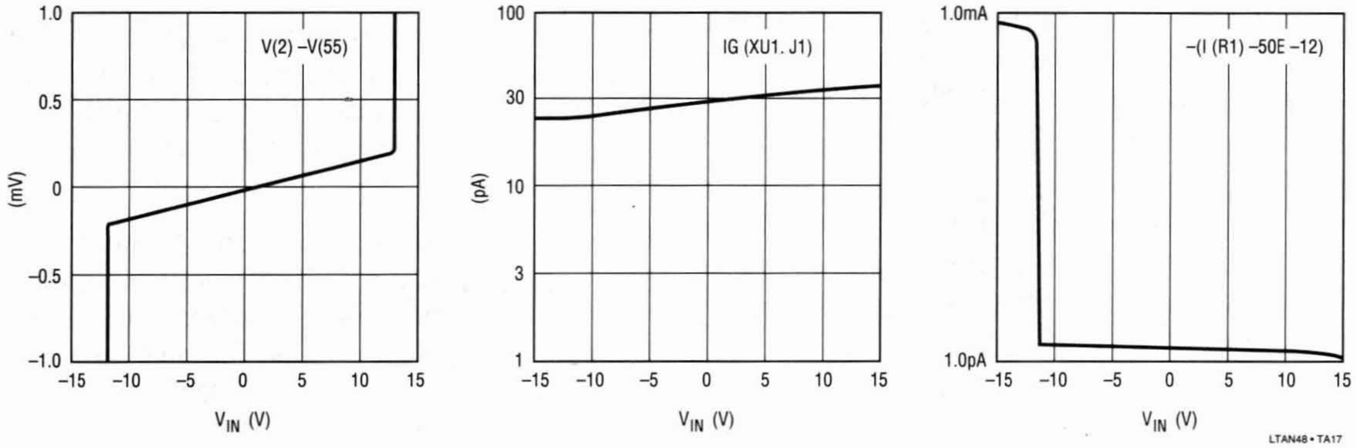

Figure 9B. LT1056 Test F3: Input Clamp, ±15V, Overdriven Follower

Figure 9. Composite Performance Points

over this range, indicating that the overall follower loop is active. In the right plot, the current in the 10k input resistor is displayed for the entire input dynamic range. It is only a few pA within the range where the amplifier is operating linearly, but then rises rapidly to about 400µA, as the clamp takes over.

The LTC P-Type MOSFET (PMOS) Macromodel Family

The LTC PMOS input op amp macromodel is shown in schematic form in Figures 10A and 10B, and a representative model for the LTC1050 is shown in Listing 6. Like the close-cousin PFET amplifier model of Figure 8, this PMOS model resembles the corresponding model of Krajewska,[9] with regards to some aspects of the input stage.

What has been said for the model of Figure 8 is generally true when PMOS transistors are used (M1/M2 in Figure 10 replace J1/J2 of Figure 8). With this PMOS FET adaptation, diodes DG1 and DG2 simulate the bias currents of the device (as opposed to the fixed current sources of the Krajewska model). As was true for the JFET transistor models, the model parameters of these diodes provide for I_B/I_{OS} characteristics. As previously, CIN simulates amplifier input capacitance.

In this PMOS input macromodel much of the remainder of the overall model is similar, and little changes in the

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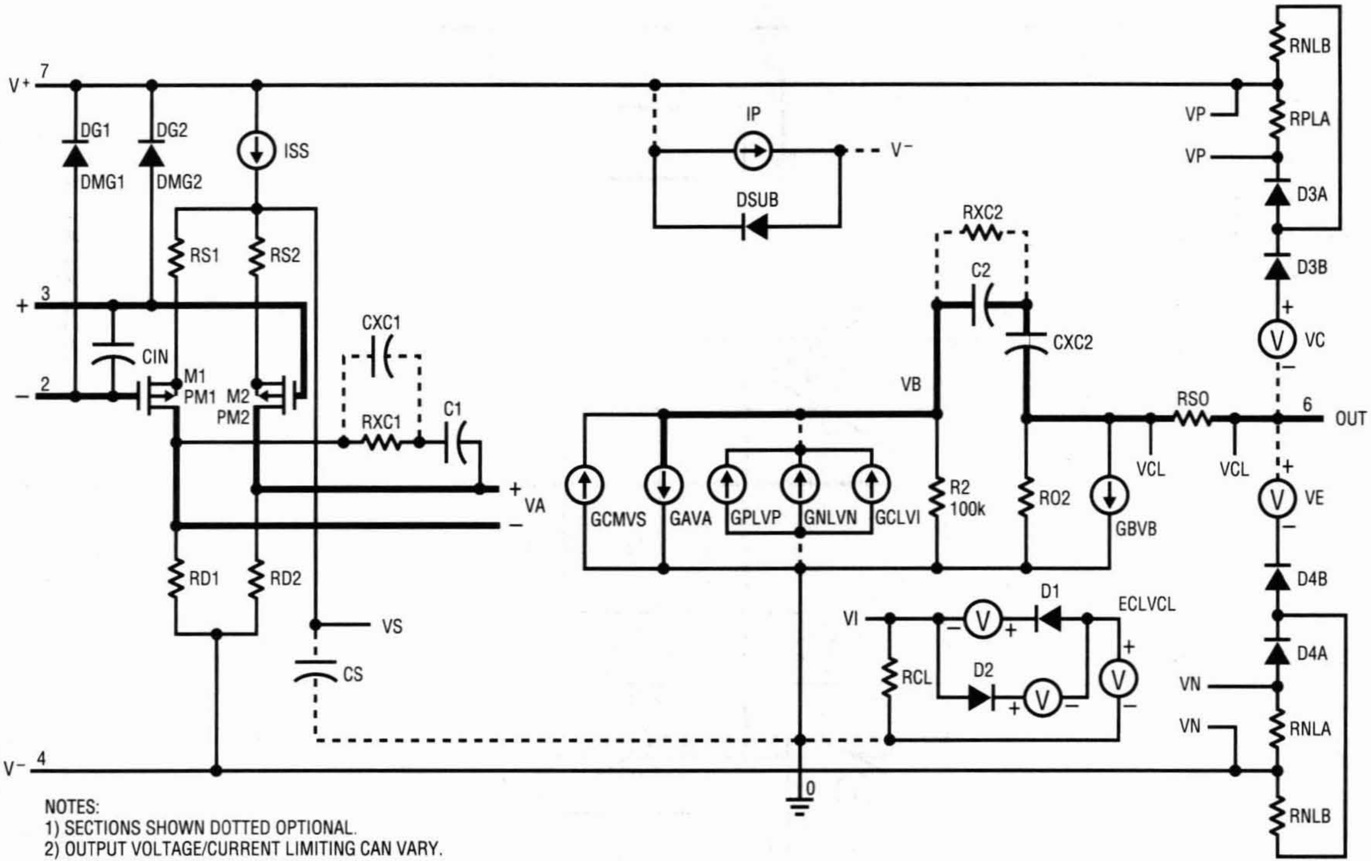
Note 9: Krajewska, G., Holmes, F.E., “Macromodeling of FET/Bipolar Operational Amplifiers,” IEEE Journal of Solid-State Circuits, Vol. SC-14, # 6, December 1979.


V+
7
DG1
DMG1
DG2
DMG2
ISS
RS1
RS2
+
3
CIN
–
2
M1
PM1
M2
PM2
CXC1
RXC1
C1
+
VA
–
RD1
RD2
VS
CS
V–
4
IP
V–
DSUB
GCMVS
GAVA
GPLVP
GNLVN
GCLVI
VB
RXC2
C2
CXC2
R2
100k
RO2
GBVB
VCL
VCL
RSO
6
OUT
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VI
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RCL
D2
VP
VP
RNLB
RPLA
D3A
D3B
VC
VE
D4B
D4A
VN
VN
RNLA
RNLB
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NOTES:
1) SECTIONS SHOWN DOTTED OPTIONAL.
2) OUTPUT VOLTAGE/CURRENT LIMITING CAN VARY.
3) SOURCE RESISTANCES RS1/RS2 OPTIONAL.
4) COMPENSATION ELEMENTS C1/C2 CAN BE EXTENDED.

Figure 10A. PMOS FET Op Amp Macromodel (Simple)

equations (refer to Figure 2 again). Practically speaking, the variation of a PMOS input stage model allows such useful device categories as the low I_B and very low V_{OS} chopper-stabilized units.[10] Accurate rail-rail output limit characteristics also allow features of single supply CMOS technologies to be realistically modeled.

PMOS Macromodel Features

One area where the emphasis on fidelity to the actual devices influences a model is found in this PMOS macromodel. While it is in fact more complex, it is so for the reason of better match to the real parts. But, IC vendors haven't all taken such steps in modeling op amps with PMOS inputs and CMOS outputs. For example, inspection of some models released show such obvious deficiencies as input transistors unlike what is in the part actually modeled, and/or a lack of close attention to output limiting levels. Obviously, such models can't simulate input or output CM ranges with a high degree of fidelity, even though these factors can be critical to single supply use.

The output current/voltage limiters used with the LTC PMOS model are of the more complex form shown because of several important performance issues. For example, amplifiers emulated by these PMOS models have rail-rail outputs, with mV level saturation voltages typical of CMOS outputs. The amplifiers also have the 160dB gains, 140dB CMRRs, and sub-microvolt V_{OS} levels, as is typical of chopper stabilized amps. Many of these performance characteristics are made possible by some model

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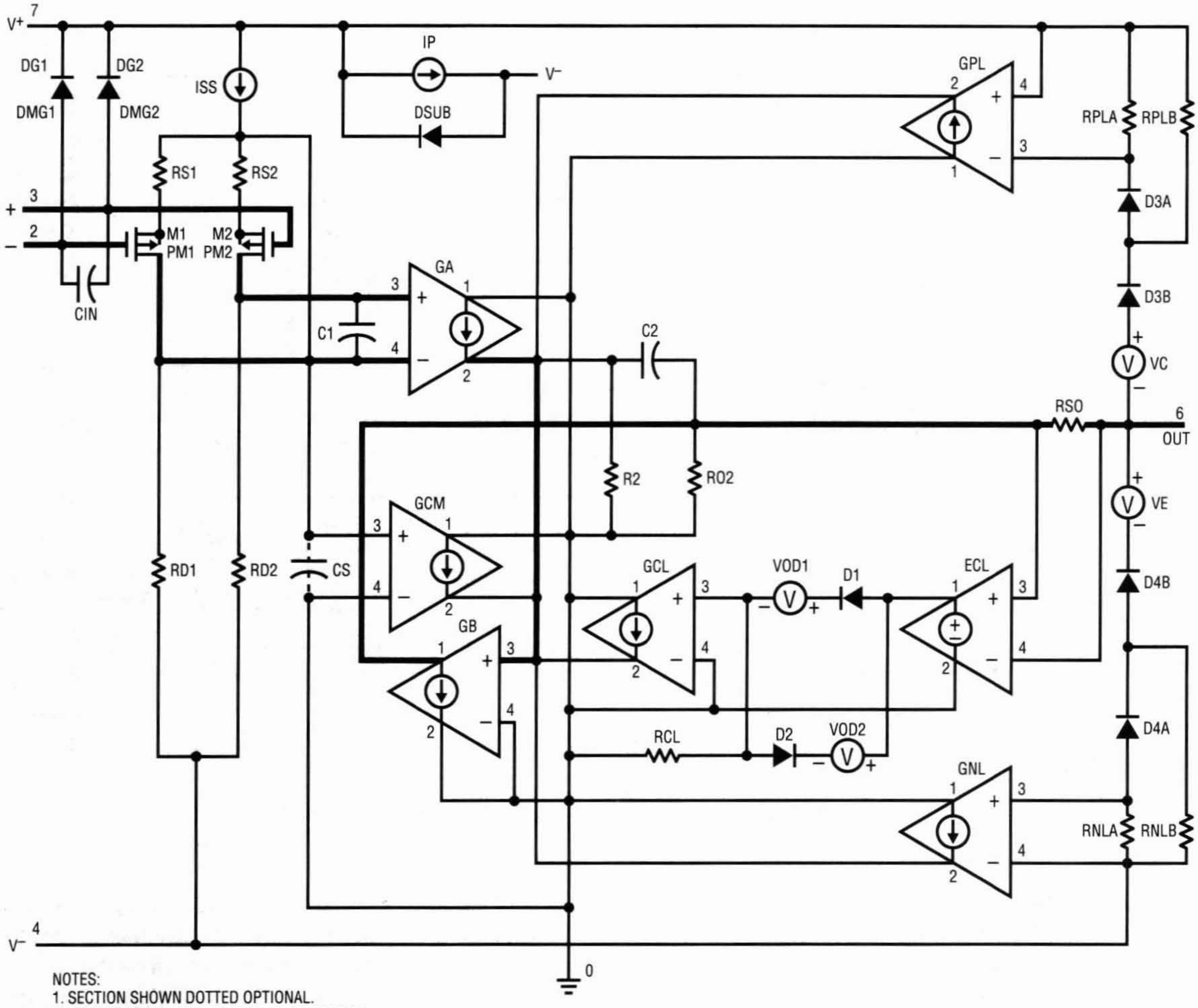
[10] **Note 10:** These models emulate actual LTC chopper amplifiers in terms of the ultra low offset, the high gain, and also in terms of single (low voltage) supply operation, input/output ranges, etc. However, there is no actual commutation function, and therefore the effects of clocking parasitics of the actual device aren't modeled.


V+
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DG1
DG2
DMG1
DMG2
ISS
IP
V–
DSUB
GPL
RPLA
RPLB
D3A
D3B
VC
RS1
RS2
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2
M1
PM1
M2
PM2
CIN
GA
C1
C2
RSO
6
OUT
R2
RO2
GCM
RD1
RD2
CS
GCL
VOD1
D1
ECL
VE
D4B
GB
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RNLA
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NOTES:
1. SECTION SHOWN DOTTED OPTIONAL.
2. OUTPUT VOLTAGE/CURRENT LIMITING VARY.
3. SOURCE RESISTANCES RS1/RS2 OPTIONAL.
4. COMPENSATION ELEMENTS C1/C2 CAN BE EXTENTED.

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Figure 10B. PMOS FET Op Amp Macromodel (Detailed)

features shown in Figure 10, such as the already discussed improved voltage limiters, for very low saturation voltages with minimal gain error.

The current limiting in this model also has some unique performance issues. Most current limit schemes used within op amp macromodels are symmetrical regarding sinking/sourcing output current, as previously described for the NPN macromodel limiter. For the most part this is not a problem, since most op amps also have symmetric limits.

However, some amplifier types do not limit symmetrically at all, and may have a skew of 3-5 times between the sinking/sourcing current levels. A case in point are those amplifiers which have CMOS common drain outputs, where the upper P device can source less current than the lower N device can sink. For example the LTC1050 under discussion can source 5mA of current, while it can sink 20mA.

The LTC improved modeling method for current limiting allows different degrees of asymmetry to be incorporated.

In the circuits of Figure 10 the output current is sampled by a low value series resistor, RSO, typically 1Ω. The current proportional voltage drop across RSO is scaled by VCVS ECL, which of course eliminates any possible loading effects on the output. As noted with the NPN model, this technique was in fact developed to remove loading effects of brute-force limiting, which can cause gain errors in a very high gain amplifier such as the LTC1050. While any op amp being modeled with gain of more than 120dB can be subject to limiter-related loading errors, in chopper-type amplifiers where gains are typically 160dB or more, it can become critical.

Along with the value of RSO, the gain of ECL plus the diodes D1/D2 and voltage sources VOD1/VOD2 are selected to provide separate ±current limit thresholds. The gain of ECL is common for both current limits, and the two voltage sources are adjusted to reflect the desired threshold for sinking/sourcing of current. In the LTC1050 model, the source and sink currents are 5mA and 20mA, respectively. Should there be a model case of equal currents, then the diodes are the same and the voltage sources are dropped.

PMOS Macromodel Performance

The performance of the LTC1050 op amp is illustrated in the composite pictures of Figure 11.

A test which demonstrates the rail-rail response characteristics is shown in Figure 11, test F7. The conditions of this test are a unity gain inverter with a single supply of +5V, driven with an input DC sweep of –6V to +1V. This deliberately overdrives the amplifier at both dynamic range extremes. The two plots show the input/output error highly magnified, a relatively sensitive test of saturation near the ± rails. The upper trace shows the general behavior, while the bottom trace shows the error on a ±10mV scale. Even on the expanded scale the input/output error is hard to see, but it is about 12mV with the output at 100mV from either rail, 500μV at 200mV, 12μV at 300mV, and essentially at the V_{OS} level for lower voltages.

As noted previously, a unique feature of the PMOS macromodel type is the ability to have different ±output current limits. With the LTC1050 model tested, this asymmetrical limiting is shown in Figure 11, test F6. For this test the conditions are an open loop comparator with ±5V supplies and a 10Ω load. As can be noted, the current in load resistor R3 is +5mA/–20mA.

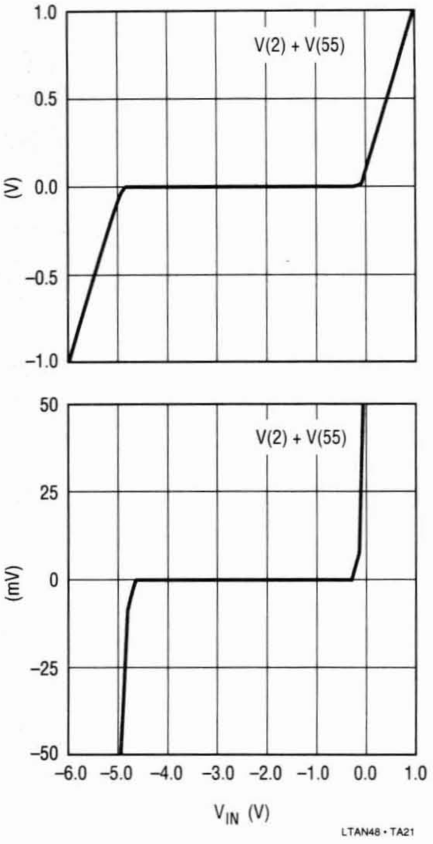

Figure 11A. LTC1050 Test F7: Input/Output Linearity, SS (–) Mode

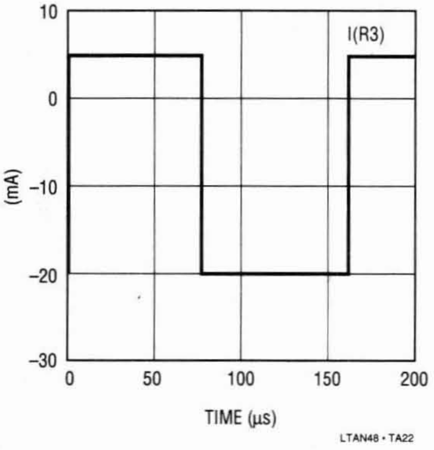

Figure 11B. LTC1050 Test F6: I_{SC} (V_S = ±5V)

Figure 11. Composite Performance Points

Examples of LTC op amps using this PMOS model are the LTC1050 series, and related parts in the chopper stabilized family.

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6. Jung, W. G., "Questions and Answers on the SPICE Macromodel Library," Linear Technology Application Note # 41, April, 1990.
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8. Jung, W. G., "Using Op Amp Macromodels," Electronic Products, June, 1990
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SPICE documents available from: EECS/ERL Industrial Support Office, 497 Cory Hall, University of California at Berkeley, Berkeley, CA 94720

APPENDIX

Improved JFET Op Amp Model Slews Asymmetrically

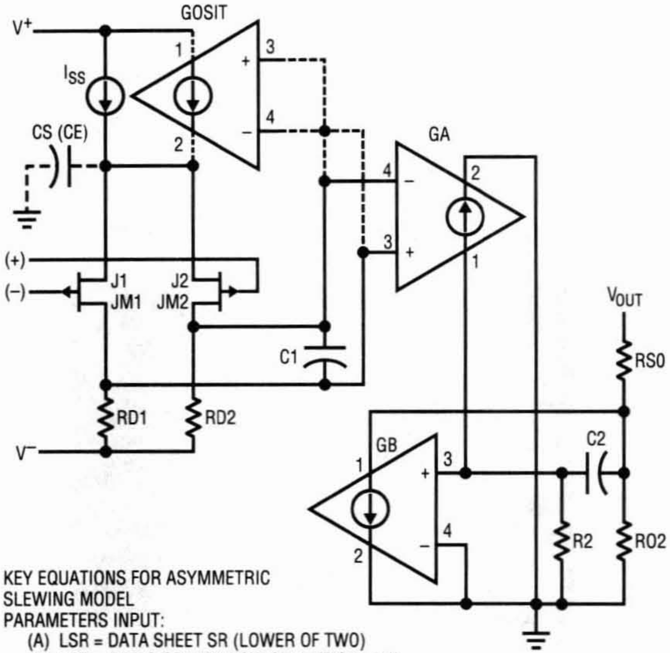
SPICE macromodels for op amps have been available for some time, for both bipolar(1, 2) and JFET(3) input stage device types. Interestingly however, not much attention has been given in the models available to controlled slewing asymmetry. Dependent upon a given amplifier design topology, the large signal characteristics can have various degrees of slew rate (SR) asymmetry. It therefore makes good sense to have models which emulate real IC parts in this regard.

A case in point is that of the available P-channel JFET input op amps, many which have a characteristic SR response which is asymmetrical. In fact, popular op amps with topologies like the original 355/356 types are intrinsically faster for negative going output swings than they are for positive. Similar comments apply to such related devices as the OP-15, OP-16, etc. Since this type of JFET device topology was introduced, the SR specified on the data sheet has typically been the *lower* of two dissimilar rates, i.e., the slower, *positive* edge SR. Thus, given an op amp with a typical SR spec of 14V/µs for positive going edges, the same amp will have a corresponding negative SR of about 28V/µs.

Ironically, this quite common JFET amplifier slewing characteristic has not been well modeled thus far. Most macromodels currently available simply do not address the asymmetric SR issue at all. Others have means of modeling it, but it is seldom found used.

A means of SR control was built into the original Boyle(1) model, and it addresses SR asymmetry for common mode

(CM) signals by means of a common emitter (source) capacitor, CE (CS, for JFET amps). However, using this capacitor alone for a general SR symmetry control mechanism leaves something to be desired, as the resulting slopes are not consistent. LTC has implemented a new means of modeling SR asymmetry, shown in Figure A1.



KEY EQUATIONS FOR ASYMMETRIC
SLEWING MODEL
PARAMETERS INPUT:
(A) LSR = DATA SHEET SR (LOWER OF TWO)
(B) DSR = RATIO OF HIGH/LOW SR (TYPICAL 2/1)

FOR A 1056 TYPE AMPLIFIER (356 TOPOLOGY),
HSR = HIGHER OF TWO SR = DSR • LSR
= 2 • 14V/μs = 28V/μs
ISR = INTERMEDIATE SR
= 4/3 • LSR
= 18.67V/μs

I_{SS} = ISR • C2
= 560μA WITH C2 = 30pF
GOSIT = I_{SS} /2
LSR = 14V/μs, DSR = 2

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Figure A1. The LTC Asymmetric Slewing JFET Macromodel Has Little Additional Complexity, But Offers Controlled Slewing Response

The circuit as shown here is a simplified Boyle type model with P-channel JFET input devices, J1 and J2. As this type (or similar input structure) of model is typically used, the SR is simply ISS/C2, which is symmetrical when CS is zero. When the common source capacitor CS is added, the SR for CM signals can be adapted (corresponds to CE in the Boyle paper). Unfortunately, this strategy works best for CM amplifier inputs, and not as well for inverting inputs.

The LTC method of modeling asymmetrical SR employs an added VCCS (shown dotted), which dynamically modifies the total tail current available to J1/J2. This controlled source, "GOSIT," is driven by the differential output of J1/J2 and produces a current which adds/subtracts to/from the fixed current, ISS. The resulting current available to charge/discharge compensation capacitor C2 is thus higher for one slewing slope than it is for the opposite. This is true regardless of whether the amplifier is operating in an inverting or non-inverting input mode. As an option, CS can still be used for further control of slewing for CM inputs (shown dotted).

In generating a new macromodel with asymmetrical SR, the *lower* of the two slew rates is input from the data sheet. Also input is the *ratio* of the high-to-low SR. Algorithms in the program used by LTC then calculate an appropriate static value or ISS and the gain of VCCS GOSIT, so that the proper slewing characteristic will be produced by the model.

A representative example op amp with these characteristics is the LT1056, a high performance op amp topologically much like the LF156-LF356 and OP-16 types (also produced by LTC, with corresponding macromodels available). Some sample lines of code taken directly from the released LT1056 model are shown below. These are shown for both the asymmetric form as released, and for an (edited) symmetric case.

Actually, only one SPICE model element is added to produce the asymmetric SR as opposed to symmetric, and that is the VCCS, GOSIT. The LT1056 example just below, taken from the released library, produces SRs of +14V/μs and –28V/μs, respectively.

```
** END CM CLAMP
C1 80 90 1.5000E-11
ISS 7 12 5.6000E-04
GOSIT 7 12 90 80 2.8000E-04
* INTERMEDIATE
```

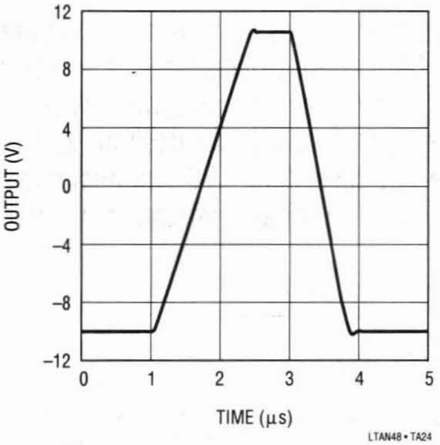
When the controlled source GOSIT is omitted, the model reverts to simple symmetric slewing, where the SR will be ±(ISS)/C2. This is shown below, with ISS adjusted for a (symmetric) SR of 14V/μs. Those lines of code edited are shown below in **bold**.

```
** END CM CLAMP
C1  80 90 1.5000E-11
* for a (symmetric) SR of 14V/μs,
* ISS = (1.4e7)*(3e –11) = 420µA
ISS 7 12 4.2000E-04
* comment out GOSIT with first column "*"
* GOSIT 7 12 90  80  2.8000E-04
* INTERMEDIATE

* Also, if a similar GBP is desired, adjust the
* BETA (only) parameter of models JM1/JM2
* BETA should be adjusted by the
* inverse proportion of the ISS change, or,
* in this case 1/(420/560) = 560/420 = 1.33 times,
* as:
.MODEL JM1 PJF (IS = 1.1000E –11
+ BETA = 1.267E-03 VTO = –1.000000E +00)
```

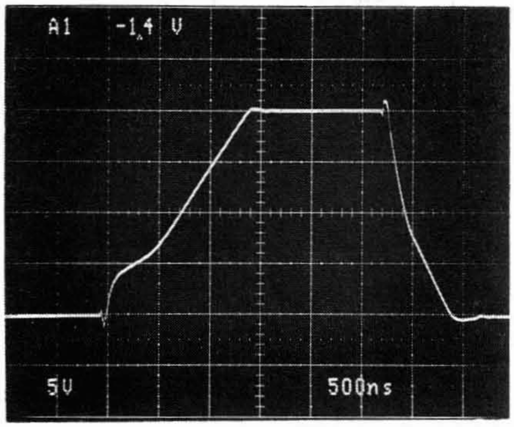
Note again that this adjustment to BETA applies to *both* JM1 and JM2, and that *no other* inline .MODEL parameters should be changed. (There is no harm if BETA is not changed, except for a low GBP).

The non-inverting mode waveforms of a typical SPICE run using the LT1056 macromodel and parallel lab results with an actual LT1056 device are shown in Figure 2.



LTAN48 • TA24

Figure 2A. LT1056 SR (+) Mode, Macromodel



LTAN48 • TA25

Figure 2B. LT1056 SR (+) Mode, Lab Photo

Listing 1

```
*
* Linear Technology 8741 op amp model
* Written: 10-29-1990 12:55:37 Type: Bipolar NPN input, internal comp.
* Typical specs:
* Vos=3.0E-04, Ib=2.6E-07, Ios=7.0E-10, GBP=1.2E+06Hz, Phase mar.= 73.2 deg,
* SR(-)=9.0E-01V/us, SR(+)=7.2E-01V/us, Av=112.4dB, CMRR=106.0dB,
* Vsat(+)=0.800V, Vsat(-)=2.300V, Isc=+26/-26mA, Rout= 566ohms, Iq=1.98mA.
* (As per Boyle Appendix)
*
* Connections: + - V+V-O
.SUBCKT 8741 3 2 7 4 6
* INPUT
RC1 7 80 4.3521E+03
RC2 7 90 4.3521E+03
Q1 80 2 10 QM1
Q2 90 3 11 QM2
CIN 2 3 2.0000E-12
C1 80 90 4.5288E-12
RE1 10 12 +2.3917E+03
RE2 11 12 +2.3917E+03
IEE 12 4 2.7512E-05
RE 12 0 7.2696E+06
CE 12 0 7.5000E-12
* INTERMEDIATE
GCM 0 8 12 0 1.1516E-09
GA 8 0 80 90 2.2978E-04
R2 8 0 1.0000E+05
C2 1 8 3.0000E-11
GB 1 0 8 0 3.2110E+01
RO2 1 0 5.6500E+02
* OUTPUT
RSO 1 6 1.0000E+00
ECL 18 0 1 6 3.2808E+01
GCL 0 8 20 0 1.0000E+00
RCL 20 0 1.0000E+01
D1 18 19 DM1
VOD1 19 20 0.0000E+00
D2 20 21 DM1
VOD2 21 18 0.0000E+00
*
D3A 131 70 DM3
D3B 13 131 DM3
GPL 0 8 70 7 1.0000E+00
VC 13 6 2.1831E+00
RPLA 7 70 1.0000E+01
RPLB 7 131 1.0000E+03
D4A 60 141 DM3
D4B 141 14 DM3
GNL 0 8 60 4 1.0000E+00
VE 6 14 3.6831E+00
RNLA 60 4 1.0000E+01
RNLB 141 4 1.0000E+03
*
IP 7 4 1.9525E-03
DSUB 4 7 DM2
* MODELS
.MODEL QM1 NPN (IS=8.0000E-16 BF=5.2662E+01)
.MODEL QM2 NPN (IS=8.0928E-16 BF=5.2807E+01)
.MODEL DM1 D (IS=1.0000E-20)
.MODEL DM2 D (IS=8.0000E-16 BV=4.8000E+01)
.MODEL DM3 D (IS=1.0000E-16)
.ENDS 8741
*
* - - - - - * FINI 8741 * - - - - - * [OAMM VN02 10/29/90]
```

Listing 2

```
.SUBCKT LT1007 3 2 7 4 6
RC1 7 80 6.6315E+02
RC2 7 90 6.6315E+02
Q1 80 2 10 QM1
Q2 90 3 11 QM2
*
C1 80 91 200E-12
RXC1 91 90 50
CXC1 91 90 500E-12
C2 8 98 4.000E-12
RXC2 8 98 4.00K
CXC2 1 98 27.000E-12
*
CIN 3 2 5E-12
DDM1 2 104 DM2
DDM3 104 3 DM2
DDM2 3 105 DM2
DDM4 105 2 DM2
RE1 10 12 -2.6233E+01
RE2 11 12 -2.6233E+01
IEE 12 4 7.5030E-05
RE 12 0 2.666E+06
CE 12 0 1.579E-12
GCM 0 8 12 0 7.558E-10
GA 8 0 80 90 1.5080E-03
R2 8 0 1.000E+05
GB 1 0 8 0 1.9176E+03
RO2 1 0 6.900E+01
*
RS 1 6 1
ECL 18 0 1 6 2.828E+01
GCL 0 8 20 0 1
RCL 20 0 1E3
D1 18 20 DM1
D2 20 18 DM1
*
D3A 131 70 DM3
D3B 13 131 DM3
GPL 0 8 70 7 1
VC 13 6 3.0909
```

```
RPLA 7 70 1E4
RPLB 7 131 1E5
D4A 60 141 DM3
D4B 141 14 DM3
GNL 0 8 60 4 1
VE 6 14 3.0909
RNLA 60 4 1E4
RNLB 141 4 1E5
*
IP 7 4 2.625E-03
DSUB 4 7 DM2
* MODELS
.MODEL QM1 NPN (IS=8.0000E-16 BF=1.7857E+03)
.MODEL QM2 NPN (IS=8.0062E-16 BF=4.1667E+03)
.MODEL DM1 D (IS=1.000E-19)
.MODEL DM2 D (IS=8.000E-16)
.MODEL DM3 D (IS=1.000E-20)
.ENDS LT1007
*
.SUBCKT LT1007CS 3 2 7 4 6
X_LT1007CS 3 2 7 4 6 LT1007
.ENDS LT1007CS
* - - - - - * FINI LT1007 FAMILY * - - - - - *
```

Listing 3

```
.SUBCKT LT1013 1 2 3 4 5
*
C1 11 12 8.661E-12
C2 6 7 30.00E-12
DC 8 53 DX
DE 54 8 DX
DLP 90 91 DX
DLN 92 90 DX
DP 4 3 DX
EGND 99 0 POLY(2) (3,0) (4,0) 0 .5 .5
FB 7 99 POLY(5) VB VC VE VLP VLN 0 2.475E9 -2E9 2E9 2E9 -2E9
GA 6 0 11 12 113.1E-6
GCM 0 6 10 99 225.7E-12
IEE 3 10 DC 12.03E-6
HLIM 90 0 VLIM 1K
Q1 11 102 13 QM1
Q2 12 101 14 QM2
RB1 2 102 400
RB2 1 101 400
DCM1 105 102 DX
DCM2 105 101 DX
VCMC 105 4 DC 0.4
R2 6 9 100.0E3
RC1 4 11 8.841E3
RC2 4 12 8.841E3
RE1 13 10 4.519E3
RE2 14 10 4.519E3
REE 10 99 16.63E6
RO1 8 5 80
RO2 7 99 25
IP 3 4 328E-6
VB 9 0 DC 0
VC 3 53 DC 1.610
VE 54 4 DC .61
VLIM 7 8 DC 0
VLP 91 0 DC 25
VLN 0 92 DC 25
.MODEL DX D(IS=800.0E-18)
.MODEL QM1 PNP (IS=8.000E-16 BF=3.974E+02)
.MODEL QM2 PNP (IS=8.019E-16 BF=4.027E+02)
.ENDS
```

Listing 4

```
.SUBCKT LT1078 3 2 7 4 6
* INPUT
RC1 4 80 2.653E+04
RC2 4 90 2.653E+04
Q1 80 102 10 QM1
Q2 90 103 11 QM2
RB1 2 102 6.000E+02
RB2 3 103 6.000E+02
DCM1 105 102 DM2
DCM2 105 103 DM2
VCMC 105 4 4.000E-01
C1 80 90 8.660E-12
RE1 10 12 4.958E+03
RE2 11 12 4.958E+03
IEE 7 12 2.412E-06
RE 12 0 8.292E+07
CE 12 0 1.579E-12
* INTERMEDIATE
GCM 0 8 12 0 1.501E-10
GA 8 0 80 90 3.770E-05
R2 8 0 1.000E+05
C2 1 8 3.000E-11
GB 1 0 8 0 2.449E+02
* OUTPUT
RO1 1 110 1.000E+02
RO2A 1 0 1.083E+03
RO2B 6 110 8.170E+02
EC 17 0 110 0 1
D1 1 17 DM1
D2 17 1 DM1
D3 110 13 DM2
D4 14 110 DM2
D5 6 110 DM2
D6 110 6 DM2
VC 7 13 1.490E+00
VE 14 4 7.911E-01
IP 7 4 4.259E-05
DSUB 4 7 DM2
* MODELS
.MODEL QM1 PNP (IS=8.000E-16 BF=1.992E+02)
```

```
.MODEL QM2 PNP (IS=8.012E-16 BF=2.008E+02)
.MODEL DM1 D (IS=3.718E-24)
.MODEL DM2 D (IS=8.000E-16)
.ENDS LT1078
*
.SUBCKT LT1079 3 2 7 4 6
X_LT1079 3 2 7 4 6 LT1078
.ENDS LT1079
*
.SUBCKT LT1077 3 2 7 4 6
X_LT1077 3 2 7 4 6 LT1078
.ENDS LT1077
*
* - - - - - * FINI LT1078 FAMILY * - - - - - * [OAMM VP02 5/11/90]
```

Listing 5

```
.SUBCKT LT1056 3 2 7 4 6
* INPUT
VCM2 40 4 2.0000E+00
RD1 40 80 9.6458E+02
RD2 40 90 9.6458E+02
J1 80 102 12 JM1
J2 90 103 12 JM2
CIN 2 3 4.0000E-12
RG1 2 102 2.0000E+00
RG2 3 103 2.0000E+00
** CM CLAMP
* DCM1 107 103 DM4
* DCM2 105 107 DM4
* VCMC 105 4 4.0E+00
* ECMP 106 4 103 4 1
* RCMP 107 106 1E+04
* DCM3 109 102 DM4
* DCM4 105 109 DM4
* ECMN 108 4 102 4 1
* RCMN 109 108 1E+04
** END CM CLAMP
C1 80 90 1.5000E-11
ISS 7 12 5.6000E-04
GOSIT 7 12 90 80 2.8000E-04
* INTERMEDIATE
GCM 0 8 12 0 1.3052E-08
GA 8 0 80 90 1.0367E-03
R2 8 0 1.0000E+05
C2 1 8 3.0000E-11
GB 1 0 8 0 7.8368E+01
RO2 1 0 4.9000E+01
* OUTPUT
RSO 1 6 1.0000E+00
ECL 18 0 1 6 1.7377E+01
GCL 0 8 20 0 1.0000E+00
RCL 20 0 1.0000E+03
D1 18 20 DM1
D2 20 18 DM1
*
D3A 131 70 DM3
D3B 13 131 DM3
GPL 0 8 70 7 1.0000E+00
VC 13 6 2.9595E+00
RPLA 7 70 1.0000E+04
RPLB 7 131 1.0000E+05
D4A 60 141 DM3
D4B 141 14 DM3
GNL 0 8 60 4 1.0000E+00
VE 6 14 2.9595E+00
RNLA 60 4 1.0000E+04
RNLB 141 4 1.0000E+05
*
IP 7 4 4.4400E-03
DSUB 4 7 DM2
* MODELS
.MODEL JM1 PJF (IS=1.1000E-11 BETA=9.5964E-04 VTO=-1.000000E+00)
.MODEL JM2 PJF (IS=9.0000E-12 BETA=9.5964E-04 VTO=-9.998600E-01)
.MODEL DM1 D (IS=1.0000E-15)
.MODEL DM2 D (IS=8.0000E-16 BV=4.8000E+01)
.MODEL DM3 D (IS=1.0000E-16)
.MODEL DM4 D (IS=1.0000E-09)
.ENDS LT1056
*
* - - - - - * FINI LT1056 * - - - - - * [OAMM VJ02 05/08/90]
```

Listing 6

```
.SUBCKT LTC1050 3 2 7 4 6
* INPUT
RD1 4 80 2.1221E+03
RD2 4 90 2.1221E+03
M1 80 2 12 12 PM1
M2 90 3 12 12 PM2
CIN 2 3 5.0000E-12
DG1 2 7 DMG1
DG2 3 7 DMG2
C1 80 90 1.5000E-11
ISS 7 12 1.2000E-04
CS 12 0 1.2857E-11
* INTERMEDIATE
GCM 0 8 12 0 1.4902E-10
GA 8 0 80 90 4.7124E-04
R2 8 0 1.0000E+05
C2 1 8 3.0000E-11
GB 1 0 8 0 1.0664E+04
RO2 1 0 1.9900E+02
* OUTPUT
RSO 1 6 1.0000E+00
ECL 18 0 1 6 1.7955E+02
GCL 0 8 20 0 1.0000E+00
RCL 20 0 1.0000E+01
D1 18 19 DM1
VOD1 19 20 0.0000E+00
```

```
D2 20 21 DM1
VOD2 21 18 2.6932E+00
*
D3A 131 70 DM3
D3B 13 131 DM3
GPL 0 8 70 7 1.0000E+00
VC 13 6 1.4332E+00
RPLA 7 70 1.0000E+01
RPLB 7 131 1.0000E+03
D4A 60 141 DM3
D4B 141 14 DM3
GNL 0 8 60 4 1.0000E+00
VE 6 14 1.4332E+00
RNLA 60 4 1.0000E+01
RNLB 141 4 1.0000E+03
*
IP 7 4 8.8000E-04
DSUB 4 7 DM2
* MODELS
.MODEL PM1 PMOS (KP=1.8506E-03 VTO=-1.1000000E+00)
.MODEL PM2 PMOS (KP=1.8506E-03 VTO=-1.1000005E+00)
.MODEL DM1 D (IS=1.0000E-20)
.MODEL DM2 D (IS=8.0000E-16 BV=1.9800E+01)
.MODEL DM3 D (IS=1.0000E-16)
.MODEL DMG1 D (IS=2.0010E-11)
.MODEL DMG2 D (IS=9.9998E-15)
.ENDS LTC1050
*
* - - - - - * FINI LTC1050 * - - - - - * [OAMM VM02 5/11/90]
```

LINEAR TECHNOLOGY
Application Note 49
August 1992

Illumination Circuitry for Liquid Crystal Displays

Tripping the Light Fantastic . . .

Jim Williams

Current generation portable computers and instruments utilize back-lit liquid crystal displays (LCDs). Cold Cathode Fluorescent Lamps (CCFLs) provide the highest available efficiency for backlighting the display. These lamps require high voltage AC to operate, mandating an efficient high voltage DC-AC converter. In addition to good efficiency, the converter should deliver the lamp drive in the form of a sine wave. This is desirable to minimize RF emissions. Such emissions can cause interference with other devices, as well as degrading overall operating efficiency. The circuit should also permit lamp intensity control from zero to full brightness with no hysteresis or "pop-on."

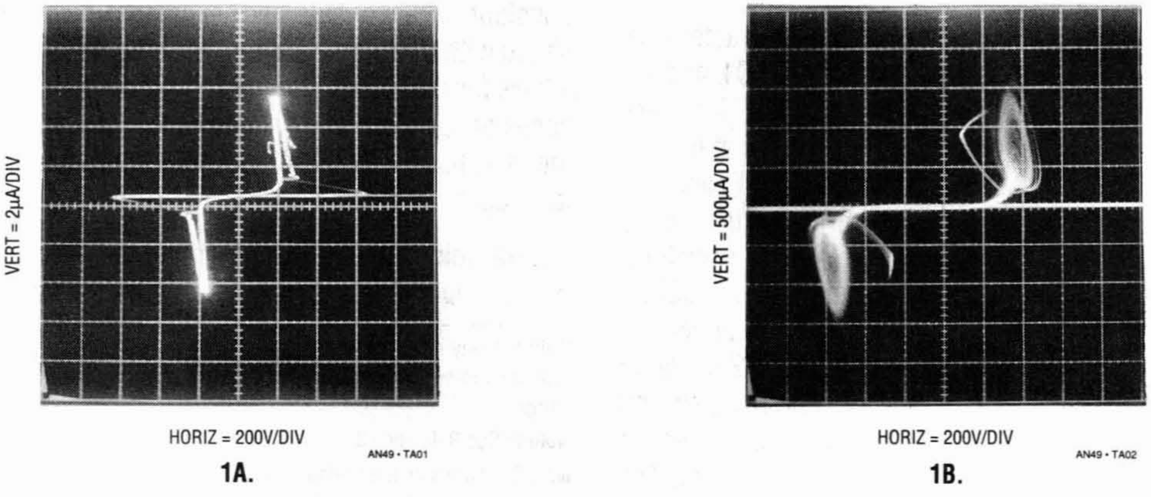
The LCD also requires a bias supply for contrast control. The supply's negative output should be regulated, and variable over a considerable range.

The small size and battery powered operation associated with LCD equipped apparatus mandate low component count and high efficiency for these circuits. Size constraints place severe limitations on circuit architecture, and long battery life is usually a priority. Laptop and hand held portable computers offer an excellent example. The CCFL and its power supply are responsible for almost 50% of the battery drain. Additionally, these components, including PC board and all hardware, usually must fit within the LCD enclosure with a height restriction of 0.25".

Cold Cathode Fluorescent Lamp (CCFL) Power Supplies

Any discussion of CCFL power supplies must consider lamp characteristics. These lamps are a difficult load to drive, particularly for a switching regulator. They have a "negative resistance" characteristic; the starting voltage is significantly higher than the operating voltage. Typically, the start voltage is about 1000V, although higher and lower voltage bulbs are common. Operating voltage is usually 300V to 400V, although other bulbs may require different potentials (see Appendix E for a comparison of various backlights). The bulbs will operate from DC, but migration effects within the bulb will quickly damage it. As such, the waveform must be AC. No DC content should be present.

Figure 1A shows an AC driven bulb's characteristics on a curve tracer. The negative resistance induced "snapback" is apparent. In Figure 1B another bulb, acting against the curve tracer's drive, produces oscillation.



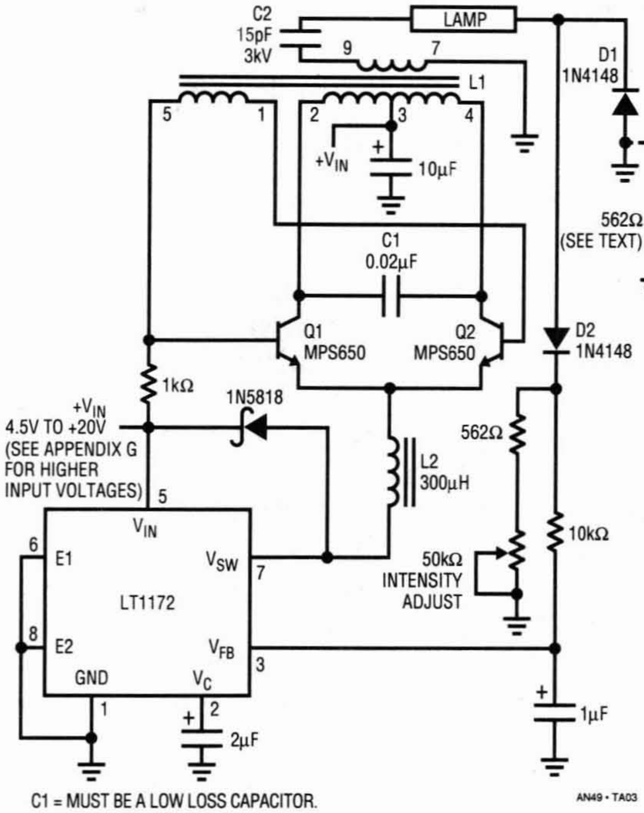
1A. 1B.

Figure 1. Negative Resistance Characteristic for Two CCFL Bulbs. "Snap Back" is Readily Apparent, Causing Oscillation in 1B. These Characteristics Complicate Power Supply Design

These tendencies, combined with the frequency compensation problems associated with switching regulators, can cause severe loop instabilities, particularly on start-up. Once the lamp is in its operating region it assumes a linear load characteristic, easing stability criteria.

Bulb operating frequencies are typically 20kHz to 100kHz, and a sine-like waveform is preferred. The sine drive's low harmonic content minimizes RF emissions, which could cause interference and efficiency degradation.[1]

Figure 2's circuit meets CCFL drive requirements. Efficiency is 78% with an input voltage range of 4.5V to 20V. 82% efficiency is possible if the LT1172 is driven from a low voltage (e.g., 3V-5V) source. Additionally, lamp intensity is continuously and smoothly variable from zero to full intensity. When power is applied the LT1172 switching regulator's feedback pin is below the device's internal 1.23V reference, causing full duty cycle modulation at the V_{SW} pin (trace A, Figure 3). L2 conducts current (trace B), which flows from L1's center tap, through the transistors, into L2. L2's current is deposited in switched fashion to ground by the regulator's action.



C1 = MUST BE A LOW LOSS CAPACITOR.
METALIZED POLYCARB
WIMA FKP2 (GERMAN) RECOMMENDED.
L1 = SUMIDA-6345-020 OR COILTRONICS-CTX110092-1.
PIN NUMBERS SHOWN FOR COILTRONICS UNIT
L2 = COILTRONICS-CTX300-4
Q1, Q2 = AS SHOWN OR BCP 56 (PHILLIPS SO PACKAGE)
DO NOT SUBSTITUTE COMPONENTS
COILTRONICS (305) 781-8900, SUMIDA (708) 956-0666

Figure 2. Cold Cathode Fluorescent Lamp (CCFL) Power Supply

L1 and the transistors comprise a current driven Royer class converter[2] which oscillates at a frequency primarily set by L1's characteristics (including its load) and the 0.02µF capacitor. LT1172 driven L2 sets the magnitude of the Q1-Q2 tail current, and hence L1's drive level. The 1N5818 diode maintains L2's current flow when the LT1172 is off. The LT1172's 100kHz clock rate is asynchronous with respect to the push-pull converter's (60kHz) rate, accounting for trace B's waveform thickening.

The 0.02µF capacitor combines with L1's characteristics to produce sine wave voltage drive at the Q1 and Q2 collectors (traces C and D respectively). L1 furnishes voltage step-up, and about 1400Vp-p appears at its secondary (trace E). Current flows through the 15pF capacitor into the lamp. On negative waveform cycles the lamp's current is steered to ground via D1. Positive waveform cycles are directed, via D2, to the ground referred 562Ω-50k potentiometer chain. The positive half-sine appearing across these resistors (trace F) represents 1/2 the lamp current. This signal is filtered by the 10k-1µF pair and presented to the LT1172's feedback pin. This connection closes a control loop which regulates lamp current. The 2µF capacitor at the LT1172's V_C pin provides stable loop compensation. The loop forces the LT1172 to switch-mode modulate L2's average current to whatever value is required to maintain a constant current in the lamp. The constant current's value, and hence lamp intensity, may be varied with the potentiometer. The constant current drive allows full 0%-100% intensity control with no lamp dead zones or "pop-on" at low intensities.[3] Additionally, lamp life is enhanced because current cannot increase as the lamp ages.

Several points should be kept in mind when observing this circuit's operation. L1's high voltage secondary can only

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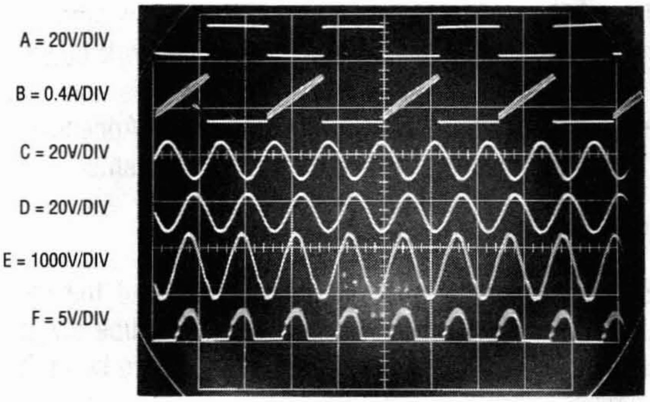
Note 1: Many of the characteristics of CCFLs are shared by so called "Hot" cathode fluorescent lamps. See Appendix A, "Hot" Cathode Fluorescent Lamps.

Note 2: See Reference 3.

Note 3: Controlling a non-linear load's current, instead of its voltage, permits applying this circuit technique to a wide variety of nominally evil loads. See Appendix D, "A Related Circuit."



A AND B HORIZ = 10µs/DIV
C THRU F HORIZ = 20µs/DIV
TRIGGERS FULLY INDEPENDENT

Figure 3. Waveforms for the Cold Cathode Fluorescent Lamp Power Supply. Note Independent Triggering on Traces A and B, and C through F

be monitored with a wideband, high voltage probe fully specified for this type of measurement. *The vast majority of oscilloscope probes will break down and fail if used for this measurement.*[4] Tektronix probe types P-6007 and P-6009 (acceptable) or types P6013A and P6015 (preferred) probes must be used to read L1's output.

Another consideration involves observing waveforms. The LT1172's switching frequency is completely asynchronous from the Q1-Q2 Royer converter's switching. As such, most oscilloscopes cannot simultaneously trigger and display all the circuit's waveforms. Figure 3 was obtained using a dual beam oscilloscope (Tektronix 556). LT1172 related traces A and B are triggered on one beam, while the remaining traces are triggered on the other beam. Single beam instruments with alternate sweep and trigger switching (e.g., Tektronix 547) can also be used, but are less versatile and restricted to four traces.

Obtaining and verifying high efficiency[5] requires some amount of diligence. The optimum efficiency values given for C1 and C2 are typical, and will vary for specific types of lamps. C1 sets the circuit's resonance point, which varies to some extent with the lamp's characteristic. C2 ballasts the lamp, effectively buffering its negative resistance characteristic. Small values of C2 provide the most load isolation, but require relatively large transformer output voltage for loop closure. Large C2 values minimize transformer output voltage, but degrade load buffering. Also, C1's "best" value is somewhat dependent on the type of lamp used. Both C1 and C2 must be selected for given lamp types. Some interaction occurs, but generalized guidelines are possible. Typical values for C1 are 0.01µF to 0.047µF. C2 usually ends up in the 10pF to 47pF range. C1 *must* be a low loss capacitor and substitution of the recommended device is not recommended. A poor quality dielectric for C1 can easily degrade efficiency by 10%. C1 and C2 are selected by trying different values for each and iterating towards minimum input supply current. During this procedure insure that loop closure is maintained by monitoring the LT1172's feedback pin, which should be at 1.23V. Several trials usually produce the optimum C1 and C2 values. Note that the highest efficiencies are not necessarily associated with the most esthetically pleasing waveshapes, particularly at Q1, Q2 and the output.

Other issues influencing efficiency include bulb wire length and energy leakage from the bulb. The high voltage side of the bulb should have the smallest practical lead length. Excessive length results in radiative losses which can easily reach 3% for a 3 inch wire. Similarly, no metal should contact or be in close proximity to the bulb. This prevents energy leakage which can exceed 10%.[6]

These considerations should be made with knowledge of other LCD issues. See Appendix B, "Mechanical Design Considerations for Liquid Crystal Displays." This section was guest written by Charles L. Guthrie of Sharp Electronics Corporation.

Special attention should be given to the layout of the circuit board since high voltage is generated at the output. The

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Note 4: Don't say we didn't warn you!

Note 5: The term "efficiency" as used here applies to *electrical* efficiency. In fact, the ultimate concern centers around the efficient conversion of power supply energy into light. Unfortunately, lamp types show considerable deviation in their current-to-light conversion efficiency. Similarly, the emitted light for a given current varies over the life and history of any particular lamp. As such, this publication treats "efficiency" on an electrical basis; the ratio of power removed from the primary supply to the power delivered to the lamp. When a lamp has been selected the ratio of primary supply power to emitted lamp light energy may be measured with the aid of a photometer.

Note 6: A very simple experiment quite nicely demonstrates the effects of energy leakage. Grasping the bulb at its low voltage end (low field intensity) with thumb and forefinger produces almost no change in circuit input current. Sliding the thumb-forefinger combination towards the high voltage (higher field intensity) bulb end produces progressively greater input currents. Don't touch the high voltage lead or you may receive an electrical shock. Repeat: Do not touch the high voltage lead or you may receive an electrical shock.

output coupling capacitor must be carefully located to minimize leakage paths on the circuit board. A slot in the board will further minimize leakage. Such leakage can permit current flow outside the feedback loop, wasting power. In the worst case, long term contamination build-up can increase leakage inside the loop, resulting in starved lamp drive or destructive arcing. It is good practice for minimization of leakage to break the silk screen line which outlines transformer T1. This prevents leakage from the high voltage secondary to the primary. Another technique for minimizing leakage is to evaluate and specify the silk screen ink for its ability to withstand high voltages.

Once these procedures have been followed efficiency can be measured. Efficiency may be measured by determining bulb current and voltage. Measuring current involves measuring RMS voltage across the 562Ω resistor (short the potentiometer). The bulb current is:

$$I_{BULB} = \left(\frac{E}{R}\right) \times 2$$

The X2 factor is necessitated because the diode steering dumps the current to ground on negative cycles. The shunting effects of the 10K-1μF RC across the 562Ω resistor introduce a small current measurement error. Because of this, best accuracy is obtained by measuring across a temporarily inserted 562Ω 1% unit in the ground lead of the negative current steering diode. Once this measurement is complete this second 562Ω resistor may be deleted and the negative current steering diode again returned directly to ground. Bulb RMS voltage is measured at the bulb with a properly compensated high voltage probe. Multiplying these two results gives power in watts, which may be compared to the DC input supply E x I product. In practice, the lamp's current and voltage contain small out of phase components but their error contribution is negligible.

Both the current and voltage measurements require a wideband True RMS voltmeter. The meter must employ a thermal type RMS converter—the more common logarithmic computing type based instruments are inappropriate because their bandwidth is too low.

The previously recommended high voltage probes are designed to see a 1MΩ-10pF-22pF oscilloscope input. The RMS voltmeters have a 10MΩ input. This difference necessitates an impedance matching network between the probe and the voltmeter. Details on this and other efficiency measurement issues appear in Appendix C, "Achieving Meaningful Efficiency Measurements."

Two Tube Designs

Some displays require two tubes instead of the more popular single tube approach. These two tube designs usually require more power. Accommodating two tubes involves separate ballast capacitors (see Figure 4), but circuit operation is similar. Higher power may require a different transformer rating. Figure 2's transformer can supply 7.5mA, although more current is possible with appropriate transformer types. For reference, an 11mA capability transformer appears in Figure 4.

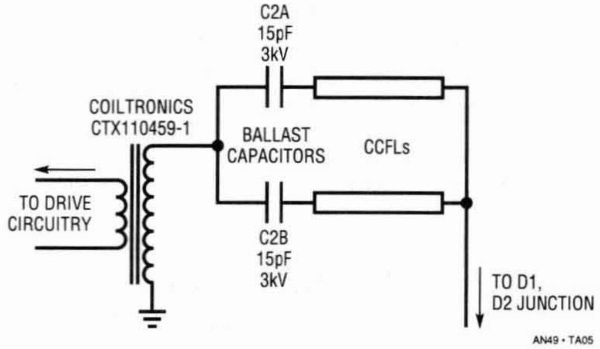


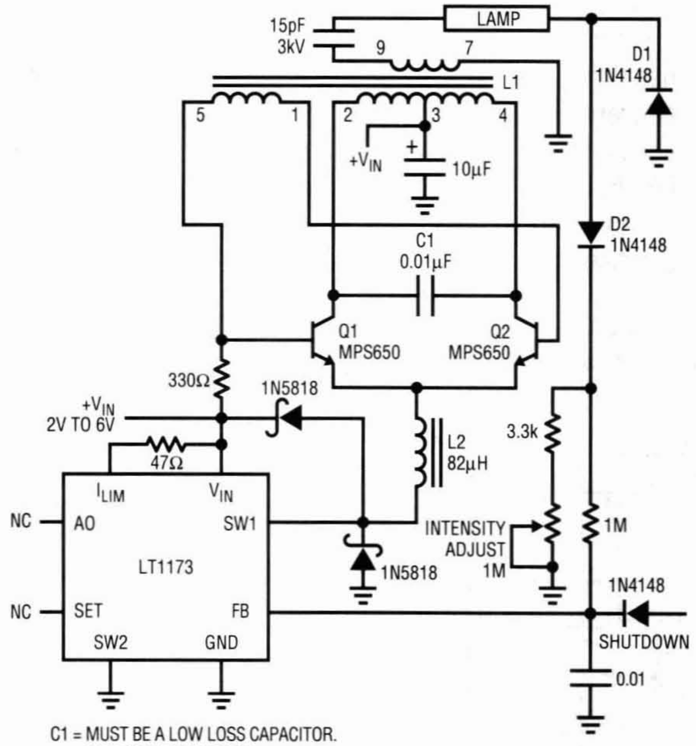
Figure 4. Driving Two Tubes. Capacitors Provide Ballast, Isolating the Tubes

The two tube designs reflect slightly different loading back through the transformer's primary. C2 usually ends up in the 10pF to 47pF range. Note that C2A and B appear with their lamp loads in parallel across the transformer's secondary. As such C2's value is often smaller than in a single tube circuit using the same type lamp. Ideally, the transformer's secondary current splits evenly between the C2-lamp branches, with the total load current being regulated. In practice, differences between C2A and B and differences in lamp wiring layout preclude a perfect current split. Practically, these differences are small, and the lamps appear to emit equal amounts of light.

Low Power CCFL Supply

Figure 5 is the other extreme. This design, the so-called "dim backlight," is optimized for single tube operation at very low currents. The circuit is meant for use at low input voltages, typically 2V to 6V. Figure 2's circuit drives 5mA maximum, but this design tops out at 1mA. This circuit maintains control down to tube currents of 1μA, a very dim light! It is intended for applications where the longest possible battery life is desired. Primary supply drain ranges from hundreds of microamperes to 100mA with tube currents of microamps to 1mA. In shutdown the circuit pulls only 110μA. Maintaining high efficiency at low tube currents requires modifying the basic design.

Achieving high efficiency at low operating current requires lowering Figure 2's quiescent power drain. To do this the LT1172, a pulse width modulator based device, is replaced with an LT1173. The LT1173 is a "burst mode" type regulator. When this device's feedback pin is too low it delivers a burst of output current pulses, putting energy into the transformer and restoring the feedback point. The regulator maintains control by appropriately modulating the burst duty cycle. The ground referred diode at the V_{SW} pin prevents substrate turn-on due to excessive L2 ring-off.



C1 = MUST BE A LOW LOSS CAPACITOR.
METALIZED POLYCARB
WIMA FKP2 (GERMAN) RECOMMENDED.
L1 = SUMIDA-6345-020 OR COILTRONICS-CTX110092-1.
PIN NUMBERS SHOWN FOR COILTRONICS UNIT
L2 = TOKO 262LYF-0091K
(408) 432-8251
DO NOT SUBSTITUTE COMPONENTS

Figure 5. Low Power CCFL Power Supply. Circuit Controls Lamp Current over a 1μA to 1mA Range

During the off periods the regulator is essentially shut down. This type of operation limits available output power, but cuts quiescent current losses. In contrast, Figure 2's LT1172 pulse width modulator type regulator maintains "housekeeping" current between cycles. This results in more available output power but higher quiescent currents.

Figure 6 shows operating waveforms. When the regulator comes on (trace A, Figure 6) it delivers bursts of output current to the L1-Q1-Q2 high voltage converter. The converter responds with bursts of ringing at its resonant frequency. The circuit's loop operation is similar to Figure 2.[7]

Some bulbs may display non-uniform light emission at very low excitation currents. See Appendix F, "The Thermometer Effect."

LCD Bias Supplies

LCD's also require a bias supply for contrast control. The supply's variable negative output permits adjustment of display contrast. Relatively little power is involved, easing RF radiation and efficiency requirements. The logic sections of display drivers operate from single 5V supplies, but the actual driver outputs swing between +5V and a negative bias potential. Varying this bias causes the contrast of the display to vary.

An LCD bias generator, developed by Steve Pietkiewicz of LTC, is shown in Figure 7. In this circuit U1 is an LT1173 micropower DC to DC converter. The 3V input is converted to +24V by U1's switch, L2, D1, and C1. The switch pin (SW1) also drives a charge pump composed of C2, C3, D2, and D3 to generate –24V. Line regulation is less than 0.2%

Note 7: The discontinuous energy delivery to the loop causes substantial jitter in the burst repetition rate, although the high voltage section maintains resonance. Unfortunately, circuit operation is in the "chop" mode region of most oscilloscopes, precluding a detailed display. "Alternate" mode operation causes waveform phasing errors, producing an inaccurate display. As such, waveform observation requires special techniques. Figure 6 was taken with a dual beam instrument (Tektronix 556) with both beams slaved to one time base. Single sweep triggering eliminated jitter artifacts. Most oscilloscopes, whether analog or digital, will have trouble reproducing this display.

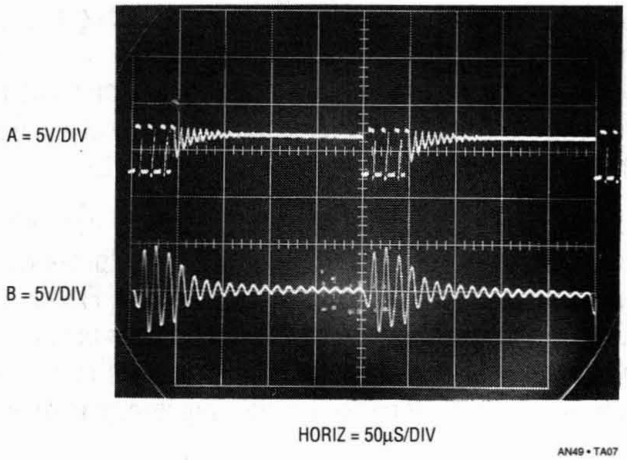
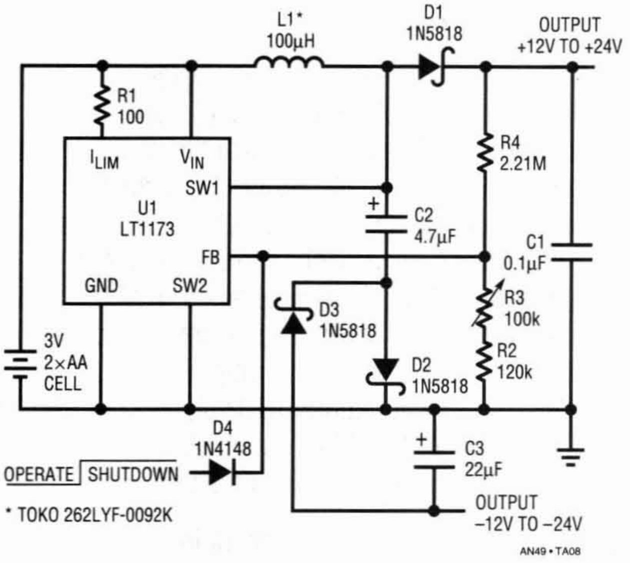


Figure 6. Waveforms for the Low Power CCFL Power Supply. LT1173 Burst Type Regulator (Trace A) Periodically Excites the Resonant High Voltage Converter (Q1 Collector is Trace B)

from 3.3V to 2V inputs. Load regulation, although suffering somewhat since the –24V output is not directly regulated, measures 2% from a 1mA to 7mA load. The circuit will deliver 7mA from a 2V input at 75% efficiency.

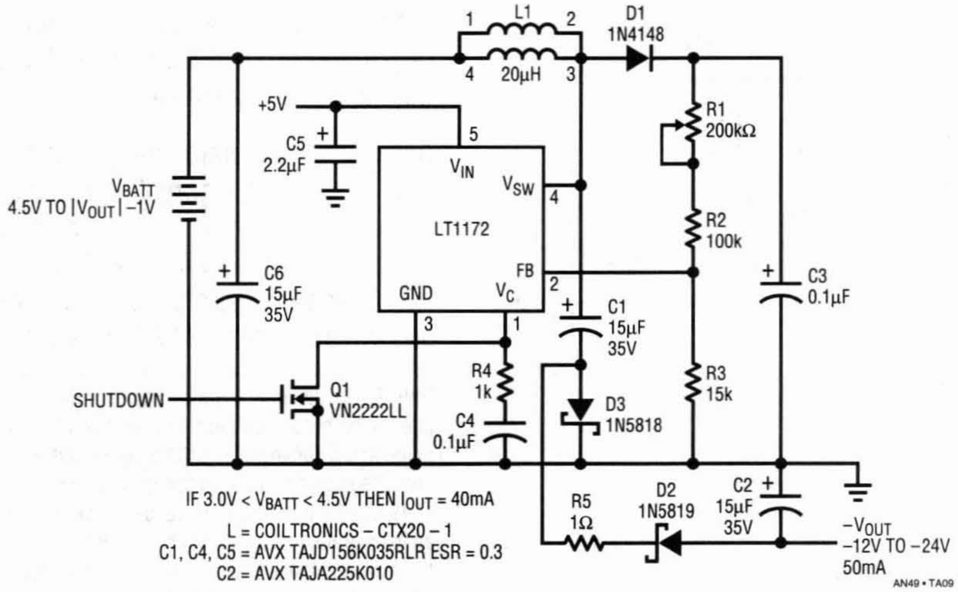
If greater output power is required, Figure 7's circuit can be driven from a +5V source. R1 should be changed to 47Ω and C3 to 47µF. With a 5V input, 40mA are available at 75% efficiency. Shutdown is accomplished by bringing the anode of D4 to a logic high, forcing the feedback pin of U1 to go above the internal 1.25V reference voltage. Shutdown current is 110µA from the input source and 36µA from the shutdown signal.


L1*
100µH
D1
1N5818
OUTPUT
+12V TO +24V
R1
100
I_LIM
V_IN
SW1
U1
LT1173
FB
GND
SW2
R4
2.21M
C2
4.7µF
C1
0.1µF
R3
100k
D3
1N5818
R2
120k
3V
2×AA
CELL
D2
1N5818
D4
1N4148
C3
22µF
OPERATE | SHUTDOWN
OUTPUT
–12V TO –24V
AN49 • TA08

* TOKO 262LYF-0092K

Figure 7. DC to DC Converter Generates LCD Bias

A similar modification of a boost converter can provide negative bias from a 5V supply is shown in Figure 8. The converter, developed by Jon Dutra of LTC, is half switcher and half charge pump. The charge pump (C1, C2, D2, and D3) is driven by the flying node at V_{SW}. The output is variable from –12V to –24V, providing contrast control for the display.


L1
1
2
4
20µH
3
D1
1N4148
+5V
C5
2.2µF
5
V_IN
V_SW
4
LT1172
FB
2
GND
V_C
3
1
R1
200kΩ
R2
100k
V_BATT
4.5V TO |V_OUT| –1V
C6
15µF
35V
C1
15µF
35V
C3
0.1µF
R4
1k
C4
0.1µF
Q1
VN2222LL
SHUTDOWN
D3
1N5818
R3
15k
R5
1Ω
D2
1N5819
C2
15µF
35V
–V_OUT
–12V TO –24V
50mA
AN49 • TA09

IF 3.0V < V_{BATT} < 4.5V THEN I_{OUT} = 40mA

L = COILTRONICS – CTX20 – 1
C1, C4, C5 = AVX TAJD156K035RLR ESR = 0.3
C2 = AVX TAJA225K010

Figure 8. The Dutra Configuration Combines Switching Regulator and Charge Pump Techniques to Generate Negative Bias for LCD Drivers

On low voltage supplies (6V or less) V_{IN} and V_{BATT} can be tied together. With higher battery voltages, high efficiency is obtained by running the LT1172 V_{IN} pin from 5V. Shutting off the 5V supply automatically turns off the LT1172. The maximum value for V_{BATT} is equal to the negative output +1V. Also, the difference between V_{BATT} and V_{IN} must not exceed 16V. R1, R2, and R3 are made large to minimize battery drain in shutdown, since they are permanently connected to the battery via L1 and D1. Efficiency is about 80% at I_{OUT} = 25mA.

Note: *This application note was derived from a manuscript originally prepared for publication in EDN Magazine.*

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APPENDIX A

"HOT" CATHODE FLUORESCENT LAMPS

Many CCFL characteristics are shared by so-called "Hot" Cathode Fluorescent Lamps (HCFLs). The most significant difference is that HCFLs contain filaments at each end of the tube (see Figure A1). When the filaments are powered they emit electrons, lowering the tube's ionization potential. This means a significantly lower voltage will start the tube. Typically the filaments are turned on, a relatively modest high voltage impressed across the tube, and start-up occurs. Once the tube starts filament power is removed. Although HCFLs reduce the high voltage requirement they require a filament supply and sequencing circuitry. The CCFL circuits shown in the text will start and run HCFLs without using the filaments. In practice this involves simply driving the filament connections at the HCFL tube ends as if they were CCFL electrodes.

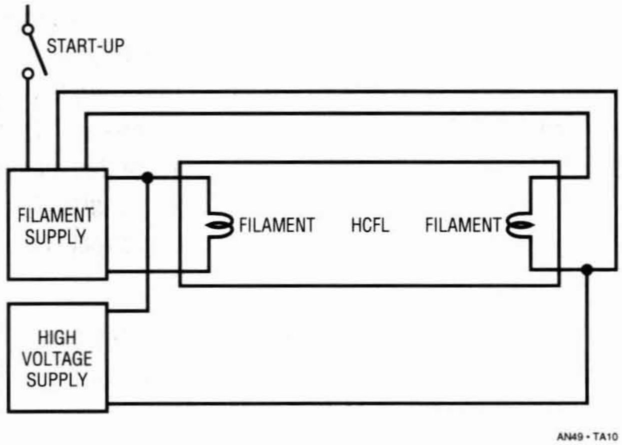

Figure A1. A Conceptual Hot Cathode Fluorescent Lamp Power Supply. Heated Filaments Liberate Electrons, Lowering the Tube's Start-Up Voltage Requirement. CCFL Supply Discussed in Text Eliminates Filament Supply

APPENDIX B

MECHANICAL DESIGN CONSIDERATIONS FOR LIQUID CRYSTAL DISPLAYS

Charles L. Guthrie, Sharp Electronics Corporation

Introduction

As more companies begin the manufacturing of their next generation of computers, there is a need to reduce the overall size and weight of the units to improve their portability. This has sparked the need for more compact designs where the various components are placed in closer proximity, thus making them more susceptible to interaction from signal noise and heat dissipation. The following is a summary of guidelines for the placement of the display components, and a summary of suggestions for overcoming difficult design constraints associated with component placement.

In notebook computers, the thickness of the display housing is important. The design usually requires the display to be in a pivotal structure so that the display may be folded down over the keyboard for transportation. Also, the outline dimensions must be minimal so that the package will remain as compact as possible. These two constraints drive the display housing design and placement of the display components. This discussion surveys each of the problems facing the designer in detail and offers suggestions for overcoming the difficulties to provide a reliable assembly.

The problems facing the pen based computer designer are similar to those realized in notebook designs. In addition, however, pen based designs require protection for the face of the display. In pen based applications, as the pen is moved across the surface of the display, the pen has the potential for scratching the front polarizer. For this reason, the front of the display must be protected. Methods for protecting the display face while minimizing effects on the display image are given.

Additionally, the need to specify the flatness of the bezel is discussed. Suggestions for acceptable construction techniques for sound design are included. Further, display components likely to cause problems due to heat buildup are identified and methods for minimization of the heat's effects are presented.

The ideas expressed here are not the only solutions to the various problems, and have not been assessed as to whether they may infringe on any patents issued or applied for.

Flatness and Rigidity of the Bezel

In the notebook computer, the bezel has several distinct functions. It houses the display, the inverter for the backlight, and in some instances, the controls for contrast and brightness of the display. The bezel is usually designed to tilt to set the optimum viewing angle for the display.

It is important to understand that the bezel must provide a mechanism to keep the display flat, particularly at the mounting holds. Subtle changes in flatness place uneven stress on the glass which can cause variations in contrast across the display. Slight changes in pressure may cause significant variation in the display contrast. Also, at the extreme, significantly uneven pressures can cause the display glass to fail.

Because the bezel must be functional in maintaining the flatness of the display, consideration must be made for the strength of the bezel. Care must be taken to provide structural members, while minimizing the weight of the unit. This may be executed using a parallel grid, normal to the edges of the bezel, or angled about 45° off of the edges of the bezel. The angled structure may be more desirable in that it provides resistance to torquing the unit while lifting the cover with one hand. Again, the display is sensitive to stresses from uneven pressure on the display housing.

Another structure which will provide excellent rigidity, but adds more weight to the computer, is a "honeycomb" structure. This "honeycomb" structure resists torquing from all directions and tends to provide the best protection for the display.

With each of these structures it is easy to provide mounting assemblies for the display. "Blind nuts" can be molded into the housing. The mounting may be done to either the front or rear of the bezel. Attachment to the rear may provide better rigidity for placement of the mounting hardware.

One last caution is worth noting in the development of a bezel. The bezel should be engineered to absorb most of the shock and vibration experienced in a portable computer. Even though the display has been carefully designed, the notebook computer presents extraordinary shock and abuse problems.

Avoiding Heat Buildup in the Display

Several of the display components are sources for heat problems. Thermal management must be taken into account in the design of the display bezel. A heated display may be adversely affected; a loss of contrast uniformity usually results. The Cold Cathode Fluorescent Tube (CCFT) itself gives off a small amount of heat relative to the amount of current dissipated in its glow discharge. Likewise, even though the inverters are designed to be extremely efficient, there is some heat generated. The buildup of heat in these components will be aggravated by the typically "tight" designs currently being introduced. There is little ventilation designed into most display bezels. To compound the problem, the plastics used are poor thermal conductors, thus causing the heat to build up which may affect the display.

Some current designs suffer from poor placement of the inverter and/or poor thermal management techniques. These designs can be improved, even where redesign of the display housing, with improved thermal management, is impractical.

One of the most common mistakes in current designs is that there has been no consideration for the build up of heat from the CCFT. Typically, the displays for notebook applications have only one CCFT to minimize display power requirements. This lamp is usually placed along the right edge of the display. Since the lamp is placed very close to the display glass, it can cause a temperature rise in the liquid crystal. It is important to note that variations in temperature of as little as 5°C can cause an apparent non-uniformity in display contrast. Variations caused by slightly higher temperature variations will cause objectionable variations in the contrast and display appearance. To further aggravate the situation, some designs have the inverter placed in the bottom of the bezel. This has a tendency to cause the same variations in contrast, particularly when the housing does not have any heat sinking for the inverter. This problem manifests itself as a "blooming" of the display, just above the inverter. This "blooming" looks like a washed out area where, in the worst case, the characters on the display fade completely.

The following section discusses the recommended methods for overcoming these design problems.

Placement of the Display Components

One of the things that can be done is to design the inverter into the base of the computer with the mother board. In some applications this is impractical because this requires the high voltage leads to be mounted within the hinges connecting the display bezel to the main body. This causes a problem with strain relief of the high voltage leads, and thus with U.L. Certification.

One mistake, made most often, is placing the inverter at the bottom on the bezel next to the lower edge of the display. It is a fact that heat rises, yet this is one of the most overlooked problems in new notebook designs. Even though the inverters are very efficient, some energy is lost in the inverter in the form of heat. Because of the insulating properties of the plastic materials used in the bezel construction, heat builds up and affects the display contrast.

Designs with the inverter at the bottom can be improved in one of three ways. The inverter can be relocated away from the display; heat sinking materials can be placed between the display and the inverter; or ventilation can be provided to remove the heat.

In mature designs, it may be impractical to do what is obvious and move the inverter up to the side of the display towards the top of the housing. In these cases, the inverter may be insulated from the display with a "heat dam". One method of accomplishing this would be to use a piece of mica insulator die cut to fit tightly between the inverter and the display. This heat dam would divert the heat around the end of the display bezel to rise harmlessly to the top of the housing. Mica is recommended in this application because of its thermal and electrical insulating properties.

The last suggestion for removing heat is to provide some ventilation to the inverter area. This has to be done very carefully to prevent exposing the high voltage. Ventilation may not be a practical solution because resistance to liquids and dust is compromised.

The best solution for the designer of new hardware is to consider the placement of the inverter to the side of the display and at the top of the bezel. In existing designs of this type the effects of heat from the inverter, even in tight housings, has been minimal or non-existent.

One problem which is aggravated by the placement of the inverter at the bezel is heat dissipated by the CCFT. In designs were the inverter is placed up and to the side of the display, fading of the display contrast due to CCFT heat is not a problem. However, when the inverter is placed at the bezel bottom, some designs experience a loss of contrast aggravated by the heat from the CCFT and inverter.

In cases where the inverter must be left at the bottom, and the CCFT is causing a loss of contrast, the problem can be minimized by using an aluminum foil heat sink. This does not remove the heat from the display, but dissipates it over the entire display area, thus normalizing the display contrast. The aluminum foil is easy to install and in some present designs has successfully improved the display contrast.

Remember that the objection to the contrast variation stems more from non-uniformity than from a total loss of contrast.

Protecting the Face of the Display

One of the last considerations in the design of notebook and pen based computers is protection of the display face. The front polarizer is made of a mylar base and thus is susceptible to scratching. The front protection for the display, along with providing scratch protection, may also provide an anti-glare surface.

There are several ways that scratch resistance and anti-glare surfaces can be incorporated. A glass or plastic cover may be placed over the display, thus providing protection. The material should be placed as close to the display as possible to minimize possible parallax problems due to reflections off of the cover material. With anti-glare materials, the further the material is from the front of the display the greater the distortion.

In pen applications, the front anti-scratch material is best placed in contact with the front glass of the display. The cover glass material normally needs to be slightly thicker to protect the display from distortion when pressure is being exerted on the front.

There are several methods for making the pen input devices. Some use the front surface of the cover glass to provide input data and some use a field effect to a printed wiring board on the back of the display. When the pen input is on the front of the display, the input device is usually on a glass surface.

To limit specular reflection in this application, the front cover glass should be bonded to the display. Care must be taken to insure that the coefficient of thermal expansion is matched for all of the materials used in the system. Because of the difficulties encountered with the bonding of the cover glass, and the potential to destroy the display through improper workmanship, consulting an expert is strongly recommended.

APPENDIX C

ACHIEVING MEANINGFUL EFFICIENCY MEASUREMENTS

Efficiency measurement is difficult. The most important points for getting good efficiency measurements are:

- Use proper equipment.
- Measure carefully.
- Measure with the CCFL you intend to use. Simple resistive loads or substitute lamps can cause 5-10% errors.
- Measure with the circuit components and layout you intend to use.

Obtaining reliable efficiency data for the CCFL circuits requires attention to measurement technique. The combination of high frequency, harmonic laden waveforms and high voltage makes meaningful results difficult to obtain.

The choice, understanding and use of test instrumentation is crucial. Clear thinking is needed to avoid unpleasant surprises![1]

Probes

The probes employed must faithfully respond over a variety of conditions. Measuring across the resistor in series with the CCFL is the most favorable circumstance. This low voltage, low impedance measurement allows use of a standard 1X probe. The probe's relatively high input capacitance does not introduce significant error. A 10X probe may also be used, but frequency compensation issues (discussion to follow) must be attended to.

The high voltage measurement across the lamp is considerably more demanding on the probe. The waveform fundamental is at 20kHz to 100kHz, with harmonics into the MHz region. This activity occurs at peak voltages in the kilovolt range. The probe must have a high fidelity response under these conditions. Additionally, the probe should have low input capacitance to avoid loading effects which would corrupt the measurement. The design and construction of such a probe requires significant attention. Figure C1 lists some recommended probes along with their characteristics. As stated in the text, almost all standard oscilloscope probes *will fail*[2] if used for this measurement. Attempting to circumvent the probe requirement by resistively voltage dividing the lamp voltage also creates problems. Large value resistors often have significant voltage coefficients and their shunt capacitance is high and uncertain. As such, simple voltage dividing is not recommended. Similarly, common high voltage probes intended for DC measurement will have large errors because of AC effects. The P6013A and P6015 are the favored probes; their 100MΩ input and small capacitance introduces low loading error. The penalty for their 1000X attenuation is reduced output, but the recommended voltmeters (discussion to follow) can accommodate this.

All of the recommended probes are designed to work into an oscilloscope input. Such inputs are almost always 1MΩ paralleled by (typically) 10pF-22pF. The recommended voltmeters, which will be discussed, have significantly different input characteristics. Figure C2's table shows higher input resistances and a range of capacitances. Because of this the probe must be compensated for the

TEKTRONIX PROBE TYPE	ATTENUATION FACTOR	ACCURACY	INPUT RESISTANCE	INPUT CAPACITANCE	RISE TIME	BAND-WIDTH	MAXIMUM VOLTAGE	DERATED ABOVE	DERATED TO AT FREQUENCY	COMPENSATION RANGE	ASSUMED TERMINATION RESISTANCE
P6007	100X	3%	10MΩ	2.2pF	14ns	25MHz	1.5kV	200kHz	$700V_{RMS}$ at 10MHz	15-55pF	1M
P6009	100X	3%	10MΩ	2.5pF	2.9ns	120MHz	1.5kV	200kHz	$450V_{RMS}$ at 40MHz	15-47pF	1M
P6013A	1000X	Adjustable	100MΩ	3pF	7ns	50MHz	12kV	100kHz	$800V_{RMS}$ at 20MHz	12-60pF	1M
P6015	1000X	Adjustable	100MΩ	3pF	1.4ns	250MHz	20kV	100kHz	$2000V_{RMS}$ at 20MHz	12-47pF	1M

Figure C1. Characteristics of Some Wideband High Voltage Probes. Output Impedances are Designed for Oscilloscope Inputs

MANUFACTURER AND MODEL	FULL SCALE RANGES	ACCURACY AT 1MHz	ACCURACY AT 100kHz	INPUT RESISTANCE AND CAPACITANCE	MAXIMUM BANDWIDTH	CREST FACTOR
Hewlett-Packard 3400 Meter Display	1mV to 300V, 12 Ranges	1%	1%	0.001V to 0.3V Range = 10M and < 50pF, 1V to 300V Range = 10M and < 20pF	10MHz	10:1 At Full Scale, 100:1 At 0.1 Scale
Hewlett-Packard 3403C Digital Display	10mV to 1000V, 6 Ranges	0.5%	0.2%	10mV and 100mV Range = 20M and 20pF ±10%, 1V to 1000V Range = 10M and 24pF ±10%	100MHz	10:1 At Full Scale, 100:1 At 0.1 Scale
Fluke 8920A Digital Display	2mV to 700V, 7 Ranges	0.7%	0.5%	10M and < 30pF	20MHz	7:1 At Full Scale, 70:1 At 0.1 Scale

Figure C2. Pertinent Characteristics of Some Thermally Based RMS Voltmeters. Input Impedances Necessitate Matching Network and Compensation for High Voltage Probes

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[1] **Note 1:** It is worth considering that various constructors of text Figure 2 have reported efficiencies ranging from 8% to 115%.

[2] **Note 2:** That's twice we've warned you nicely.

voltmeter's input characteristics. Normally, the optimum compensation point is easily determined and adjusted by observing probe output on an oscilloscope. A known amplitude square wave is fed in (usually from the oscilloscope calibrator) and the probe adjusted for correct response. Using the probe with the voltmeter presents an unknown impedance mismatch and raises the problem of determining when compensation is correct.

The impedance mismatch occurs at low and high frequency. The low frequency term is corrected by placing an appropriate value resistor in shunt with the probe's output. For a 10MΩ voltmeter input a 1.1MΩ resistor is suitable. This resistor should be built into the smallest possible BNC equipped enclosure to maintain a coaxial environment. No cable connections should be employed; the enclosure should be placed *directly* between the probe output and the voltmeter input to minimize stray capacitance. This arrangement compensates the low frequency impedance mismatch.

Correcting the high frequency mismatch term is more involved. The wide range of voltmeter input capacitances combined with the added shunt resistor's effects presents problems. How is the experimenter to know where to set the high frequency probe compensation adjustment? One solution is to feed a known value RMS signal to the probe-voltmeter combination and adjust compensation for a proper reading. Figure C3 shows a simple way to generate a known RMS voltage. This scheme takes advantage of the recommended voltmeter's insensitivity to waveform shape. The CMOS flip-flop is driven from a stable 10.00V source.

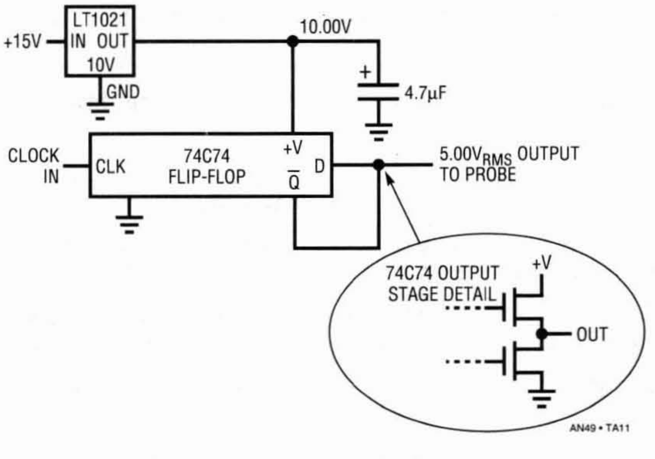

Figure C3. The RMS Calibrator. MOSFET Output Stage Detail Shows Purely Ohmic Switching to Power Rails

The CMOS output stage, which is purely ohmic, produces essentially errorless switching between the power supply rails. Clocking the flip-flop produces a square wave output with a 10.00V amplitude. The result is a known $5.00V_{RMS}$ output. Now, the probe's compensation is adjusted for a 5.00V voltmeter reading. This procedure, combined with the added resistor, completes the probe-to-voltmeter impedance match. If the probe compensation is altered (e.g., for proper response on an oscilloscope) the voltmeter's reading will be erroneous.[3]

RMS Voltmeters

The efficiency measurements require an RMS responding voltmeter. This instrument must respond accurately at high frequency to irregular and harmonically loaded waveforms. These considerations eliminate almost all AC voltmeters, including DVMs with AC ranges.

There are a number of ways to measure RMS AC voltage. Three of the most common include *average, logarithmic,* and *thermally* responding. Averaging instruments are calibrated to respond to the average value of the input waveform, which is almost always assumed to be a sine wave. Deviation from an ideal sine wave input produces errors. Logarithmically based voltmeters attempt to overcome this limitation by continuously computing the input's true RMS value. Although these instruments are "real time" analog computers their 1% error bandwidth is well below 300kHz and crest factor capability is limited. Almost all general purpose DVMs use such a logarithmically based approach and, as such, are not suitable for CCFL efficiency measurements. Thermally based RMS voltmeters are direct acting thermo-electronic analog computers. They respond to the input's RMS heating value. This technique is explicit, relying on the very definition of RMS (e.g., the heating power of the waveform). By turning the input into heat, thermally based instruments achieve vastly higher bandwidth than other techniques.[4] Additionally, they are insensitive to waveform shape and easily

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Note 3: The translation of this statement is to hide the probe when you are not using it. If anyone wants to borrow it, look straight at them, shrug your shoulders, and say you don't know where it is. This is decidedly dishonest, but eminently practical. Those finding this morally questionable may wish to re-examine their attitude after producing a days worth of worthless data with a probe that was unknowingly readjusted.

Note 4: Those finding these descriptions intolerably brief are commended to References 5, 6 and 7.

accommodate large crest factors. These characteristics are necessary for the CCFL efficiency measurements.

Figure C4 shows a conceptual thermal RMS-DC converter. The input waveform warms a heater, resulting in increased output from its associated temperature sensor. A DC amplifier forces a second, identical, heater-sensor pair to the same thermal conditions as the input driven pair. This differentially sensed, feedback enforced loop makes ambient temperature shifts a common mode term, eliminating their effect. Also, although the voltage and thermal interaction is non-linear, the input-output RMS voltage relationship is linear with unity gain.

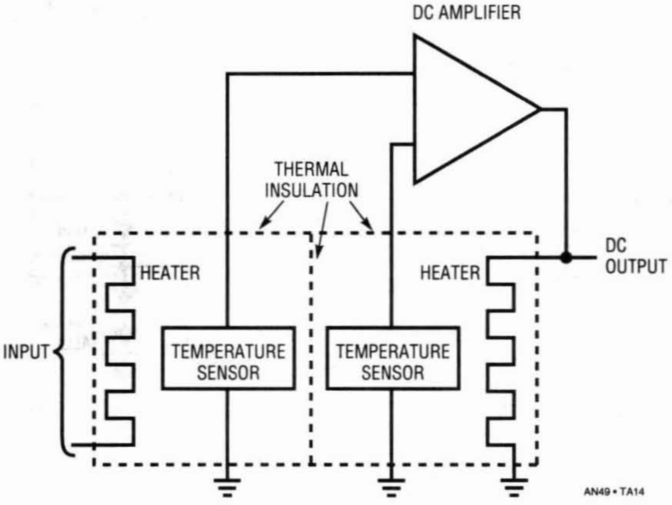


Figure C4. Conceptual Thermal RMS-DC Converter

The ability of this arrangement to reject ambient temperature shifts depends on the heater-sensor pairs being isothermal. This is achievable by thermally insulating them with a time constant well below that of ambient shifts. If the time constants to the heater-sensor pairs are matched, ambient temperature terms will affect the pairs equally in phase and amplitude. The DC amplifier will reject this common mode term. Note that, although the pairs are isothermal, they are insulated from each other. Any thermal interaction between the pairs reduces the system's thermally based gain terms. This would cause unfavorable signal-to-noise performance, limiting dynamic operating range.

Figure C4's output is linear because the matched thermal pair's non-linear voltage-temperature relationships cancel each other.

The advantages of this approach have made its use popular in thermally based RMS-DC measurements.

The instruments listed in Figure C2, while considerably more expensive than other options, are typical of what is required for meaningful results. The HP3400A and the Fluke 8920A are currently available from their manufacturers. The HP3403C, an exotic and highly desirable instrument, is no longer produced but readily available on the secondary market.

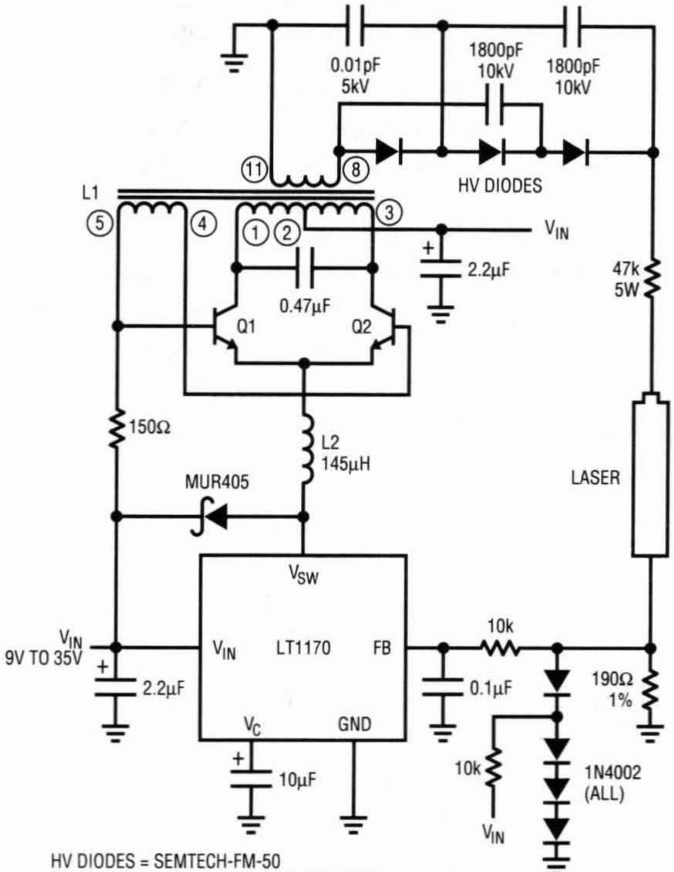
APPENDIX D

A RELATED CIRCUIT

The high voltage compliance current loop approach of the CCFL power supply suits other applications. The current sensing permits precise high efficiency control of a wide variety of difficult loads. A HeNe Laser represents such a load. Lasers are negative impedances operating at very high voltages. Typically, they require 6kV-10kV to start, with an operating voltage in the 1kV-3kV region. Best optical characteristics are achieved by controlling the current through the laser. Simple high voltage drive does not provide this. Figure D1 adapts the CCFL circuitry to control a laser. Both tube current stability and electrical efficiency are improved over the more conventional voltage mode drive.

The start-up and sustaining functions have been combined into a single closed loop current source with over 10kV of compliance. When power is applied, the Laser does not conduct and the voltage across the 190Ω resistor is zero. The LT1170 switching regulator FB pin sees no feedback voltage, and its switch pin (V_{SW}) provides full duty cycle pulse width modulation to L2. Current flows from L1's center tap through Q1 and Q2 into L2 and the LT1170. This current flow causes Q1 and Q2 to switch, alternately driving L1. The 0.48μF capacitor resonates with L1, providing boosted, sine wave drive. L2 provides substantial step-up, causing about 3500V to appear at its secondary. The capacitors and diodes associated with L2's secondary form a voltage tripler, producing over 10kV across the Laser. The Laser breaks down and current begins to flow through it. The 47kΩ resistor ballasts the Laser, limiting current. The current flow causes a voltage to appear across the 190Ω resistor. A filtered version of this voltage appears at the LT1170 FB pin, closing a control loop. The LT1170 adjusts its pulse width drive to L2 to maintain the FB pin at 1.23V regardless of changes in operating conditions. In this fashion the Laser sees constant current drive, in this case 6.5mA. Other currents are obtainable by varying the 190Ω value. The 1N4002 diode string clamps excessive voltages when Laser conduction first begins, protecting the LT1170. The 10µF capacitor at the V_C pin frequency compensates the loop and the MUR405 maintains L1's current flow when the LT1170 V_{SW} pin is not conducting.

The circuit will start and run the Laser over a 9V – 35V input range with an electrical efficiency of about 75%.



HV DIODES = SEMTECH-FM-50
0.47µF = WIMA 3X 0.15µF TYPE MKP-20
Q1, Q2 = ZETEX ZTX-849
L1 = COILTRONICS CTX0211128-2
L2 = PULSE ENGINEERING PE-92105
LASER = HUGHES 3121H-P

AN49 • TA12

Figure D1. ***Laser*** **Power Supply is Essentially a 10kV Compliance Current Source**

APPENDIX E

BACKLIGHT CHARACTERISTICS

DISPLAY TYPE	RUN VOLTAGE	START VOLTAGE	DISCHARGE CURRENT IN mA	BRIGHTNESS IN nt	POWER CONSUMPTION IN WATTS
CXA-M10M	480 ± 80	1200 MIN	4-6	5000 TYP	2.4
EMI-1231	355 ± 60	1200 TYP	5 ± 1	10,000	1.8
LM000105	340 ± 60	1200 MIN	5 ± 1	5000 MIN	1.7
CXA-1301	335 ± 25	1000 TYP	5 ± 1	2300 MIN	1.7
CXA-M10M	300 ± 30	1300 MIN	5.3 TYP	8000 MIN	1.8
CSA-0113	290 ± 60	1000 TYP	3.0	4500	.87
EHI-1231	280 TYP	1100 MIN	3.5-7	10,000 TYP	2

Figure E1. Characteristics of Some Sharp Corporation LCD Backlights

APPENDIX F

THE THERMOMETER EFFECT

Bulbs operating at very low currents may display the "thermometer effect"; that is, light intensity may be nonuniformly distributed along the bulbs length. Although bulb current density is uniform, the associated electromagnetic field is not. The field's low intensity, combined with its gradient, means that there is not enough energy to maintain uniform phosphor glow beyond some point.

Bulbs displaying the thermometer effect emit most of their light near the high voltage electrode, with rapid emission fall-off as distance from the electrode increases. Placing a conductor along the bulb's length largely alleviates "thermometering." The trade-off is decreased efficiency due to energy leakage (see footnote 6 and associated text). It is worth noting that various bulb types have different degrees of susceptibility to the thermometer effect.

APPENDIX G

OPERATION FROM HIGH VOLTAGE INPUTS

Some applications require higher input voltages. The 20V maximum input specified in Figures 2 and 4 is set by the LT1172 going into its isolated flyback mode (see LT1072 and LT1172 data sheets), not breakdown limits. If the LT1172 is driven from a low voltage source (e.g., 5V) the 20V limit may be extended by using Figure G1's network. If the LT1172 is driven from the same supply as L1's center tap the network is unnecessary.

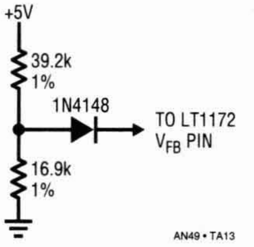
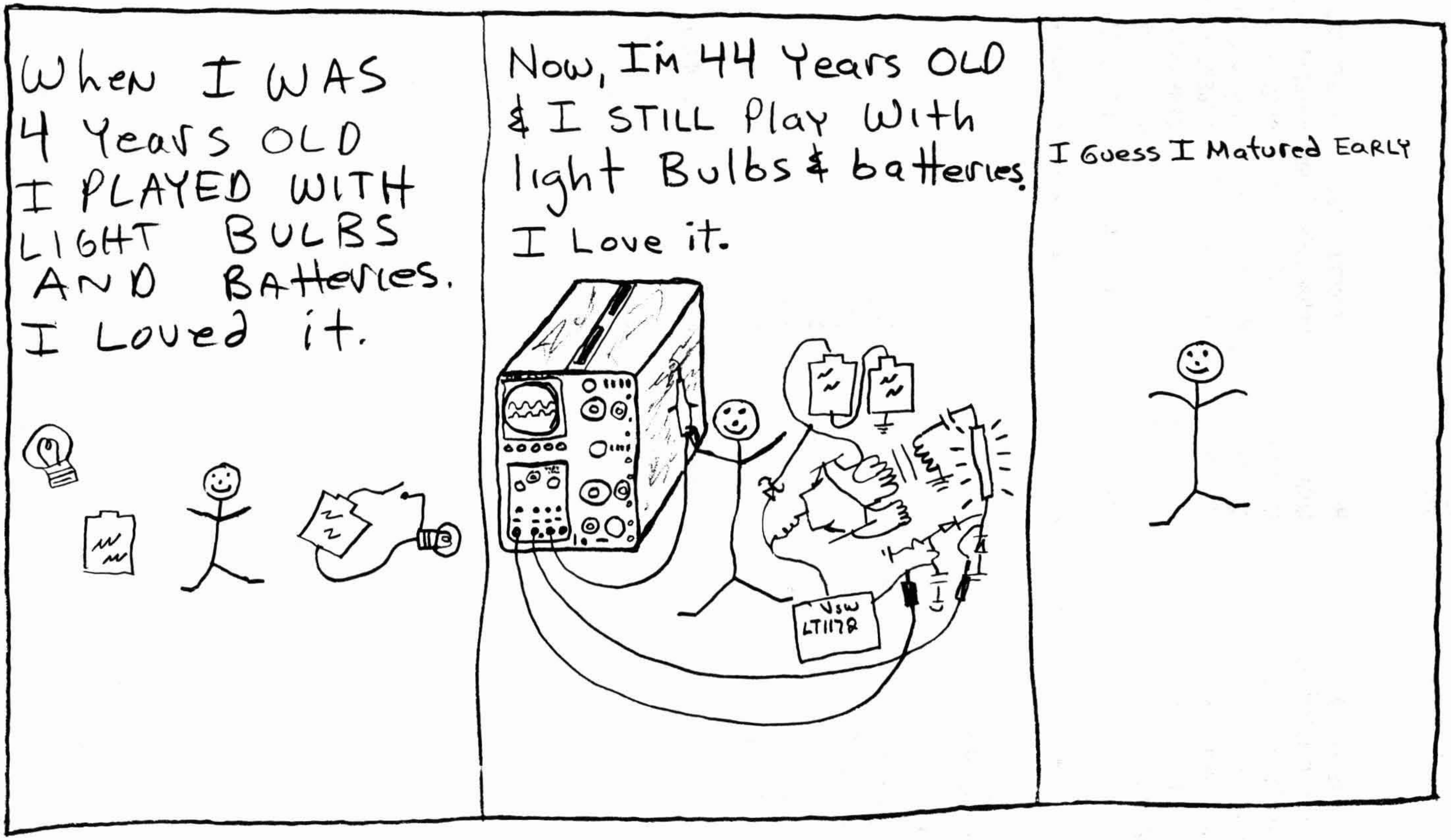


Figure G1. Network Allows CCFL Operation Beyond 20V Inputs


When I WAS
4 Years OLD
I PLAYED WITH
LIGHT BULBS
AND Batteries.
I Loved it.
Now, I'm 44 Years OLD
& I STILL Play With
light Bulbs & batteries.
I Love it.
Vsw
LT1172
I Guess I Matured EARLY

CALL ME ABOUT YOUR BACKlight Application

— '92

LINEAR TECHNOLOGY

Application Note 50

August 1992

Interfacing to Microprocessor Based 5V Systems

Thomas Mosteller

Introduction

As microcontrollers become more compact and powerful, the opportunity arises for the designer to use these digital powerhouses to pack more and more functionality onto small PCBs. A number of devices include 8 or even 10-bit A/Ds, to allow painless conversion from the analog realm into neat and simple digits. For situations where the on-chip A/D is not appropriate or nonexistent, many external A/D systems-on-a-chip are available. Linear Technology has the LTC1099, LTC1096/LTC1098 and the LTC1196/LTC1198 8-bit A/Ds; the LTC1090 thru LTC1096 10-bit A/Ds; and the LTC1290 through LTC1296 12-bit A/Ds.

As attractive as this possibility sounds, it seems the input signal is never in quite the form it needs to be in for easy digitization. It's either too small, too noisy, the impedance is too high, it's not referenced to ground, or some combination of these factors. The problem varies, but it seems there's always *something* that requires a little bit of signal conditioning prior to digitization.

Operational amplifiers are the obvious method of solving these problems, but there are a few snags. One of the most common design constraints on microcontroller based PCBs is to use only one 5V supply. Modern single supply op amps come close to allowing operation under these constraints, but with a few important exceptions the successful designer should be aware of. This note will outline some of these pitfalls, along with techniques for solving them.

The Search for a Rail-to-Rail Op Amp

The first approach is to simply find an op amp which will handle rail-to-rail inputs and outputs. One common method is to use a CMOS op amp, but it's not the panacea it is thought to be by some designers. In general, CMOS output stages do not suffer from the fixed voltage drops inherent in bipolar devices. Instead, the losses are ohmic in nature. As a result, when operating into high impedance loads, the output of a CMOS amplifier typically comes very close to — probably within a few millivolts — the power supply rails.

So, the output is no problem. Now for the bad news, which resides at the inputs. While most CMOS amplifiers can handle inputs down to the negative supply rails (if not always with perfect accuracy), they can't get close to the positive rail. As a class, the input common mode range limit generally falls about 1V to 2.5V below the positive supply.

But there are more problems. In general, CMOS amplifiers have very good input leakage current characteristics, especially at low temperatures. This makes them well suited for high source impedance applications. The kicker, though, is the input offset voltage, which is generally in the millivolt range. This limits the CMOS device's usefulness to low gains. Unfortunately, many sensors have low output voltages which require rather high gains.

Of course, there is a way around these large input offset voltages. Zero drift op amps retain the desirable characteristics of the CMOS output stage while continuously autozeroing the input offset voltage. While many designers are prejudiced against zero drift op amps (especially those who have used older devices), modern "choppers" have eliminated most of the pitfalls. They provide a level of stability over temperature and time no other technology can match. See George Erdi's Design Note 42[1] for a revealing discussion.

In between these two extremes of DC accuracy there lies a middle ground, which entails making a composite amplifier for the job. As shown in Figure 1A, by using a good single supply bipolar op amp as a front end, with an inexpensive 4000 or 74C series CMOS gate as a back end, excellent results can be achieved. Jim Williams outlined

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Note 1: LTC Design Notes, No. 42, *Chopper vs Bipolar Amps – An Unbiased Comparison* by George Erdi, December, 1990.

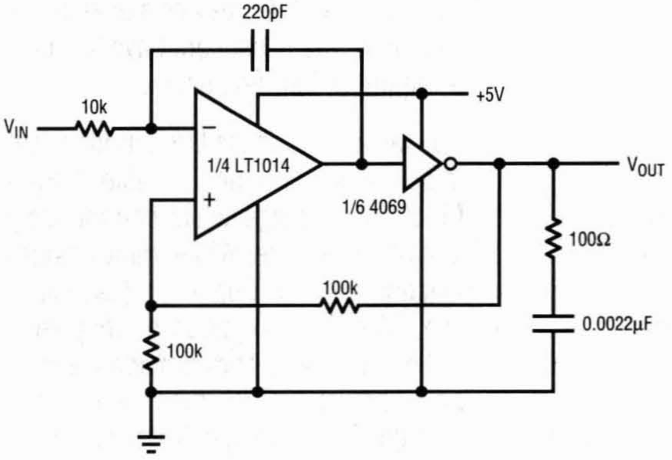
this method in AN18[2], and it works quite well. The front end amplifier's output simply sits at the CMOS gate's input threshold voltage, relieving it of the requirement to swing to the rails.

You can economize on the package count here versus the AN18 circuit. Since we're usually driving a CMOS A/D, with its inherent high input impedance, excellent results can be obtained using just one CMOS gate instead of six. Tests of the circuit using one gate, shown in Figure 1B and 1C, show that you can get within 1LSB or 2 LSBs of both rails, even for 10-bit circuits, for load impedances of 100kΩ or so. Thus, we can combine a good single supply op amp like the LT1013/LT1014 or LT1077/LT1078/LT1079, along with a 4069 hex inverter, and get very good accuracy combined with rail-to-rail output swing. The clever designer can combine leftover gates with the op amps, giving "free" performance enhancement.

Three things to watch for here are:

1. Be careful of noise if you have to route the analog signal all over the noisy digital data paths.
2. If you use a non-inverting gate, reverse the sense of the op amp inputs shown in Figure 1.
3. Be aware that the power supply current of the CMOS gate will go up, since it's operating in its linear region. I tested a few random parts, and found the average quiescent current was in the hundreds of microamps range. Micropower system designers may need to keep this in mind.

This composite amplifier still leaves us short of the mark in one way — common mode range. Single supply bipolar devices like the LT1013/LT1014 have a common mode input range limit of about 1V to 1.5V below the positive supply rail.



LOAD	LT1014		LT1014/4069	
	MIN	MAX	MIN	MAX
200k	0.013	4.390	0	4.991
67k	0.013	4.380	↑	4.971
40k	0.013	4.360		4.951
30k	0.012	4.340		4.932
20k	0.012	4.320		4.893
10k	0.011	4.290	↓	4.797
5k	0.010	4.240	0	4.606

LTAN50 • TA01

Figure 1A. LT1014 and 4069 Composite Amplifier

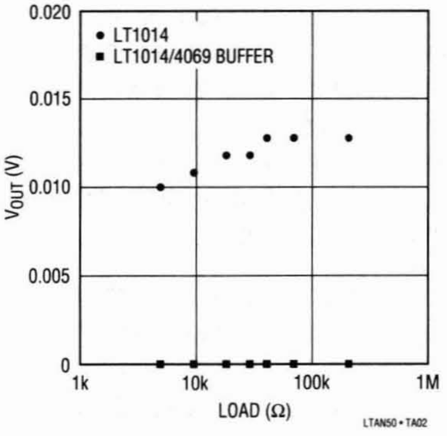


Figure 1B. Saturation Performance – Minimum V_{OUT}

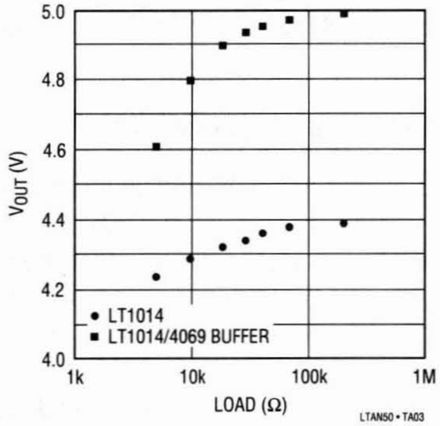


Figure 1C. Saturation Performance – Maximum V_{OUT}

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[2] **Note 2:** LTC Application Note 18, *Power Gain Stages for Monolithic Amplifiers* by Jim Williams, March, 1986.

Giving Up the Search: Alternate Approaches

The easiest method for ensuring proper operation over a full 0V to 5V range is to cheat and use higher power supply voltages. Consider the case where your circuit has a local voltage regulator to provide +5V. You can utilize the input to this regulator to run the analog circuitry. A 6.5V power supply is enough to ensure that devices like the LT1013 and LT1078 will handle 0V to 5V at their inputs and outputs. While the raw supply may have unknown noise characteristics, this is usually handled by the op amp's power supply rejection ratio, which is over 100dB at low frequencies. If you're running off a switching power supply whose output is full of high frequency noise, a small R-C filter in the supply line will help this problem. See Figure 2 for an illustration of this technique.

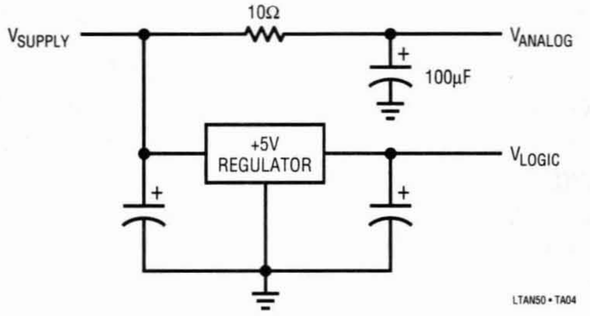


Figure 2. Clean Analog Supply from Input Supply Voltage

If these voltages aren't available from the input power supply, an LT1026 along with a couple of caps provides enough current drive to allow the use of dozens of low power op amps. At low currents, the LT1026 will provide ±9V, which is more than enough to ensure proper operation of inexpensive precision op amps like the LT1097 over a full 0V to 5V range at both the input and the output.

The usual objection to this approach is that it adds cost and requires another IC. This is true, and it may be an important factor in low cost designs. Also, some designers feel that the purity and beauty of their design is spoiled by the addition of other power supply voltages. However, these aesthetic properties manage to survive the affront of incorporating 5V only RS-232 interface chips, even though these devices utilize the same type of charge pump to generate bipolar RS-232 signals.

Realizing this, we can make the RS-232 device serve a dual purpose without requiring any additional parts on many designs, by pulling power from the interface chip's plus and minus rails. For instance, the charge pump on a LT1180 5V RS-232 RX/TX chip can easily provide 10mA to an external load while still meeting the RS-232 interface standard. Noise on these lines can be reduced by a 10Ω/1µF R-C filter. This will provide approximately 100:1 noise reduction at the power supply ripple frequency.

Even if you don't like the idea of generating additional power supplies on your board, you may not have a choice. For instance, if you wish to have a 5V reference on your A/D converter, you're going to need a more positive supply to run that reference.

To those who plan to simply use the V_{CC} line as their 5V reference, beware! This supply is typically noisy due to the rapid current changes caused by the logic chips. In addition, it has a poor ±5% initial tolerance, which amounts to nearly ±13 counts of error in an 8-bit system. Adding a trimmer to adjust the system for proper readings is only a partial solution, since it doesn't allow for the regulator's unspecified time and temperature drift, which will also be poor. These factors are not problems for systems which use transducers with ratiometric output that use the power supply for both the transducer drive and the A/D reference, thereby cancelling any errors in voltage.

One way to reduce this problem is to use Linear Technology's precision fixed output voltage regulators, which have tighter output voltage specs than industry standard parts. For instance, the LT1086-5 has a ±1% initial tolerance, and ±2% over temperature, cutting the initial error to ±3 counts. Compared to industry standard regulators like the 7805, these devices may suffice as a reference in some applications. If you go this route, consider using an R-C filter on the reference path to help kill the noise caused by the digital load.

To those who decide to use a real +5V reference, your problems aren't over just yet. As shown in Figure 3, the typical ±5% power supply tolerance results in a minimum voltage of 4.75V. Using an LT1029 or LT1019 +5V reference, the maximum output voltage is 5.01V. Now you have a system where, worst case, the reference voltage is 0.26V higher than the power supply. This is a problem for any A/D.

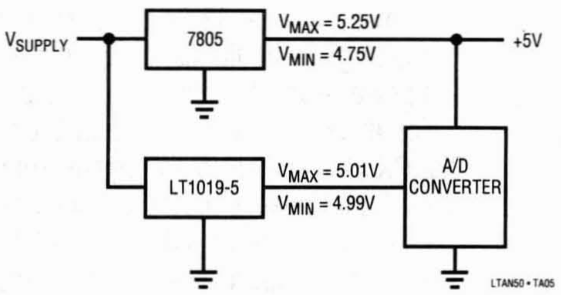


Figure 3. Power Supply Voltage Higher Than Reference Voltage

But this isn't the only place where this issue crops up. If you use the LT1026 voltage converter, your op amps are running on ±9V. With these supply voltages, they are capable of merrily swinging ±6V or ±7V at their outputs, so the A/D inputs present the same unhappy possibilities. Even if allowing the inputs to go beyond the power supply range does not damage or latch up the A/D, it will almost always cause improper readings on the other channels.

The best solution here is system dependent. Some ICs will require Shottky diode clamps on any input capable of exceeding the power supply range to prevent latch-up and possible damage. Others may only require series input resistors for the analog input, but you must test such a combination to make sure that:

1. The conversion speed and accuracy is not degraded by the R-C formed by the input resistor and the A/D's intrinsic capacitance.
2. Errors are not introduced due to input leakage current, especially at elevated temperatures.
3. On a multiple channel A/D, one over range input will not affect the other channels.

If you must ensure that a signal does not go beyond the A/D's power supply range, you can employ the circuit shown in Figure 4. These clamps will hold the input within the legal range as long as the input signal's slew rate does not exceed the clamp amplifier's ability to come out of saturation and limit. The buffer amplifier may be necessary in applications that require low output impedance.

Ensuring that the 5V reference does not exceed the power supply is a slightly different story. While a series resistor may prevent damage to the A/D, accuracy at high voltage inputs will be degraded. Here a different approach is required.

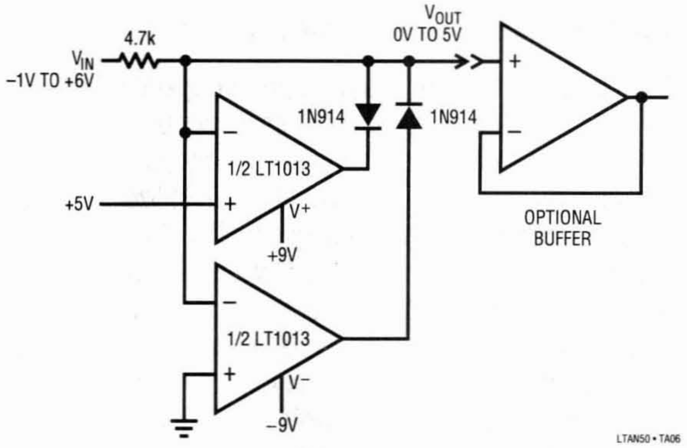


Figure 4. Precision Limiter for Analog-to-Digital Converter Inputs

If both initial and long-term accuracy requirements are low, or a ratiometric system is used, the previously discussed filtered V_{CC} approach is the simplest. This automatically solves the V_{REF} overvoltage problem.

If you have to use a stable reference, there are other approaches. If you need local regulation on your board, you can utilize an LT117 or LT1086 in the circuit shown in Figure 5. The superior reference used in these parts allows them to be set to a voltage which will always be higher than the 5V reference, yet is lower than the 5.25V maximum logic ICs are specified for.

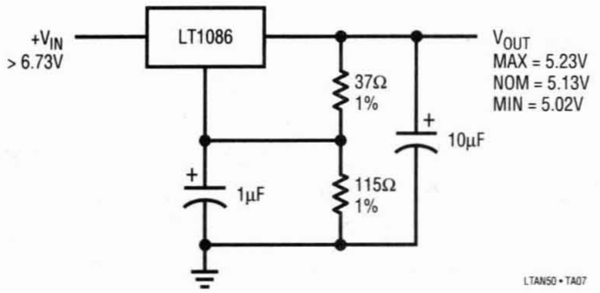


Figure 5. +5V Regulator with 5V > V_{OUT} > 5.25V

However, if your PCB doesn't use local regulation, but brings in a nominal +5V supply from an external source, you're stuck. The typical power supply tolerance means that, unless you take steps to raise the supply voltage on your board, you can't work with a 0V to 5V signal "straight in."

Rescaling the Output to 0V to 2.5V

This is accomplished by realizing that we normally really don't have to use a 0V to 5V input swing on our A/D. Most

A/Ds provide both high and low reference inputs, rather than tying them to the power supply terminals. In fact, given the noisy state of the average digital power supply, the IC manufacturer generally has no choice! We can take advantage of this by using a lower reference voltage that is within the swing capabilities of the unaided single supply op amp.

Most single supply op amps can swing to within 1V of the positive power supply when lightly loaded. Looking over the range of available references leads us to pick 2.5V as a convenient value. References like the LT1004-2.5 and LT1009 are inexpensive and give good accuracy at this voltage level. This reference voltage allows plenty of margin on the output swing at the high end, as well as keeping us out of trouble with the input common mode range. In addition, it's not impossibly low for the A/D. Most 8 and 10-bit designs will work adequately at this reference voltage.

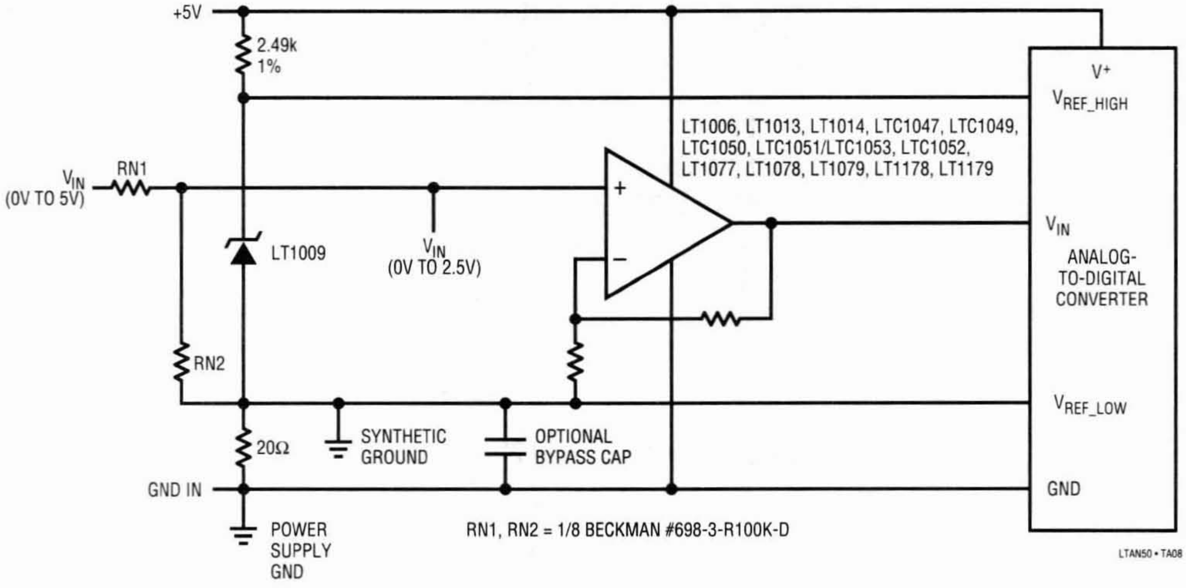
Now we get to the low end. Linear Technology bipolar single supply op amps use a unique output topology which allows them to pull their output down to less than 10mV with good linearity. In an 8-bit, 2.5V reference system, this amounts to an error of approximately 1 count. This grows to 4 or 5 counts in 10-bit systems. However, keep in mind, you can't really use the A/D's full range most of the time — you have to allow some margin for circuit tolerances at both the high and low ends of the A/D's range. Most 10-bit systems will not be noticeably compromised by having 5 counts unavailable at the low end.

But suppose you can't deal with that additional error. There is a simple way to get those lowest few counts back, using a technique known as a synthetic ground. Rather than using the power supply's ground terminal as the common point for the amplifier chain, you use a resistor divider to create an arbitrary ground point offset above power supply ground. This is shown in Figure 6.

Since we only need a few millivolts of offset here, we can use a low value resistor for the bottom of the divider chain. This gives a stable voltage at synthetic ground without drawing a lot of current. To the op amp, it's exactly as though we have power supply voltages of, say, 4.95V and −0.05V.

We can take advantage of the lower reference voltage input on the A/D and feed the synthetic ground into there. Thus, 0 counts will always be equal to the value of synthetic ground, and full scale will be equal to synthetic ground plus the reference voltage.

Some designers may feel uncomfortable without a hardwired ground terminal. In most systems, ground is an arbitrary point, such as the bottom of a bridge rectifier in the power supply. As long as the synthetic ground and the power supply ground are not both tied to a common point, such as AC power supply ground, there's no problem. This



+5V
2.49k
1%
V+
V_REF_HIGH
LT1006, LT1013, LT1014, LTC1047, LTC1049, LTC1050, LTC1051/LTC1053, LTC1052, LT1077, LT1078, LT1079, LT1178, LT1179
V_IN
(0V TO 5V)
RN1
+
−
LT1009
V_IN
(0V TO 2.5V)
V_IN
ANALOG-TO-DIGITAL CONVERTER
RN2
V_REF_LOW
20Ω
SYNTHETIC GROUND
OPTIONAL BYPASS CAP
GND IN
GND
POWER SUPPLY GND
RN1, RN2 = 1/8 BECKMAN #698-3-R100K-D
LTAN50 • TA08

Figure 6. Synthetic Ground

technique is especially good when the voltage being measured is generated by a floating transducer whose output is not committed to ground.

But we're not yet *completely* free of gotchas. You'll have to remember to make all voltage measurements referenced to the synthetic ground, rather than instinctively clipping your DVM lead to power supply ground. This can be a difficult point to get across to troubleshooting personnel. Also, watch out for ground loops when you hook AC powered voltmeters or oscilloscopes to your synthetic ground point.

The most valid complaint is that a cable running from a remote transducer to your circuit will not have a "hard" ground. This is true, and the few ohms to "real" ground could be troublesome in some cases. However, if you use shielded cable, the shield can be isolated from circuit ground and connected to power supply or earth ground. Additionally, the synthetic ground point can be coupled to ground through a bypass cap, giving an AC ground. Be sure to pick a value which will not do funny things to your circuit parameters at the frequencies of interest.

So, now, using this technique, we can finally handle the 0V to 5V input with only 0V and 5V supplies that started this discussion in the first place using the 0V to 5V input in Figure 6. Here, the 5V signal is run through a precision 2:1 divider which is formed by a matched resistor package, such as the Beckman 698-3-R100K-D. These resistors are matched well enough to allow 8-bit accuracy with no trimming. As detailed above, this shifts the 0V to 5V output to a more manageable 0V to 2.5V.

Further, the output of the 2:1 divider is committed to our synthetic ground, rather than the power supply system ground. Using an LT1009 2.5V reference gives us an 8-bit accurate system with no adjustments. The only caveat remaining is that the 0V to 5V signal source and the PCB containing our A/D must not share a common ground, otherwise we must abandon the synthetic ground approach and lose the bottom LSB or two.

The Resolution Issue: When Eight (Bits) Is Not Enough

Resolution, along with memory and megahertz, are some of the things digital systems never have enough of. Linear Technology manufactures a line of 10 and 12 A/Ds which address this need nicely.

But what if 8 bits isn't quite enough, and you need just one more bit? It's hard to justify the cost of another A/D, especially when the microcontroller you're using has one on board already.

The circuit in Figure 7 will add another bit of resolution cheaply. It uses one quad op amp and the same precision resistor package referenced above to "fold" a 0V to 2.47V input to an A/D range of 1.235V to 2.47V while providing a comparator to sense whether the input is in the upper or lower half of the range.

Op amps U1A and U1B, along with RN1 to RN6, form a full wave rectifier with a "center" point equal to the reference voltage, V_{REF_LOW}. Input voltages above V_{REF_LOW} are passed through the rectifier unchanged, while those below V_{REF_LOW} are inverted and shifted upwards according to the equation:

$$V_{OUT} = 2 \times V_{REF\_LOW} - V_{IN}$$

The accuracy of this section is held within 8 bits by the accurate matching of the package's resistors and the low errors in the op amps shown in the figure. If lower power consumption is required, the LT1014 op amps can be replaced by the LT1079 or LT1179.

The 9th bit is formed by the comparator U1C. The output of this comparator will trigger a standard CMOS gate, or its value can be read into a free A/D channel. Note that when the 9th bit is low, the readings are biased upwards and inverted. The proper sense can be restored to the reading in software.

The A/D's positive reference voltage (V_{REF_HIGH}) is set to exactly twice the LT1004-1.2 reference's voltage by op amp U1D. The gain of this circuit is set at precisely 2 by the 7th and 8th resistors in the resistor package. Thus, the A/D sees the input signal changing between 1.235V and 2.47V.

This circuit does require a negative voltage to operate, although it does not have to be regulated.

Even More Resolution

There are times when even more than 12 bits of resolution are required. An example is when the A/D has to monitor a variable which can take on a number of different ranges, each of which requires good precision. For instance,

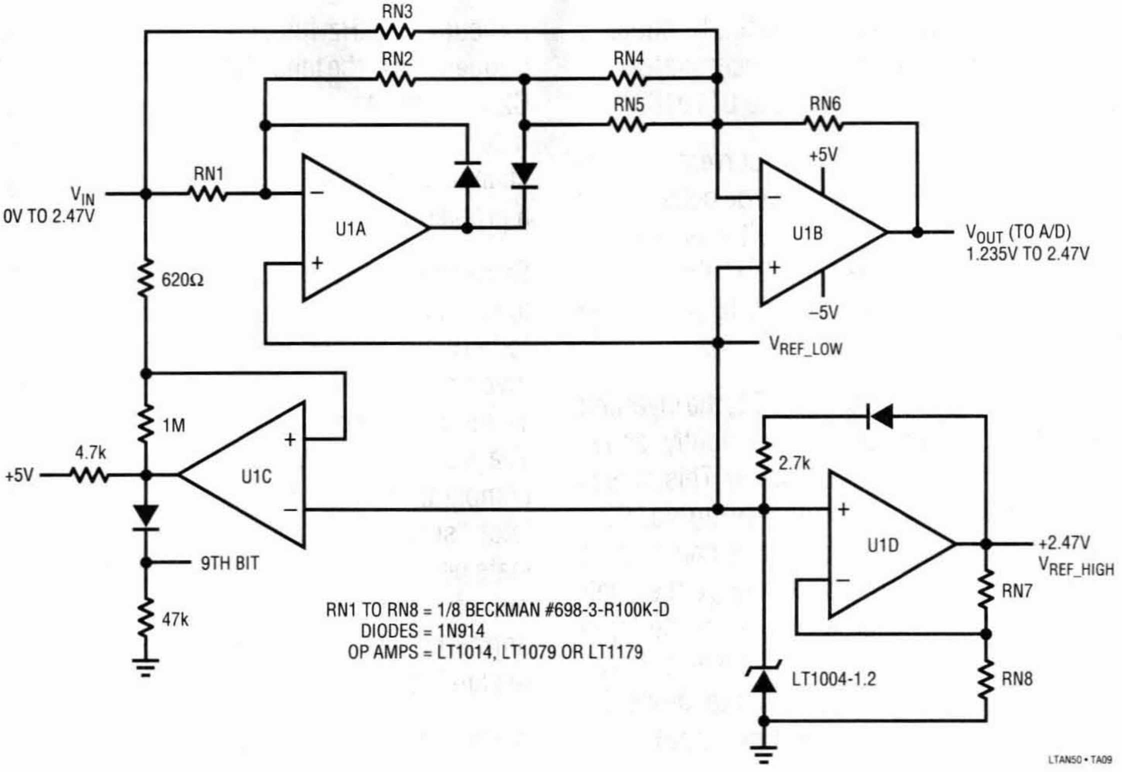

RN3
RN2
RN4
RN5
RN6
+5V
RN1
V_{IN}
0V TO 2.47V
U1A
U1B
V_{OUT} (TO A/D)
1.235V TO 2.47V
620Ω
–5V
V_{REF_LOW}
1M
4.7k
+5V
U1C
2.7k
U1D
+2.47V
V_{REF_HIGH}
9TH BIT
RN7
47k
RN1 TO RN8 = 1/8 BECKMAN #698-3-R100K-D
DIODES = 1N914
OP AMPS = LT1014, LT1079 OR LT1179
LT1004-1.2
RN8
LTAN50 • TA09

Figure 7. 8-Bit to 9-Bit Converter

industrial temperature monitors use many different kinds of thermocouples, and each of them can be used over a wide range. If the instrument is required to have a display range of 0°F to 2000°F and a resolution of 0.1°F without requiring gain or offset changes, you'd need an A/D with at least 20,000 counts. This implies a 17-bit A/D, an expensive proposition.

There is a less costly approach if you're monitoring a slowly changing parameter like temperature. A voltage to frequency converter can be used to convert the input variable into a precision pulse train. By counting these pulses over a fixed time length, a very accurate voltage reading can be made. This is particularly easy to do in software, as most microcontrollers have an input capture function which allows them to count incoming pulses conveniently.

A simple way to do this is shown in Figure 8. This is a variation on the circuit Jim Williams showed in AN3[3], Figure 12. The major modification made here is that a

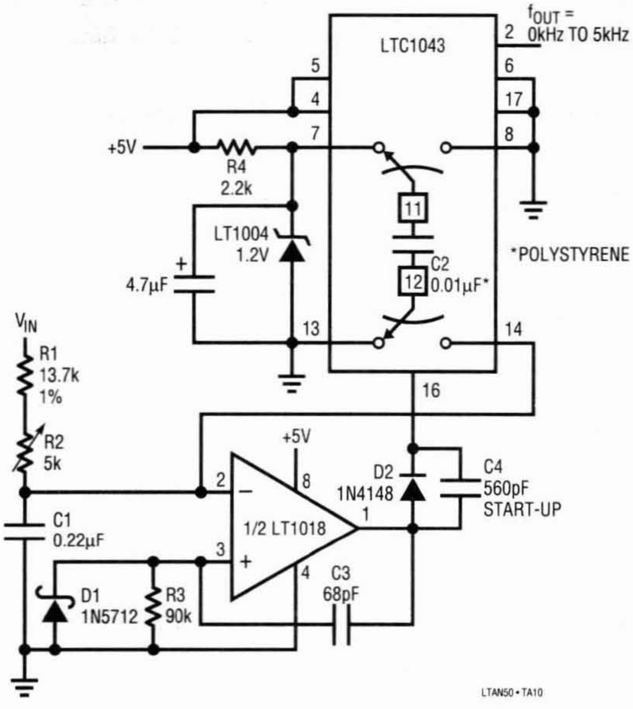

LTC1043
f_{OUT} =
0kHz TO 5kHz
2
5
6
4
17
7
8
+5V
R4
2.2k
11
LT1004
1.2V
C2
0.01µF*
12
4.7µF
*POLYSTYRENE
V_{IN}
13
14
R1
13.7k
1%
16
R2
5k
+5V
2
8
D2
1N4148
C4
560pF
START-UP
C1
0.22µF
1/2 LT1018
1
3
D1
1N5712
R3
90k
4
C3
68pF
LTAN50 • TA10

Figure 8. Single Supply Voltage to Frequency Converter

Note 3: LTC Application Note 3, *Applications for a Switched-Capacitor Instrumentation Building Block* by Jim Williams, July, 1985.

single supply is used rather than the dual ±15 supplies employed in the earlier circuit. This necessitates the switch to a single supply comparator, the LT1018.

The circuit operates by balancing the current flowing into the input with discrete packets of charge delivered by the flying capacitor C_T (C2). This capacitor is charged up to a 1.2V reference level when the LTC1043 analog switch's pin 11 and pin 12 are connected to pins 7 and 13 respectively.

As the input voltage charges up capacitor C1, the inverting input of the LT1018 comparator rises slightly above ground, forcing the comparator's output low. This causes the analog switch to change states bringing C2's positively charged end to ground on pin 8 and forcing pin 14 negative. This negatively biased charge then balances the positively biased charge stored on the input capacitor. A delay, provided by C3 and R3, ensures that all of C2's charge is transferred to C1. Clamp diode D1 protects the comparator's noninverting input from excessive negative excursion.

As the input voltage rises, the input capacitor charges more quickly, thus requiring more frequent "hits" of C2's charge to balance the circuit. This action forms a voltage to frequency converter with the following equation:

$$F_{OUT} = \frac{V_{IN}}{\left(R_{IN} \times V_{REF} \times C_T\right)} \qquad \text{(See note 4)}$$

Typical performance specifications are:

V_{IN} = 0V to 5V

F_{OUT} = 0kHz to 5kHz

Linearity = 0.0025%

PSRR = 0.1%/V

TC = 200ppm/°C

I_q = 3mA

Although a 5kHz full-scale frequency is shown, output frequencies in the tens of kHz are possible by rescaling R1, C2 or both. Applications requiring very high resolution may require long pulse accumulation times. For slowly changing variables like temperature this is generally not a problem.

Start-up or overdrive can cause this circuit's AC coupled loop to latch. If the output of the comparator is forced low for an extended period, the analog switch forces C2 to the inverting input of the comparator before it is charged up. This is a stable condition, so oscillation will not commence. The problem is cured by the addition of C4 and D2. When the comparator's output is low, the LTC1043's internal oscillator "sees" C4 to ground and begins oscillating if this state persists. The free running oscillation pumps charge out of C1 until normal operation commences. Under normal conditions, the comparator's output state controls the analog switch through D2.

Another potential problem is that the reversed sense of C2 forces pin 14 of the LTC1043 and the inverting input of the LT1018 below ground. This is usually poor practice. However, the size of the input capacitor has been chosen to limit the excursion below ground to a safe level. The input capacitor should not be made any smaller without careful testing to ensure linearity at high temperatures.

This circuit meets the ideals outlined in the beginning of this note in that it only requires one supply to handle a 0V to 5V input signal. In fact, the input can swing to levels greater than the power supply, since the op amp/comparator is used in the inverting mode — its summing junction is held close to ground at all times.

Note 4: Note the accidental inversion of the C_T term in the AN3 equation.

For literature call **(800) 637-5545**.
For applications help, call (408) 432-1900, Ext. 777.

Application Note 51
August 1992

Power Conditioning for Notebook and Palmtop Systems

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Carl Nelson
Dennis O'Neill
Steve Pietkiewicz
Tim Skovmand
Milt Wilcox

INTRODUCTION

Notebook and palmtop systems need a multiplicity of regulated voltages developed from a single battery. Small size, light weight, and high efficiency are mandatory for competitive solutions in this area. Small increases in efficiency extend battery life, making the final product much more usable with no increase in weight. Additionally, high efficiency minimizes the heat sinks needed on the power regulating components, further reducing system weight and size.

Battery systems include NiCad, nickel-hydride, lead acid, and rechargeable lithium, as well as throw-away alkaline batteries. The ability to power condition a wide range of batteries makes the ultimate product much more attractive because power sources can be interchanged, increasing overall system versatility.

A main rechargeable battery may be any of the four secondary type cells, with a back-up or emergency ability to operate off alkaline batteries. The higher energy density available in non-rechargeable alkaline batteries allows the systems to operate for extended time without battery replacement.

The systems shown here provide power conditioning with high efficiency and low parts count. Trade-offs between complexity and efficiency have been made to maximize manufacturability and minimize cost. All the supplies operate over a wide range of input voltage allowing great flexibility in the choice of battery configuration.

LT1432 Driver for High Efficiency 5V and 3.3V Buck Regulator

The LT1432 is a control chip designed to operate with the LT1170 or LT1270 family of switching regulators to make a very high efficiency (Figure 1) 5V or 3.3V step-down (buck) switching regulator. These regulators feature a low-loss saturating NPN switch that is normally configured with the negative terminal (emitter) at ground. The LT1432 allows the switch to be floated as required in a step-down converter, yet still provides full switch saturation for highest efficiency.

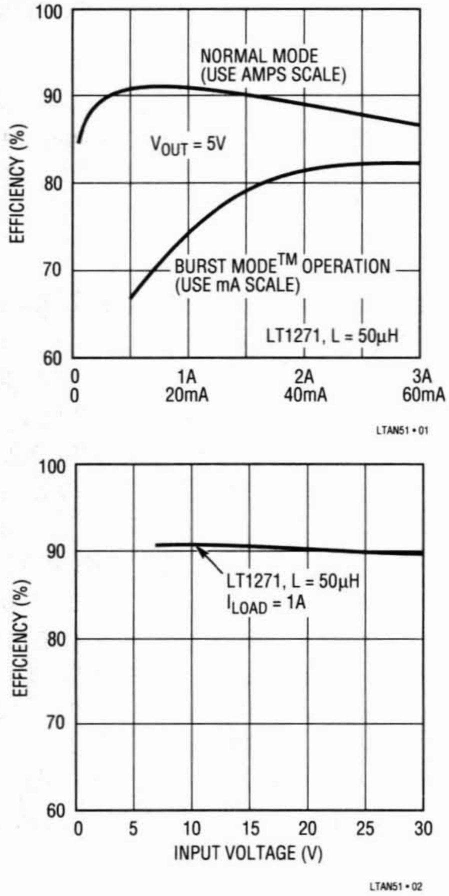


Figure 1. LT1432 5V Efficiency

Burst Mode™ is a trademark of Linear Technology Coporation.

Many other features have been incorporated into the LT1432 to enhance operation in battery powered applications. An accurate current limit uses only 60mV sense voltage, allows for foldback, and uses "free" PC board trace material for the sense resistor. Logic controlled shutdown mode draws only 15µA battery current to allow for extremely long shutdown periods. The switching IC is powered from the regulator output to enhance efficiency and to allow input voltages as low as 6.5V.

The LT1432 has optional Burst Mode^{TM} operation to achieve high efficiency at very light load currents (0mA to 100mA). In normal switching mode, the standby power loss is about 60mW, limiting efficiency at light loads. In burst mode, standby loss is reduced to approximately 15mW. Output ripple is 150mV$_{P-P}$ in this mode, but this is normally well within the requirements for digital logic supplies. Burst Mode^{TM} operation would typically be used for "sleep" conditions where IC memory chips remain powered for data retention, but the remainder of the system is powered down. Load current in this mode is typically in the 5mA-100mA range. The operating mode is under logic control.

The LT1432 is available in 8-pin surface mount and DIP packages. The LT1170 and LT1270 families are available in a surface mount version of the 5-pin TO-220 package.

Circuit Description

The circuit shown in Figure 2 is a basic 5V positive buck converter which can operate with input voltages from 6.5V to 25V. The power switch is located between the V_{SW} pin and GND pin on the LT1271. Its current and duty cycle are controlled by the voltage on the V_C pin with respect to the GND pin. This voltage ranges from 1V to 2V as switch currents increase from zero to full scale. Correct output voltage is maintained by the LT1432 which has an internal reference and error amplifier. The amplifier output is level shifted with an internal open collector NPN to drive the V_C pin of the switcher. The normal resistor divider feedback to the switcher feedback pin cannot be used because the feedback pin is referenced to the GND pin, which is switching many volts. The feedback pin (FB) is simply bypassed with a capacitor. This forces the switcher V_C pin to swing high with about 200µA sourcing capability. The LT1432 V_C pin then sinks this current to control the loop. C4 forms the dominant loop pole with a loop zero added by R1. C5 forms a higher frequency loop pole to control switching ripple at the V_C pin.

A floating 5V power supply for the switcher is generated by D2 and C3 which peak detect the output voltage during switch "off" time. This is a very efficient way of powering the switcher because power drain does not increase with regulator input voltage. However, the circuit is not self-starting, so some means must be used to start the regulator. This is performed by an internal current path in the LT1432 which allows current to flow from the input supply to the V^+ pin during start-up.

In both the 5V and 3.3V regulators, D1, L1, and C2 act as the conventional catch diode and output filter of the buck converter. These components should be selected carefully to maintain high efficiency and acceptable output ripple.

Current limiting is performed by R2. Sense voltage is only 60mV to maintain high efficiency. This also reduces the value of the sense resistor enough to utilize a printed circuit board trace as the sense resistor. The sense voltage has a positive temperature coefficient to match the temperature coefficient of copper.

The basic regulator has three different operating modes, defined by the mode pin drive. Normal operation occurs when the mode pin is grounded. A low quiescent current Burst Mode^{TM} operation can be initiated by floating the mode pin. Input supply current is typically 1.3mA in this mode, and output ripple voltage is 100mV$_{P-P}$. Pulling the mode pin above 2.5V forces the entire regulator into micropower shutdown where it typically draws less than 20µA.

What are the benefits of using an active (synchronous) switch to replace the catch diode? This is the trendy thing to do, but calculations and actual breadboards show that the improvement in efficiency is only a few percent at best. This can be shown with the following simplified formulas:

$$\text{Diode loss} = V_f\,(V_{IN} - V_{OUT})(I_{OUT})/V_{IN}$$

$$\text{FET switch loss} = (V_{IN} - V_{OUT})(R_{SW})(I_{OUT})^2/V_{IN}$$

The change in efficiency is:

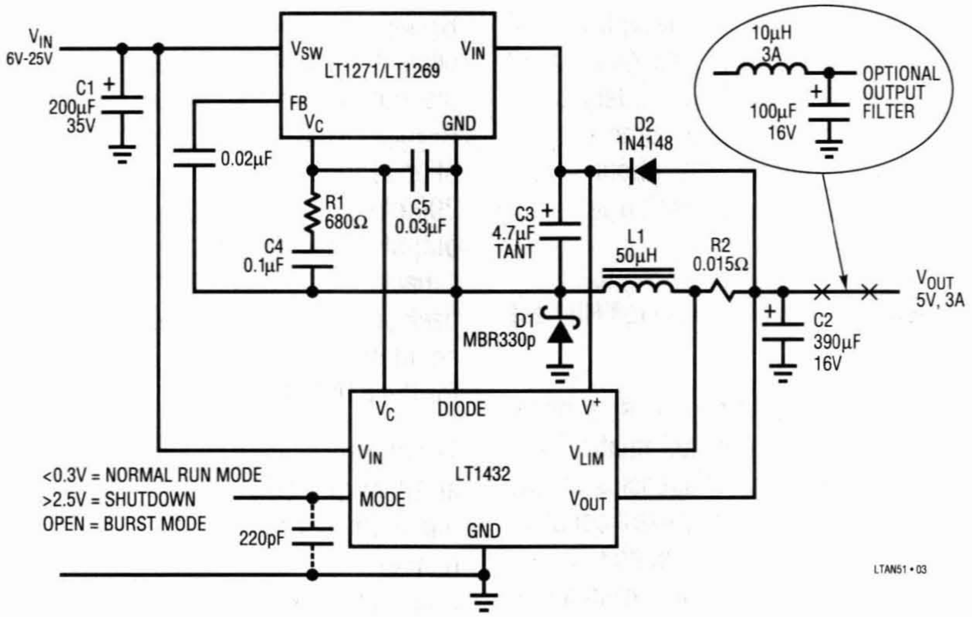
$$(\text{Diode loss} - \text{FET loss})(\text{Efficiency})^2/(V_{OUT})(I_{OUT})$$

This is equal to:

$$(V_{IN} - V_{OUT})(V_f - R_{FET} \times I_{OUT})(E)^2/(V_{IN})(V_{OUT})$$

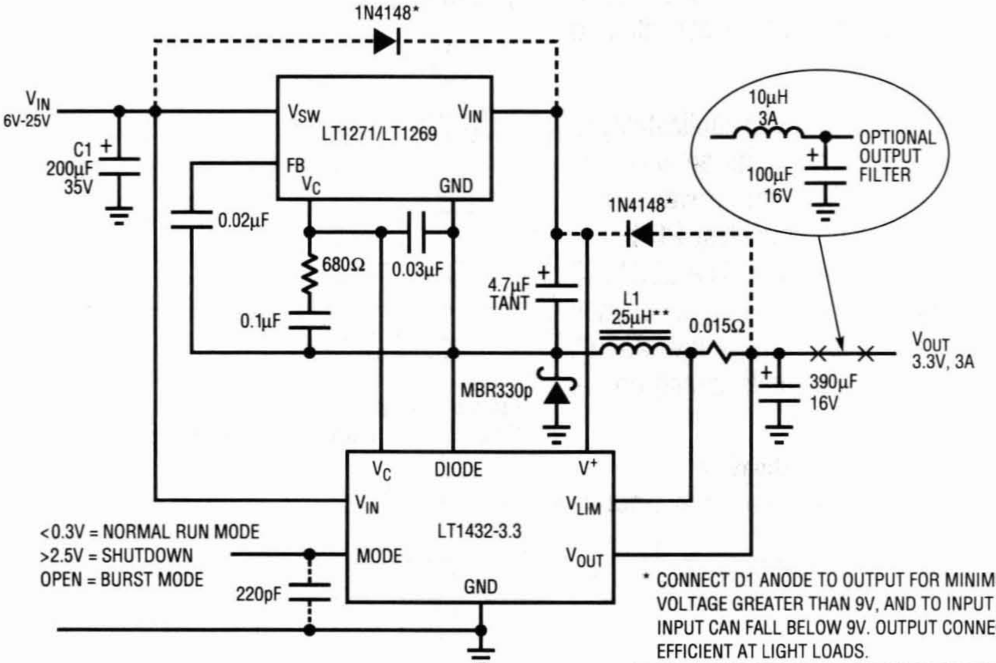
If V_f (diode forward voltage) = 0.45V, V_{IN} = 10V, V_{OUT} = 5V, R_{FET} = 0.1Ω, I_{OUT} = 1A, and efficiency = 90%, the improvement in efficiency is only:

$$(10V - 5V)(0.45V - 0.1\Omega \times 1A)(0.9)2/(10V)(5V) = 2.8\%$$



VIN
6V-25V
C1
200µF
35V
0.02µF
VSW
LT1271/LT1269
VIN
FB
VC
GND
R1
680Ω
C4
0.1µF
C5
0.03µF
C3
4.7µF
TANT
D2
1N4148
L1
50µH
R2
0.015Ω
D1
MBR330p
C2
390µF
16V
VOUT
5V, 3A
10µH
3A
100µF
16V
OPTIONAL
OUTPUT
FILTER
VC
DIODE
V+
VIN
LT1432
VLIM
MODE
VOUT
GND
<0.3V = NORMAL RUN MODE
>2.5V = SHUTDOWN
OPEN = BURST MODE
220pF
LTAN51 • 03

Figure 2. High Efficiency 5V Regulator with Manual Burst Mode™ Operation



1N4148*
VIN
6V-25V
C1
200µF
35V
0.02µF
VSW
LT1271/LT1269
VIN
FB
VC
GND
680Ω
0.03µF
0.1µF
4.7µF
TANT
1N4148*
L1
25µH**
0.015Ω
MBR330p
390µF
16V
VOUT
3.3V, 3A
10µH
3A
100µF
16V
OPTIONAL
OUTPUT
FILTER
VC
DIODE
V+
VIN
LT1432-3.3
VLIM
MODE
VOUT
GND
<0.3V = NORMAL RUN MODE
>2.5V = SHUTDOWN
OPEN = BURST MODE
220pF

* CONNECT D1 ANODE TO OUTPUT FOR MINIMUM INPUT VOLTAGE GREATER THAN 9V, AND TO INPUT IF MINIMUM INPUT CAN FALL BELOW 9V. OUTPUT CONNECTION IS MORE EFFICIENT AT LIGHT LOADS.

** USE MOLYPERMALLOY, KOOLMU OR FERRITE CORE.

LTAN51 • 04

Figure 3. High Efficiency 3.3V Regulator with Manual Burst Mode™ Operation

This does not take FET gate drive losses into account, which can easily reduce this figure to less than 2%. The added cost, size, and complexity of a synchronous switch configuration would be warranted only in the most extreme circumstances.

Burst Mode™ efficiency is limited by quiescent current drain in the LT1432 and the switching IC. The typical Burst Mode™ zero-load input power is 17mW. This gives about one month battery life for a 12V, 1.2AHr battery pack. Increasing load power reduces discharge time proportionately. Full shutdown current is only about 15μA, which is considerably less than the self-discharge rate of typical batteries.

BiCMOS Switching Regulator Family Provides Highest Step-Down Efficiencies

The LTC1147/LTC1148/LTC1149 family of step-down switching regulator controllers features automatic Burst Mode™ operation to maintain high efficiencies at low output currents. All members of the family use a constant offtime, current mode architecture. This results in excellent line and load transient response, constant inductor ripple current, and well controlled start-up and short circuit currents. The LTC1147 drives a single external P-channel MOSFET, while the LTC1148 and LTC1149 drive synchronous external power MOSFETs at switching frequencies up to 250kHz.

Table 1 gives an overview of the family with applicability to common notebook DC to DC converter requirements. The LTC1147 is available in an 8-pin SOIC and drives only a single power MOSFET, giving it the smallest PC board footprint at a slight penalty in efficiency. The LTC1148 offers synchronous switching capability at input voltages from 4V to 13.5V (16V abs max) with a low 200μA quiescent current. The LTC1149 extends synchronous switching operation up to input voltages of 48V (60V abs max) with a slight penalty in quiescent current.

The rated current level for all three device types is set by the external sense resistor according to the formula I_{OUT} = 100mV/R_{SENSE}. The maximum peak inductor current and Burst Mode™ current are also linked to R_{SENSE}. The peak current is limited to 150mV/R_{SENSE}, while Burst Mode™ operation automatically begins when the output current drops below approximately 15mV/R_{SENSE}. In this mode, the external MOSFET(s) are are held off to reduce switching losses and the controller sleeps at 200μA supply current (600μA for the LTC1149), while the output capacitor supports the load. When the output capacitor discharges 50mV, the controller briefly turns back on, or "bursts," to recharge the capacitor. Complete shutdown reduces the supply current to only 10μA (150μA for the LTC1149).

The first application shown in Figure 4 converts 5V to 3.3V at 1A output current. By choosing the LTC1147-3.3, a minimum board space solution is achieved at a slight penalty in peak efficiency (the LTC1148-3.3 driving synchronous MOSFETs in this application would add approximately 2.5% to the high current efficiency). Figure 5 shows how Burst Mode™ operation maintains high operating efficiencies at low output currents.

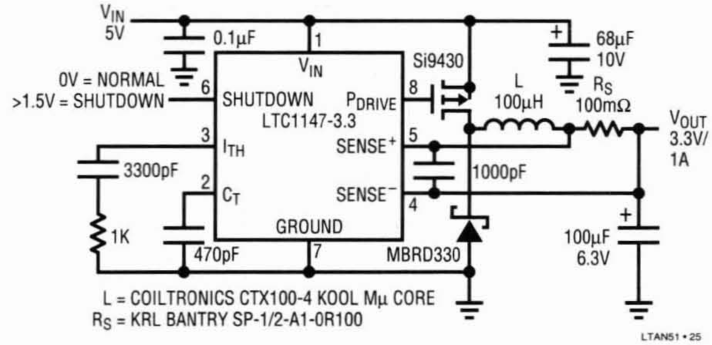


Figure 4. High Efficiency Surface Mount 5V to 3.3V Converter Delivers 1A in Minimum Board Area

Table 1. LTC1147/LTC1148/LTC1149 Applications

	LTC1147-3.3	LTC1147-5	LTC1148-3.3	LTC1148-5	LTC1148	LTC1149-3.3	LTC1149-5	LTC1149
Continuous Input Voltage < 48V						X	X	X
Continuous Input Voltage < 13.5V	X	X	X	X	X			
Low Dropout 5V		X		X			X	
Adjustable/Multiple Output					X			X
5V to 3.3V	X			X				
Minimum Board Area	X	X						

In the second application (Figure 6), an LTC1148-5 is used as the controller for a 10W high efficiency regulator. This circuit can be used with as few as 5 NiCad or NiMH cells thanks to its excellent low dropout performance. Like other members of the family, the LTC1148 goes to 100% duty cycle (P-channel MOSFET turned on DC) in dropout. The input to output voltage differential required to maintain regulation then simply becomes the product of the load current and total resistance of the MOSFET, inductor, and current sense resistor. In the Figure 6 circuit, this total resistance is less than 200mΩ. For operation at low input voltages, logic-level MOSFETs must be used.

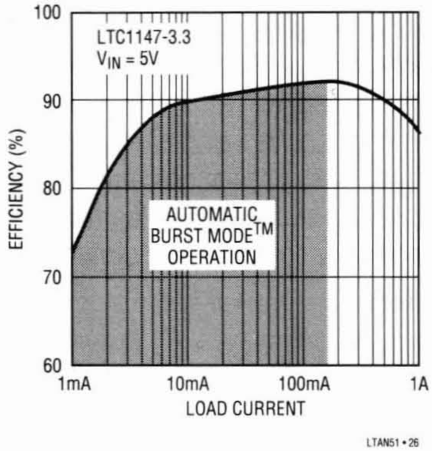


Figure 5. High Operating Efficiency for Figure 4 Circuit Spans Three Decades of Output Current

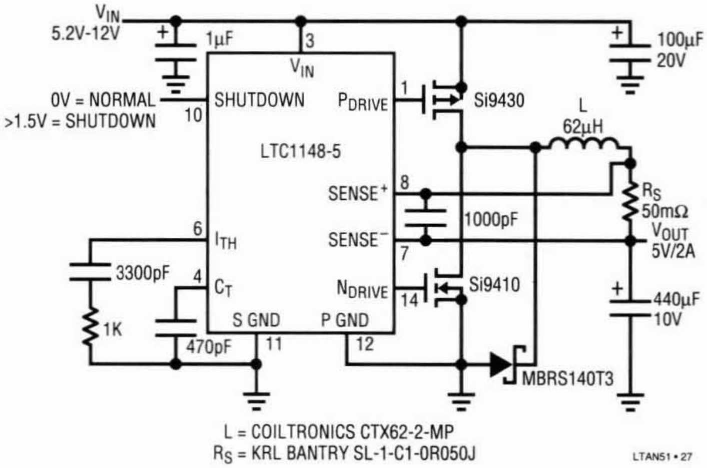

V_{IN}
5.2V-12V
1µF
3
V_{IN}
0V = NORMAL
>1.5V = SHUTDOWN
10
SHUTDOWN
P_{DRIVE}
1
Si9430
100µF
20V
LTC1148-5
L
62µH
SENSE⁺
8
R_S
50mΩ
1000pF
6
I_{TH}
SENSE⁻
7
V_{OUT}
5V/2A
3300pF
4
C_T
N_{DRIVE}
14
Si9410
440µF
10V
1K
S GND
P GND
470pF
11
12
MBRS140T3
L = COILTRONICS CTX62-2-MP
R_S = KRL BANTRY SL-1-C1-0R050J
LTAN51 • 27

Figure 6. High Efficiency Low Dropout 5V Switching Regulator Needs Only 200mV Headroom at 1A Output

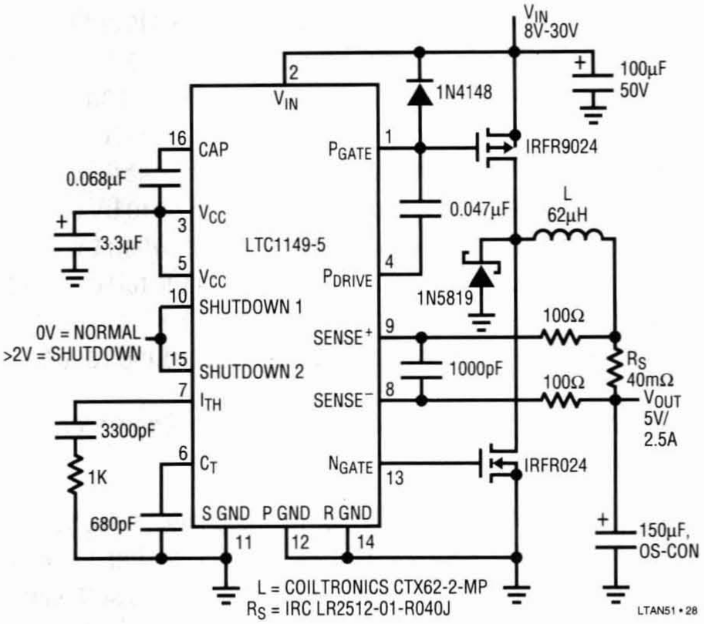

V_{IN}
8V-30V
2
V_{IN}
1N4148
100µF
50V
16
CAP
P_{GATE}
1
IRFR9024
0.068µF
V_{CC}
3
0.047µF
L
62µH
3.3µF
LTC1149-5
5
V_{CC}
P_{DRIVE}
4
1N5819
10
SHUTDOWN 1
100Ω
0V = NORMAL
>2V = SHUTDOWN
SENSE⁺
9
R_S
40mΩ
15
SHUTDOWN 2
1000pF
100Ω
7
I_{TH}
SENSE⁻
8
V_{OUT}
5V/
2.5A
3300pF
6
C_T
N_{GATE}
13
IRFR024
1K
680pF
S GND
P GND
R GND
11
12
14
150µF,
OS-CON
L = COILTRONICS CTX62-2-MP
R_S = IRC LR2512-01-R040J
LTAN51 • 28

Figure 7. High Efficiency 5V/2.5A Regulator Operates from AC Wall Adapters as High as 30V

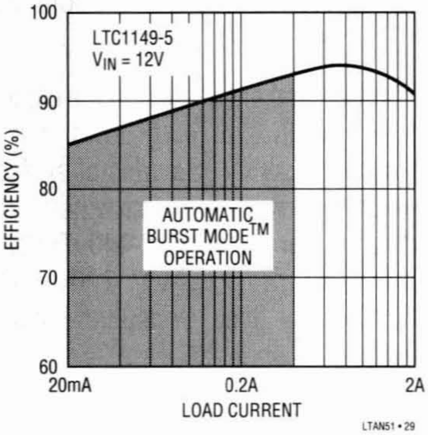


Figure 8. Operating Efficiency for LTC1149-5 High Efficiency Converter

While the 13.5V input voltage rating of the LTC1147 and LTC1148 can generally accommodate most battery packs, the AC wall adapters used in conjunction with notebook systems often dictate significantly higher input voltages. This is the primary home for the LTC1149, shown in the Figure 7 application. This 2.5A regulator can operate at input voltages from 8V (limited by the standard MOSFET threshold voltages) to 30V, while still providing excellent efficiency as shown in Figure 8. The synchronous switch plays an increasing role at high input voltages due to the low duty cycle of the main switch.

Board layout of the Figures 4, 6, and 7 circuits is critical for proper transition between Burst Mode™ operation and continuous operation. The timing capacitor pin and inductor current are the two most important waveforms to monitor while checking an LTC1147/LTC1148/LTC1149 regulator. The timing capacitor pin only goes to 0V during sleep intervals, which should only happen when the load current is less than approximately 20% of the rated output current. Consult the appropriate data sheet for information on proper component location and ground routing.

Surface Mount Capacitors for Switching Regulator Applications

A good rule of thumb for the output capacitor selection in all LTC1147/LTC1148/LTC1149 circuits is that it must have an ESR less than or equal to the sense resistor value (for example, 50mΩ for the Figure 6 circuit). In surface mount applications multiple capacitors may have to be paralleled to meet the capacitance, ESR, or RMS current handling requirements of the application. Aluminum electrolytic and dry tantalum capacitors are both available in surface mount configurations.

In the case of tantalum, it is critical that the capacitors are surge tested for use in switching power supplies. An excellent choice is the AVX TPS series of surface mount tantalum capacitors, available in case heights ranging from 2mm to 4mm. For example, if 440µF/10V is called for in an application, (2) AVX 220µF/10V (P/N TPSE227K010) could be used. Consult the manufacturer for other specific recommendations.

High Efficiency Linear Supplies

The switching supplies operate over a wide input range while maintaining high efficiency. Alternative notebook systems have been developed for narrow supply operation using for example, four NiCad batteries and a linear regulator to provide the 5V output. At full charge, four NiCad batteries can be as high as 6V and are allowed to discharge down to 4.5V while directly powering the system. A high efficiency low dropout linear regulator suited for this technique is shown in Figure 9.

This is a complete IC in a very low cost TO-92 3-pin package driving a low saturation PNP transistor. The dropout voltage of this regulator depends on the PNP transistor saturation and, for the one shown, is 0.25V at 3A output current — lower at lower current. The simplicity of this system is attractive for notebook applications and efficiency is good since little power is lost across the linear regulator at low input voltages.

For input voltages of 5.2V* and above, the output is regulated at 5V. As the battery voltage decreases below 5.2V*, the transistor saturates and the output voltage follows the input voltage down with the saturation voltage of the transistor subtracted from the input voltage.

The LT1123 low dropout driver can supply up to 125mA of base current to the MJE1123 pass transistor (any power PNP can be used). At dropout this current is supplied continuously into the base of the pass transistor as the transistor remains in saturation. If lower drive current is desired an optional resistor (R2) can be inserted in series with the base of the transistor to minimize the drive current and decrease the power dissipation in the IC. An N-channel FET can be inserted in series with the drive lead of the LT1123 to electrically shutdown the system.

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* Actual voltage depends on load current.

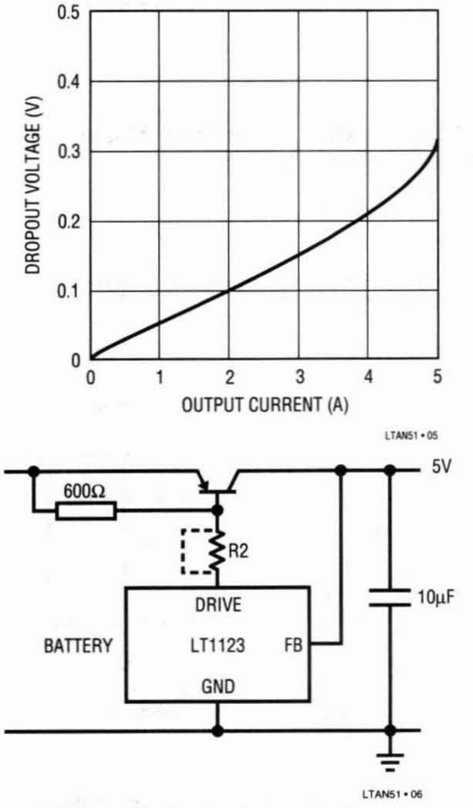


Figure 9. LT1123 Dropout Voltage

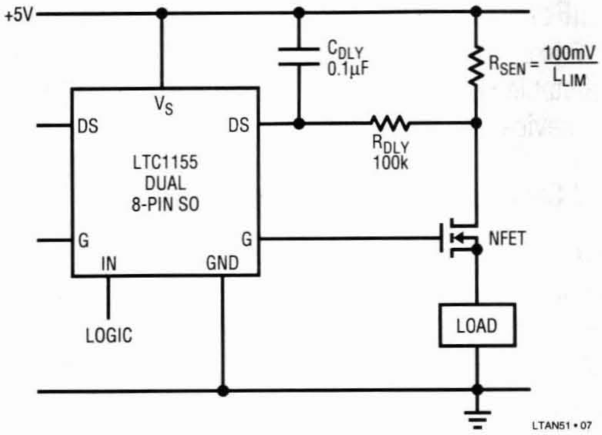

+5V
V_S
LTC1155
DUAL
8-PIN SO
DS
DS
G
G
IN
GND
LOGIC
C_{DLY} 0.1µF
$R_{SEN} = \frac{100mV}{I_{LIM}}$
R_{DLY} 100k
NFET
LOAD
LTAN51 • 07

Figure 10. LTC1155 Dual Micropower N-Channel MOSFET Driver

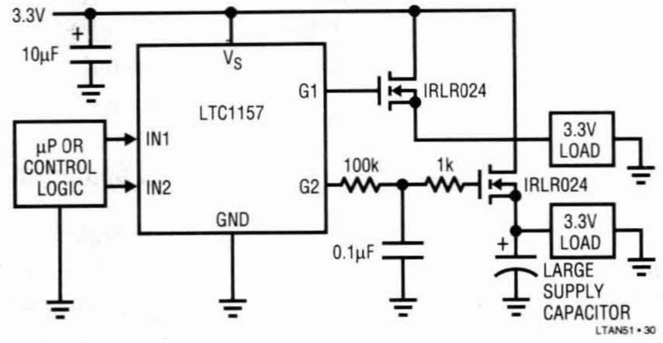

3.3V
10µF
V_S
LTC1157
µP OR CONTROL LOGIC
IN1
IN2
G1
G2
GND
IRLR024
IRLR024
100k
1k
0.1µF
3.3V LOAD
3.3V LOAD
LARGE SUPPLY CAPACITOR
LTAN51 • 30

Figure 11. LTC1157 Dual 3.3V MOSFET Driver

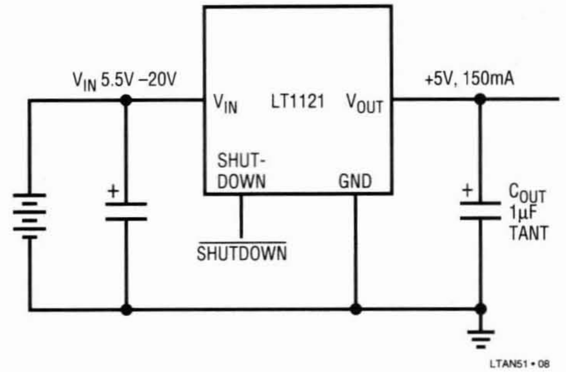

V_{IN} 5.5V –20V
V_{IN}
LT1121
V_{OUT}
SHUT-DOWN
GND
SHUTDOWN
+5V, 150mA
C_{OUT} 1µF TANT
LTAN51 • 08

Figure 12. LT1121 Micropower Low Dropout Regulator

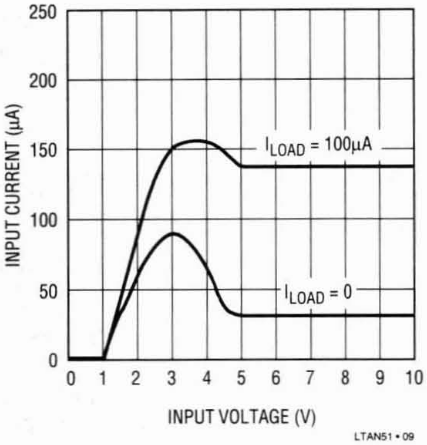


Figure 13. LT1121 Input Current

Power Switching with Dual High Side Micropower N-Channel MOSFET Drivers

The LT1155 dual high side N-channel FET gate driver allows using low cost N-channel FETs for high side switching applications. No external components are needed since an internal charge pump boosts the gate above the positive rail, fully enhancing an N-channel MOSFET. Micropower operation, with 8µA standby current and 85µA operating current, allows use in virtually all battery powered systems even for main power switching.

Included on the chip is over-current sensing to provide automatic shutdown in case of short circuits. A time delay can be added in series with the current sense to prevent false triggering on high in-rush loads such as capacitors or lamps.

The LTC1155 operates off a 4.5V to 18V supply input and safely drives the gates of virtually all FETs. It is particularly well-suited for portable applications where micropower operation is critical. The device is available in 8-pin SO and DIP packages.

The LTC1157 is a dual driver for 3.3V supplies. (N-channel switches are required at 3.3V because P-channel MOSFETs do not have guaranteed $R_{DS(ON)}$ with V_{GS} = 3.3V.) The LTC1157 internal charge pump boosts the gate drive voltage 5.4V above the positive rail (8.7V above ground), fully enhancing a logic-level N-channel MOSFET for 3.3V high side switching applications. The charge pump is completely on-chip and therefore requires no external components to generate the higher gate voltage. The charge pump has been designed to be very efficient, requiring only 3µA in the standby mode and 80µA while delivering 8.7V to the power MOSFET gate.

Figure 11 demonstrates how two surface mount MOSFETs and the LTC1157 can be used to switch two 3.3V loads. The gate rise and fall time is typically in the tens of microseconds, but can slowed by adding two resistors and a capacitor as shown on the second channel. Slower rise and fall times are sometimes required to reduce the start-up current demands of large supply capacitors.

LT1121 Micropower 150mA Regulator with Shutdown

The LT1121 is a low dropout regulator designed for applications where quiescent current must be very low when output current is low. It draws only 30µA input current at zero load current. Ground pin current increases with load current, but the ratio is about 1:25, so the efficiency of the regulator is only about 4% below theoretical maximum for a linear regulator. More importantly, the ground pin current does not increase significantly when the input voltage falls below the minimum required to maintain a regulated output.

These characteristics allow the LT1121 to be used in situations where it is desirable to have the output track the input when the input falls below its normal range. Previous regulators drew such high input current in this condition that micropower operation was not possible.

Extra effort was taken to make the LT1121 stable with small output capacitors that have high ESR. A 1µF tantalum output capacitor is suggested, as compared to 10µF for previous designs. Larger output capacitors can be used without fear of instabilities.

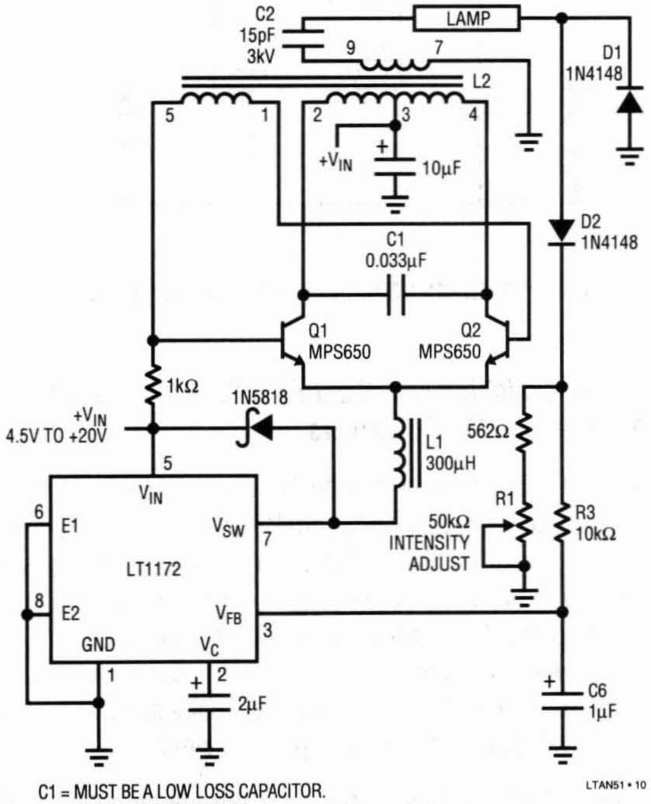
The LT1121 is ideal for the backup and/or suspend mode power supply in notebook computers. A shutdown pin allows the regulator to be fully turned off, with input current dropping to only 16µA. Careful design of the IC circuitry connected to the input and output pins allows the output to be held high while the input is pulled to ground or reversed, without current flowing from the output back to the input. The input pin can be reversed up to 20V.

The LT1121 is available with a fixed output voltage of 3.3V or 5V and as an adjustable device with an output voltage range of 3.75V to 30V. Fixed voltage devices are available in 3-pin SOT-223, and 8-pin SO packages. Adjustable devices are available in an 8-pin SO package.

The LT1129, a 700mA version of the LT1121 is also available. The LT1129 includes all of the protection features of the LT1121. No load quiescent current is slightly higher at 50µA and the LT1129 requires a minimum of 3.3µF of output capacitance. The LT1129 is also available with fixed output voltages of 3.3V and 5V and in an adjustable version with an output range of 3.75V to 5V. The device is available in a 5-pin DD package.

Cold Cathode Fluorescent Display Driver

New backlight systems seem universally to use cold cathode fluorescent tubes. Electroluminescent backlights have limited light output and limited life for notebook systems, and have limited usage among notebook and notebook manufacturers. The cold cathode fluorescent, on the other hand, has high efficiency, long life, and high light output. Typically the cold cathode fluorescent wants to be driven with 1mA to 5mA at 30kHz to 50kHz. The driving voltage and current are a function of the manufacturer and tube geometry.



C1 = MUST BE A LOW LOSS CAPACITOR.
METALIZED POLYCARB
WIMA FKP2 (GERMAN) RECOMMENDED.
L1 = SUMIDA-6345-020 OR COILTRONICS-CTX110092-1.
PIN NUMBERS SHOWN FOR COILTRONICS UNIT
L2 = COILTRONICS-CTX300-4
Q1, Q2 = AS SHOWN OR BCP 56 (PHILIPS SO PACKAGE)
DO NOT SUBSTITUTE COMPONENTS

SUMIDA (708) 956-0666
COILTRONICS (305) 781-8900

Figure 14. CCFL Inverter

Optimally the current through the tube should be regulated to control its brightness.

To understand the operation of the cold cathode fluorescent display driver in Figure 14, the circuit should be looked at as two sections; 1. The regulating loop, 2. The high voltage oscillator/driver.

The regulating loop consists of an LT1172 switching regulator in a buck mode configuration driving constant current into a self-oscillating converter coupled to a high voltage transformer. The architecture of the driver allows a wide input range of battery voltage while maintaining fluorescent tube current constant. In negative buck mode, the LT1172 periodically connects inductor L1 to ground via the switch pin. This creates a flow of current in L1 which is steered by self-oscillating transistors Q1 and Q2 to the primary of transformer L2. The output of L2 is a high voltage AC waveform that is partially ballasted by the 15pF capacitor. To achieve the desired regulation of actual bulb current, D1 and D2 rectify bulb current and pass one phase through R1. This rectified current is converted to a voltage by R1 and filtered by R3 and C6. The filtered signal becomes a feedback signal to the LT1172, which maintains it at 1.25V.

Enclosing the cold cathode fluorescent bulb in a feedback loop allows precise control of its operating current and allows microprocessor control of its brightness. Voltage fed through a resistor to the top of C6, either from a D/A converter or from logic, will control the current through the fluorescent tube, allowing brightness to be varied from a keyboard input.

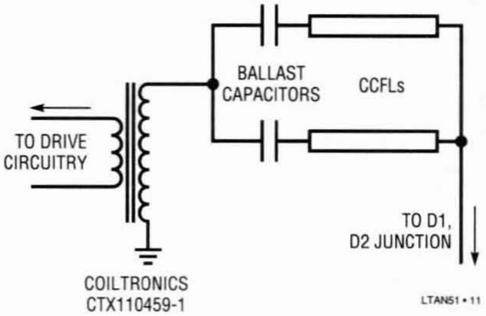


Figure 15. Two Bulb Adaption for Color

This architecture of a buck converter driving a self-oscillating inverter was chosen because it allows a wide range of input voltages. It is also tolerant of winding ratios on the cold cathode fluorescent transformer. One caution with this circuit is the voltage applied to the bulb terminals is not limited if the feedback loop is broken, so care must be taken to minimize the possibility of power being applied to this circuit with the fluorescent tube removed.

BATTERY CHARGING

Lead Acid Battery Charger

Though not as popular as NiCad, Lead acid rechargeable gel cells are attractive because of their high energy density per unit volume. These cells have a long life expectancy when treated properly, but often suffer premature failure because of improper charging. The circuit shown in Figure 16 provides a near ideal charging system for lead-acid cells. It has precise nonlinear temperature compensation, constant voltage charging with constant current override, and high efficiency over a wide range of input and battery voltages.

The basic charger is a flyback design to allow operation with input voltages above or below battery voltage. The LT1171 IC switcher operates at 100kHz and can deliver up to 15W into the battery. A dual op amp is used to control constant voltage and constant current modes. A1 activates as a current limiter when charging current through R7 exceeds a preset limit determined by R3, R6, and R7. This current limit is included to prevent excess charge current for heavily discharged batteries. Losses in R7 are kept low because the voltage drop across R7 is kept to several hundred millivolts.

Lead acid batteries have a nonlinear negative temperature coefficient which must be accurately compensated to ensure long battery life and full charge capacity. R5 is a positive temperature coefficient thermistor (tempsistor) whose +0.7%/°C linear TC is converted to the required nonlinear characteristic by the parallel connection with R2. The combination of R2, R3, and R4 multiply the 1.244V feedback level of the LT1171 to the proper 2.35V

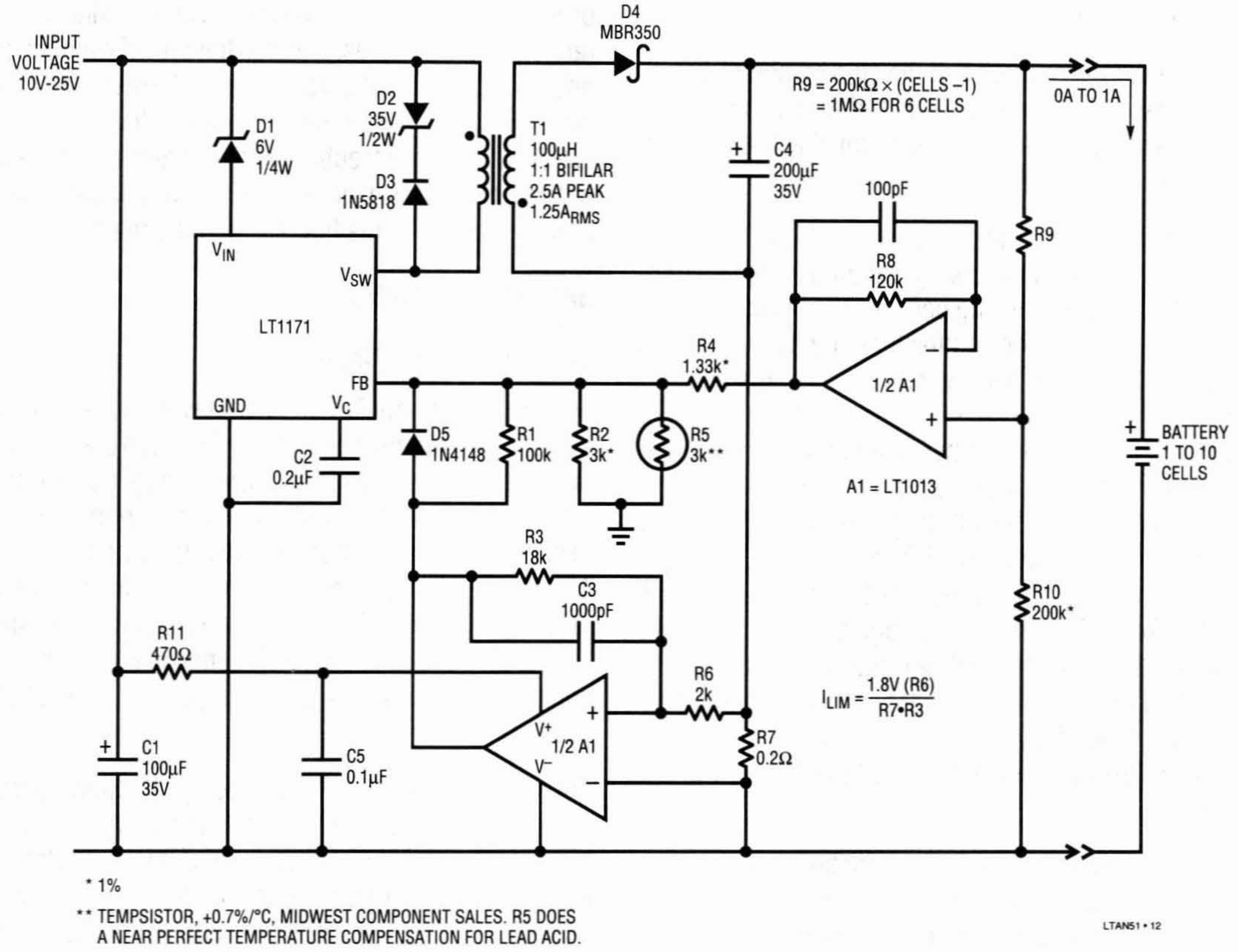

INPUT VOLTAGE 10V-25V
D1 6V 1/4W
D2 35V 1/2W
D3 1N5818
T1 100μH 1:1 BIFILAR 2.5A PEAK 1.25A RMS
D4 MBR350
C4 200μF 35V
R9 = 200kΩ × (CELLS –1) = 1MΩ FOR 6 CELLS
0A TO 1A
100pF
R8 120k
R9
LT1171
VIN
VSW
FB
GND
VC
C2 0.2μF
R4 1.33k*
1/2 A1
D5 1N4148
R1 100k
R2 3k*
R5 3k**
A1 = LT1013
BATTERY 1 TO 10 CELLS
R3 18k
C3 1000pF
R11 470Ω
R6 2k
R7 0.2Ω
R10 200k*
ILIM = 1.8V (R6) / R7•R3
C1 100μF 35V
C5 0.1μF
V+
V–
1/2 A1
* 1%
** TEMPSISTOR, +0.7%/°C, MIDWEST COMPONENT SALES. R5 DOES A NEAR PERFECT TEMPERATURE COMPENSATION FOR LEAD ACID.
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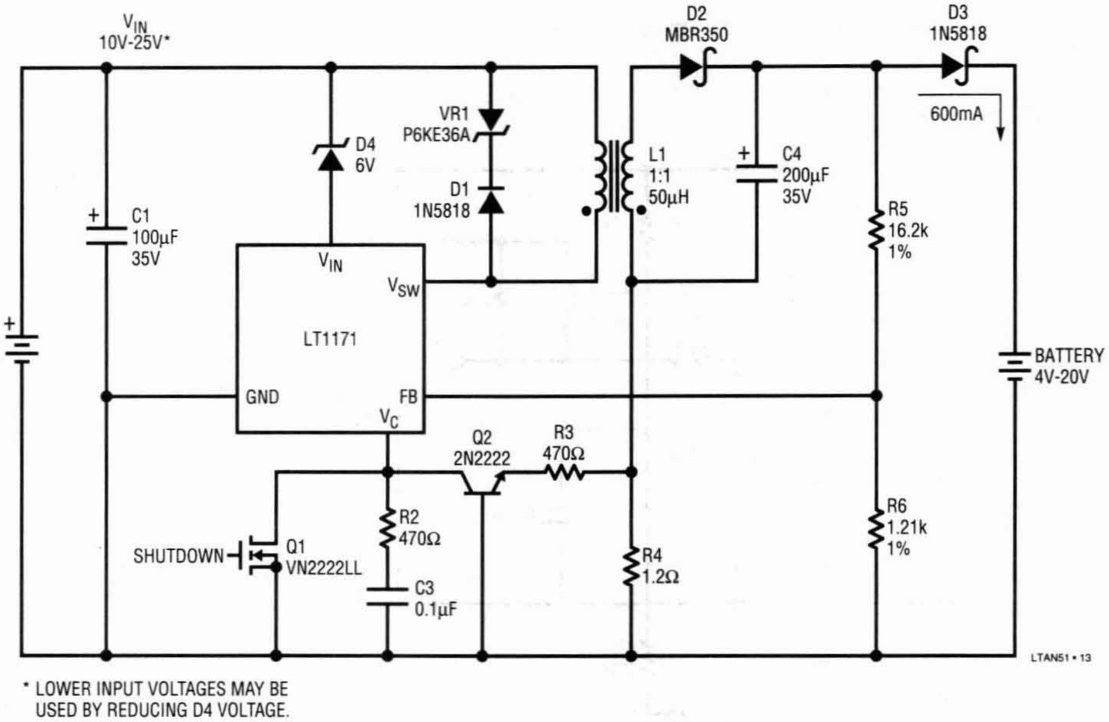
Figure 16. Lead Acid Battery Charger

level required by one cell at 25°C. A2 is used as a buffer to drive the resistor network. This allows large resistors to be used for the cell multiplier string, R9 and R10. R9 is set at 200k for each series cell over one. R9 current is only 12μA, so it can be left permanently connected to the battery. R1 is added to give the charger a finite output resistance (≈0.025Ω/cell) in constant voltage mode to prevent low frequency hunting.

NiCAD Charging

Battery charging is a very important section of any notebook system. The battery charging circuits shown here for nickel cadmium or nickel metal hydride batteries control the current into the battery but do not detect when full battery charge is reached.

The first circuit, Constant Current Battery Charger (Figure 17), is built around a flyback configuration. This allows the battery voltage to be lower or higher than the input voltage. For example, a 16V battery stack may be charged off of a 12V automobile battery. The charge current is sensed by R4, a 1.2Ω resistor and set at approximately 600mA. Resistors R5 and R6 limit the peak output voltage when no battery is connected. Diode D3 prevents the battery discharging through the divider network when the charger is off, while transistor Q1 allows electronic shutdown of the charger.


V_IN
10V-25V*
D2
MBR350
D3
1N5818
600mA
VR1
P6KE36A
D4
6V
D1
1N5818
L1
1:1
50µH
C4
200µF
35V
C1
100µF
35V
R5
16.2k
1%
V_IN
V_SW
LT1171
GND
FB
V_C
BATTERY
4V-20V
Q2
2N2222
R3
470Ω
R2
470Ω
SHUTDOWN
Q1
VN2222LL
C3
0.1µF
R4
1.2Ω
R6
1.21k
1%
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* LOWER INPUT VOLTAGES MAY BE USED BY REDUCING D4 VOLTAGE.

Figure 17. Constant Current Battery Charger

The next two chargers are a high efficiency buck charger configuration. The input voltage must be higher than the battery voltage for charging to occur. These chargers are 90% efficient when charging at maximum output current. No heat sinks are needed on either the switching regulator or diodes because the efficiency is so high.

The dual rate battery charger in Figure 18 uses a logic signal to toggle between a high charge rate, up to 2A, or a trickle rate for keep alive. An LT1006 amplifier senses the current into the battery and drives the feedback pin of an LT1171 switching regulator. The entire control circuit is bootstrapped to the LT1171 and floats at the switching frequency, so stray capacitance must me minimized. A gain setting transistor changes the gain on the LT1006 by shorting or opening resistor R1. This changes the charge rate, for the value shown, between 0.1A and 1A.

The charger in Figure 19 is programmable with a voltage from D-A converters. The charging current is directly proportional to the program voltage. A small sense resistor in the bottom side of the battery senses the battery charging current. This is compared with the program voltage and a feedback signal is developed to drive the LT1171 V_C pin. This controls the charging current from the LT1171 and with appropriate control circuits any battery current may be programmed. Efficiency during high charge currents is 90%.

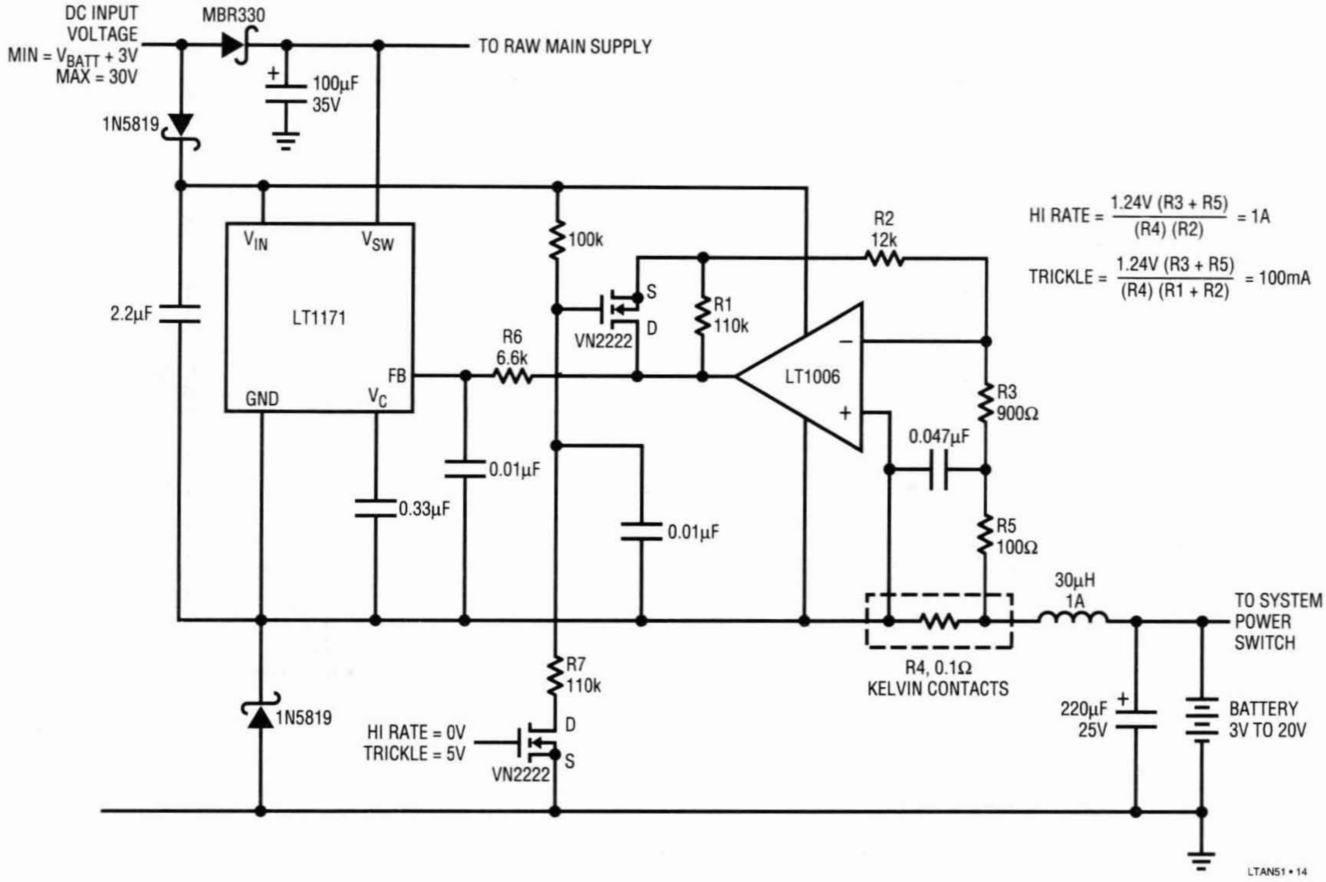
DC INPUT VOLTAGE
MIN = V_{BATT} + 3V
MAX = 30V
MBR330
TO RAW MAIN SUPPLY
100µF
35V
1N5819
2.2µF
V_{IN}
V_{SW}
LT1171
GND
V_C
FB
100k
VN2222
S
D
R1
110k
R2
12k
R6
6.6k
LT1006
0.01µF
0.33µF
0.01µF
R3
900Ω
0.047µF
R5
100Ω
30µH
1A
TO SYSTEM POWER SWITCH
R4, 0.1Ω
KELVIN CONTACTS
R7
110k
1N5819
HI RATE = 0V
TRICKLE = 5V
VN2222
D
S
220µF
25V
BATTERY
3V TO 20V
HI RATE = $\frac{1.24V\,(R3 + R5)}{(R4)\,(R2)}$ = 1A
TRICKLE = $\frac{1.24V\,(R3 + R5)}{(R4)\,(R1 + R2)}$ = 100mA
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Figure 18. High Efficiency Dual Rate Battery Charger (Up to 2A)

LCD Display Contrast Power Supply

LCD display typically requires between –18V and –24V to set the contrast of the display. Usually, a switching regulator is needed in the system to generate this voltage although it runs at low power. The LT1172 generates the voltage with a minimum parts count.

The circuit in Figure 20 works by generating +18V to +24V in a boost configuration and then inverting the voltage by charge pumping. This allows the use of a small inductor for the converter rather than a transformer.

A 4-Cell NiCad Regulator/Charger

The new LTC1155 Dual Power MOSFET Driver delivers 12V of gate drive to two N-channel power MOSFETs when powered from a 5V supply with no external components required. This ability, coupled with its micropower current demands and protection features, makes it an excellent choice for high side switching applications which previously required more expensive P-channel MOSFETs.

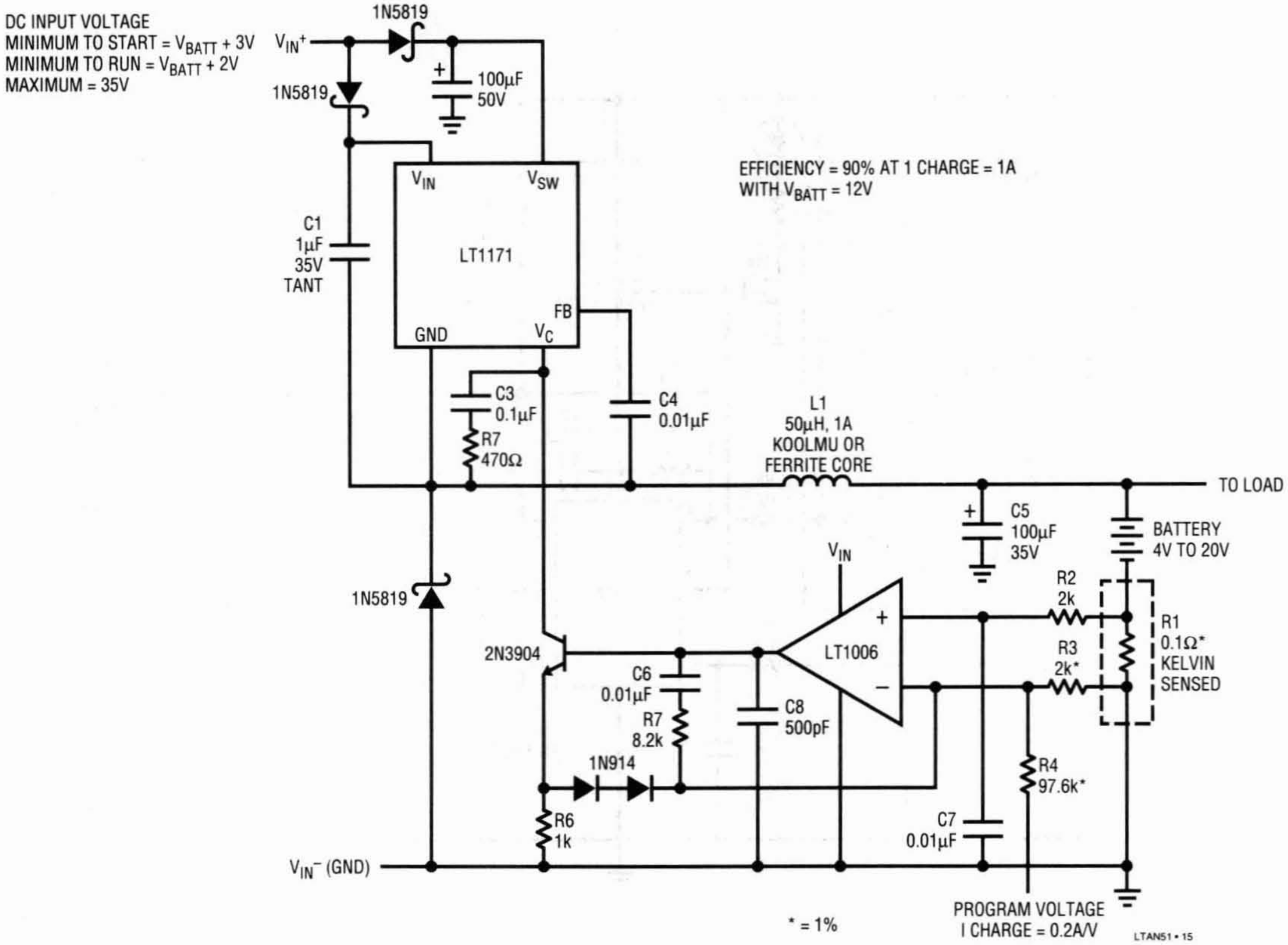
DC INPUT VOLTAGE
MINIMUM TO START = V_{BATT} + 3V
MINIMUM TO RUN = V_{BATT} + 2V
MAXIMUM = 35V
V_{IN}^+
1N5819
1N5819
100µF
50V
V_{IN}
V_{SW}
LT1171
FB
GND
V_C
C1
1µF
35V
TANT
EFFICIENCY = 90% AT 1 CHARGE = 1A
WITH V_{BATT} = 12V
C3
0.1µF
R7
470Ω
C4
0.01µF
L1
50µH, 1A
KOOLMU OR
FERRITE CORE
TO LOAD
C5
100µF
35V
BATTERY
4V TO 20V
V_{IN}
1N5819
2N3904
LT1006
R2
2k
R3
2k*
R1
0.1Ω*
KELVIN
SENSED
C6
0.01µF
R7
8.2k
C8
500pF
1N914
R4
97.6k*
R6
1k
C7
0.01µF
V_{IN}^- (GND)
PROGRAM VOLTAGE
I CHARGE = 0.2A/V
* = 1%
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Figure 19. High Efficiency Programmable Buck-Mode Battery Charger (Input Voltage Must be Higher than Battery Voltage)

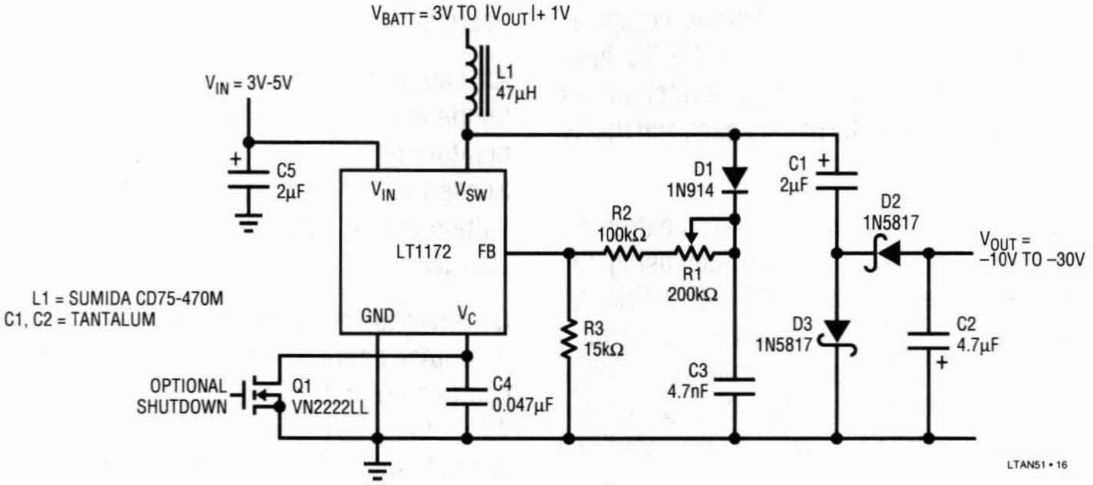
V_{BATT} = 3V TO $|V_{OUT}|$+ 1V
L1
47µH
V_{IN} = 3V-5V
C5
2µF
V_{IN}
V_{SW}
LT1172
FB
GND
V_C
D1
1N914
C1
2µF
D2
1N5817
R2
100kΩ
R1
200kΩ
V_{OUT} =
–10V TO –30V
L1 = SUMIDA CD75-470M
C1, C2 = TANTALUM
R3
15kΩ
D3
1N5817
C2
4.7µF
C3
4.7nF
OPTIONAL
SHUTDOWN
Q1
VN2222LL
C4
0.047µF
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Figure 20. LCD Bias Circuit Generates –24V

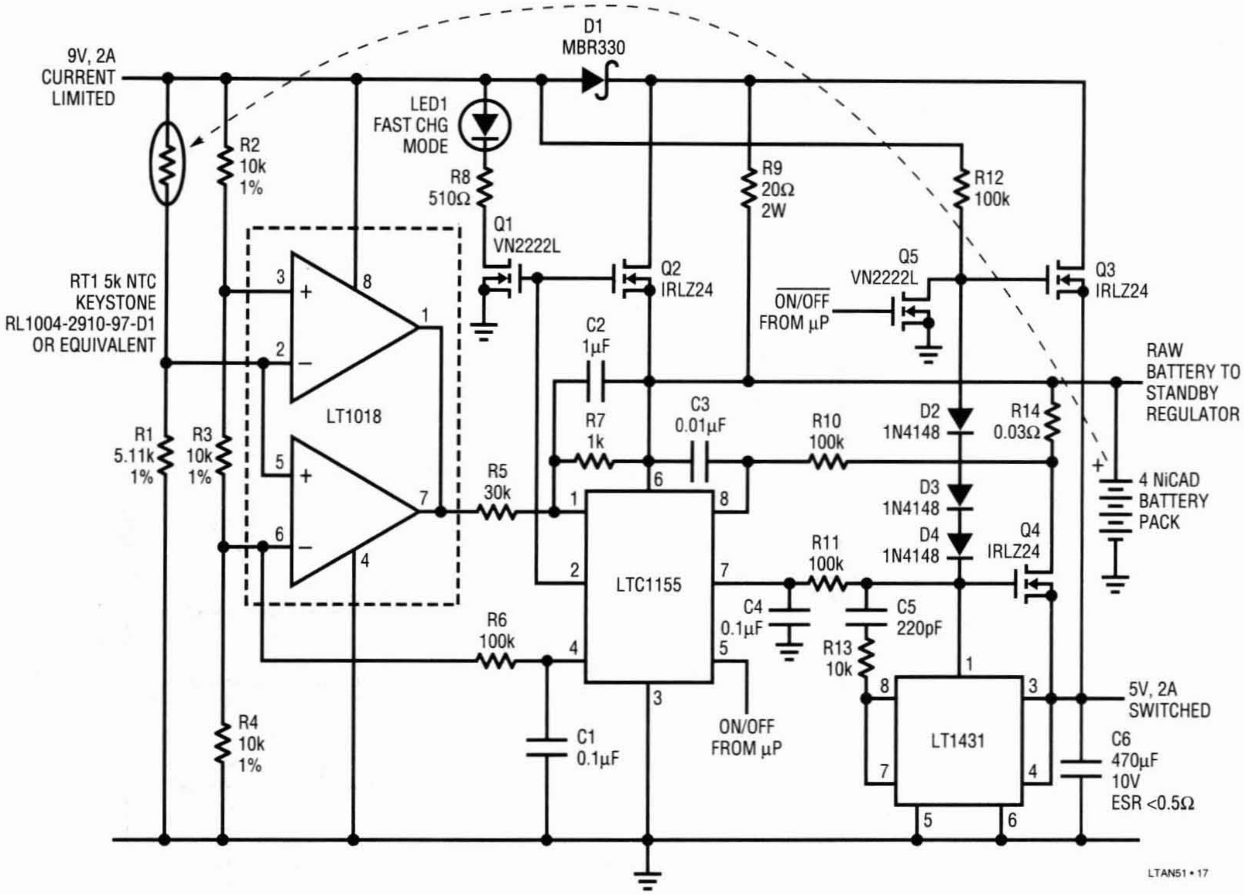
9V, 2A
CURRENT
LIMITED
D1
MBR330
LED1
FAST CHG
MODE
R8
510Ω
R2
10k
1%
RT1 5k NTC
KEYSTONE
RL1004-2910-97-D1
OR EQUIVALENT
R1
5.11k
1%
R3
10k
1%
R4
10k
1%
3
8
2
1
5
7
6
4
LT1018
Q1
VN2222L
Q2
IRLZ24
C2
1μF
R7
1k
C3
0.01μF
R5
30k
R6
100k
C1
0.1μF
LTC1155
1
2
3
4
5
6
7
8
C4
0.1μF
ON/OFF
FROM μP
R9
20Ω
2W
R10
100k
R11
100k
C5
220pF
R13
10k
R12
100k
Q5
VN2222L
ON/OFF
FROM μP
Q3
IRLZ24
D2
1N4148
D3
1N4148
D4
1N4148
R14
0.03Ω
Q4
IRLZ24
RAW
BATTERY TO
STANDBY
REGULATOR
4 NiCAD
BATTERY
PACK
LT1431
8
7
1
3
4
5
6
5V, 2A
SWITCHED
C6
470μF
10V
ESR <0.5Ω
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Figure 21. The LTC1155 Dual MOSFET Driver Provides Gate Drive and Protection for a 4-Cell NiCad Charger and Regulator

A notebook computer power supply system in Figure 21 is a good example of an application which benefits directly from this high side driving scheme. A 4-cell, NiCad battery pack can be used to power a 5V notebook computer system. Inexpensive N-channel power MOSFETs have very low ON resistance and can be used to switch power with low voltage drop between the battery pack and the 5V logic circuits.

Figure 21 shows how a battery charger and an extremely low voltage drop 5V regulator can be built using the LTC1155 and three inexpensive power MOSFETs. One half of the LTC1155 Dual MOSFET Driver controls the charging of the battery pack. The 9V, 2A current limited wall unit is switched directly into the battery pack through an extremely low resistance MOSFET switch, Q2. The gate drive output, pin 2, generates about 13V of gate drive to fully enhance Q1 and Q2. The voltage drop across Q2 is only 0.17V at 2A and, therefore, can be surface mounted to save board space.

An inexpensive thermistor, RT1, measures the battery temperature and latches the LTC1155 off when the temperature rises to 40°C by pulling low on pin 1, the Drain Sense Input. The window comparator also ensures that battery packs which are very cold (<10°C) are not quick charged.

Q1 drives an indicator lamp during quick charge to let the computer operator know that the battery pack is being charged properly. When the battery temperature rises to 40°C, the LTC1155 latches off and the battery charge current flowing through R9 drops to 150mA.

A 4-cell NiCad battery pack produces about 6V when fully charged. This voltage will drop to about 4.5V when the batteries are nearly discharged. The second half of the LTC1155 provides gate voltage drive, pin 7, for an extremely low voltage drop MOSFET regulator. The LT1431 controls the gate of Q4 and provides a regulated 5V output when the battery is above 5V. When the battery voltage drops below 5V, Q4 acts as a low resistance switch between the battery and the regulator output.

A second power MOSFET, Q3, connected between the 9V supply and the regulator output "bypasses" the main regulator when the 9V supply is connected. This means that the computer power is taken directly from the AC line while the charger wall unit is connected. The LT1431 provides regulation for both Q3 and Q4, and maintains a constant 5V at the regulator output. The diode string made up of diodes D2-D4 ensure that Q3 conducts all the regulator current when the wall unit is plugged in by separating the two gate voltages by about 2V.

R14 acts as a current sense for the regulator. The regulator latches off at 3A when the voltage drop between the second Drain Sense Input, pin-8, and the supply, pin-6, rises above 100mV. R10 and C3 provide a short delay. The µP can restart the regulator by turning the second input, pin-5, off and then back on.

The regulator is switched off by the µP when the battery voltage drops below 4.6V. The standby current for the 5V, 2A regulator is less than 10µA. The regulator is switched on again when the battery voltage rises during charging.

Power dissipation in the notebook computer itself is generally quite low. The current limited wall unit dissipates the bulk of the power created by quick charging the battery pack. Q2 dissipates less than 0.5W. R9 dissipates about 0.7W. Q4 dissipates about 2W for a very short period of time when the batteries are fully charged and dissipates less than 0.5W as soon as the battery voltage drops to 5V. The three integrated circuits shown are micropower and dissipate virtually no power. Q3, however, can dissipate as much as 7W if the full 2A output current is required while powered from the wall unit.

The circuit shown in Figure 21 consumes very little board space. The LTC1155 is available in an 8-pin SO package and the three power MOSFETs can also be housed in SO packaging. Q3 and Q4 must be heat sinked properly however. (Consult the MOSFET manufacturer data sheet for surface mount heat sink recommendations).

The LTC1155 allows the use of inexpensive N-channel MOSFET switches to directly connect power from a 4-cell NiCad battery pack to the charger and the load. This technique is very cost effective and is also very efficient. Nearly all the battery power is delivered directly to the load to ensure maximum operating time from the batteries.

POWER SUPPLIES FOR PALMTOP COMPUTERS

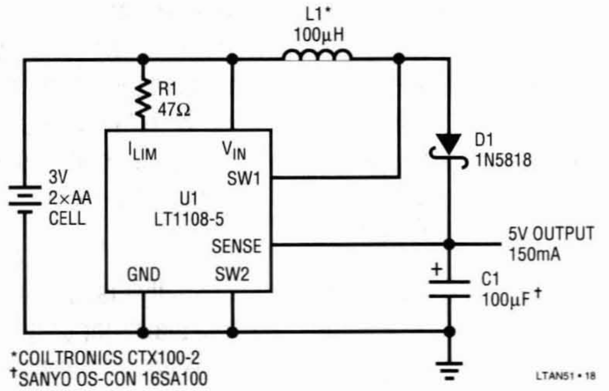
Palmtop computer power supply designs present an entirely separate set of problems from notebook computers. Notebook machines typically use a 9V to 15V NiCad stack for the power source. Palmtop machines, due to their extremely small size, have room for only two or four AA cells. The palmtop machines require much longer operating time in sleep mode, since they presently do not have disk drives. A typical palmtop system may have several hours of operating life with the processor at full activity, tens of hours of quiescent operation with the processor shutdown but the display active, and up to two months life in sleep mode where all memory is retained but no computation takes place. Palmtop machines also use a lithium battery for backup power when the AA cells are dead or being replaced.

The power source for palmtops are usually disposable AA alkaline cells. The use of these disposable batteries generates a separate set of problems from notebook computers. Unlike power supply systems powered by rechargeable NiCad or NiMH batteries, high efficiency power converter circuits are not necessarily optimum for use with disposable batteries. Since rechargeable batteries have very low output impedance, the most efficient converter circuits result in maximum operating time.

Disposable cells, on the other hand, have relatively high internal impedance, so maximum battery life results when the battery load is low and relatively constant. Power supply converters that minimize both the loss in the converter circuit and minimize the effect of battery internal resistance will give longest system operating life. Some of the 4-cell designs presented here are optimized for low peak battery current to lengthen the disposable battery life. Other configurations, while they may have higher efficiency, require higher peak energy demands on the battery and consequently shorten the battery life. The converter circuits shown here have been tested using alkaline AA cells and provide long battery life.

2-Cell Input Palmtop Power Supply Circuits

A regulated 5V supply can be generated from two AA cells using the circuit shown in Figure 22. U1, an LT1108-5 micropower DC to DC converter, is arranged as a step-up, or "boost" converter. The 5V output, monitored by U1's SENSE pin, is internally divided down and compared to a 1.25V reference voltage inside the device. U1's oscillator turns on when the output drops below 5V, cycling the switching transistor at a 19kHz rate. This action alternately causes current to build up in L1, then dump into C1 through D1, increasing the output voltage. When the output reaches 5V, the oscillator turns off.



*COILTRONICS CTX100-2
†SANYO OS-CON 16SA100

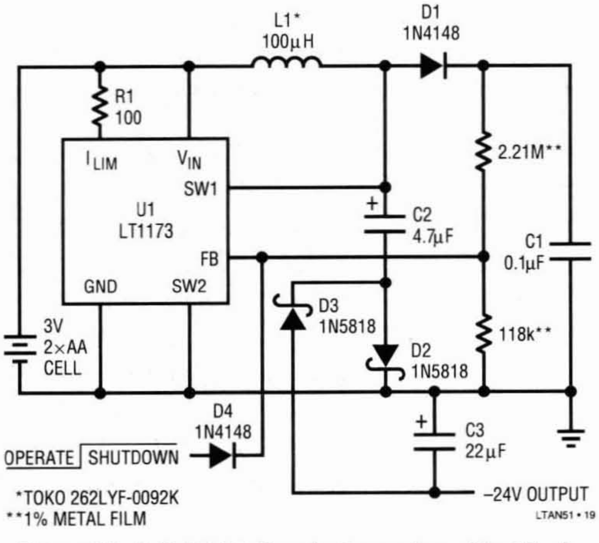
Figure 22. 2 AA Cells to 5V Deliver 150mA

The gated oscillator provides the mechanism to keep the output at a constant 5V. R1 invokes the current limit feature of the LT1108, limiting peak switch current to approximately 1A. U1 limits switch current by turning off the switch when the current reaches the programmed limit set by R1. Switch "on" time, therefore, decreases as V_{IN} is increased. Switch "off" time is not affected. This scheme keeps peak switch current constant over the entire input voltage range, allowing minimum energy transfer to occur at low battery voltage without exceeding L1's maximum current rating at high battery voltage. Maximum current demands should be carefully considered, with R1 tailored to the individual application to obtain longest possible battery life. For example, if only 75mA maximum is required, R1 can be increased to 100Ω. This will limit switch current to approximately 650mA which has the effect of increasing converter efficiency and lowering peak current demands, considerably extending battery life.

The circuit delivers 5V at up to 150mA from an input range of 3.5V to 2.0V. Efficiency measures 80% at 3.0V, decreasing to 70% at 2.0V for load currents in the 15mA to 150mA range. Output ripple measures $75mV_{P-P}$ and no-load quiescent current is just 135µA.

LCD Bias from 2 AA Cells

A –24V LCD bias generator is shown in Figure 23. In this circuit U1 is an LT1173 micropower DC to DC converter. The 3V input is converted to +24V by U1's switch, L1, D1, and C1. The switch pin (SW1) then drives a charge pump consisting of C2, C3, D2, and D3 to level shift the +24V output to -24V. Line regulation is less than 0.2% from 3.3V to 2.0V inputs. Load regulation measures 2% from a 1mA to 7mA load. The circuit delivers up to 7mA from a 2.0V input at 73% efficiency.



*TOKO 262LYF-0092K
**1% METAL FILM

Figure 23. 2-Cell LCD Supply Generates –24 at 7mA

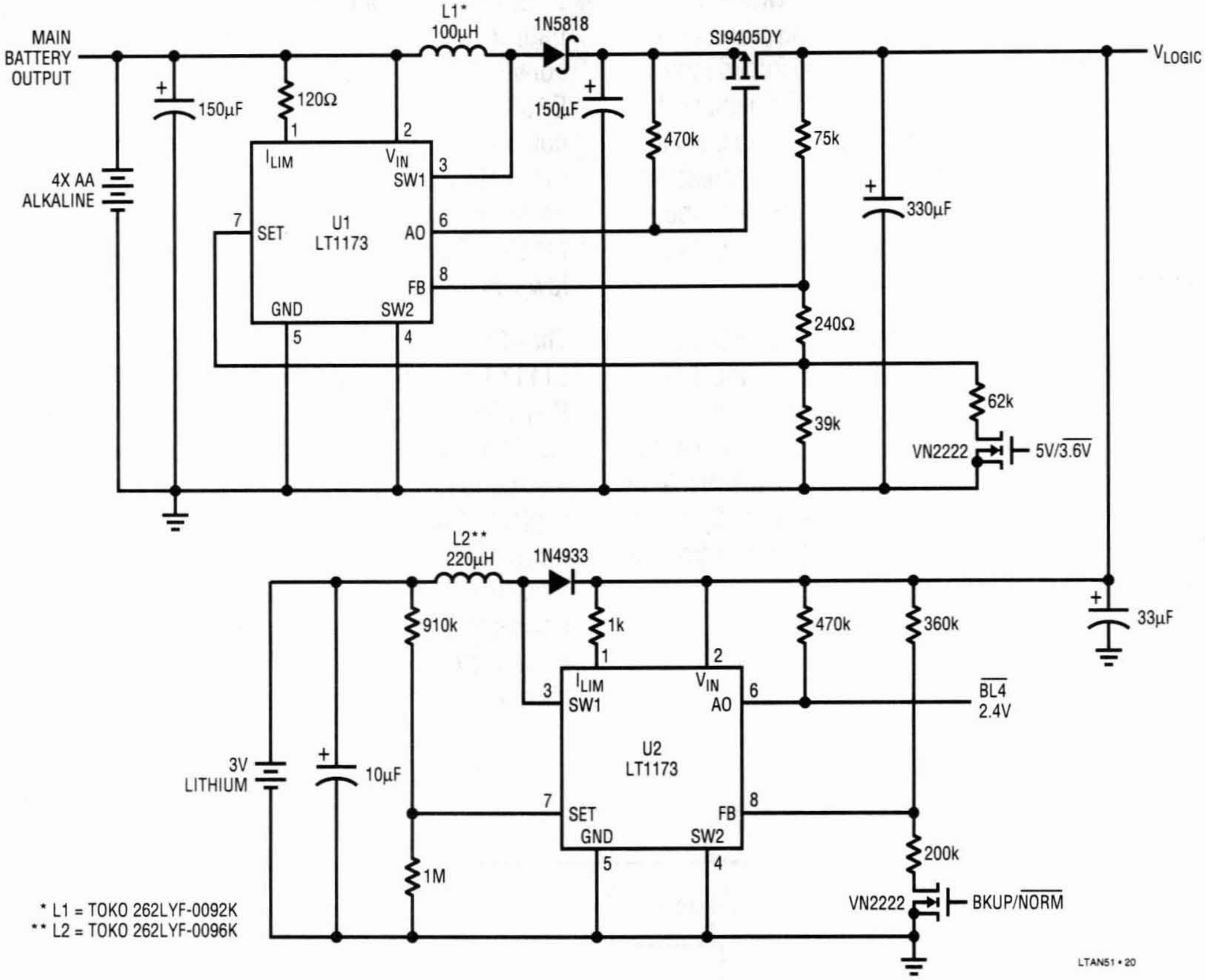

MAIN BATTERY OUTPUT
L1*
100µH
1N5818
SI9405DY
VLOGIC
150µF
120Ω
150µF
470k
75k
330µF
4X AA ALKALINE
ILIM
VIN
SW1
SET
U1
LT1173
AO
FB
GND
SW2
240Ω
62k
39k
VN2222
5V/3.6V
L2**
220µH
1N4933
910k
1k
470k
360k
33µF
ILIM
VIN
SW1
AO
BL4
2.4V
3V LITHIUM
10µF
U2
LT1173
SET
FB
GND
SW2
200k
1M
VN2222
BKUP/NORM
* L1 = TOKO 262LYF-0092K
** L2 = TOKO 262LYF-0096K
LTAN51 • 20

Figure 24. Main Logic Converter Generates 3.6V/5V at 200mA; Backup Converter Generates 3.4V when Main Battery is Dead or Removed

4-Cell Input Palmtop Power Supply Circuits

Newer, more powerful palmtop machines using 386SX processors require more power than two AA cells can deliver for reasonable operating life. The circuits shown here provide a switchable 3.6V/5V output for main logic, a –23V output for LCD display bias, a +12V output for Flash memory V_{PP} generation, and an automatic backup supply using a 3V lithium cell. Under no-load conditions, the quiescent current required by the entire system is 380µA.

The main converter circuit shown in Figure 24 is a combination step-up/step-down converter. When the 4 AA cells are fresh, the circuit behaves as a linear regulator. While this may seem to be inefficient, note that the battery voltage normally quickly drops from 6V to 5V. At 5V input, the efficiency is 3.6V/5V or 72%. As battery voltage drops further, efficiency increases, reaching over 90% at 4.2V input. When the battery drops below 4V, the circuit switches over to step-up mode, squeezing every bit of available energy out of the battery.

The converter delivers 200mA at 3.6V with as little as 2.5V input. In step-up mode, efficiency runs between 83% and 73% (at $2.5V_{IN}$). The linear regulator has no current spikes. AA alkaline cells have a fairly high internal impedance, and the current spikes that switching regulators demand from the battery reduces battery life. A 4-cell AA alkaline battery has an impedance of about 0.5Ω when fresh, increasing to 2Ω at end-of-life. This topology delivers over 9.3 hours of 3.6V, 200mA output power, compared to just 7 hours using a flyback topology.

A backup function is implemented with another LT1173 circuit also shown in Figure 24. Power for the LT1173 comes from the main logic output. The lithium battery sees a load consisting of the 10µF capacitor leakage, switch leakage, and about 1.5µA due to the 910k/1M resistor divider. The total load is less than 5µA. The LT1173 requires 110µA quiescent current, taken from the main logic supply line.

When the BACKUP/NORMAL input goes high, the feedback string is connected, but the converter does not cycle until the main logic supply voltage drops to 3.4V. This converter is capable of supplying 3.6V at 10mA. If the BACKUP/NORMAL signal is driven from Figure 27's circuit, the backup converter will automatically kick in when the main AA cells are removed or dead. A low-battery detector function is provided using the gain block inside the LT1173. The 910k/1M divider set the BL4 output to go low when V_{BATT} equals 2.4V.

The –24V LCD bias generator, shown in Figure 25, uses the LT1173 as a controller driving the FZT749, a 2A PNP in a SOT-223 package. The LT1173 maintains 1.25V between its FB pin and its GND pin. Current must flow through the 3M resistor to force 1.25V across R1. This forces the "GND" pin negative. The 220µH inductor limits switch current to 500mA from a fresh battery and 300mA from a dead (3.6V) battery. Efficiency of this converter is in the 70% range. Higher efficiency can be obtained merely by decreasing the value of the inductor; however, this will actually DECREASE battery life due to the higher current spikes drawn from the battery.

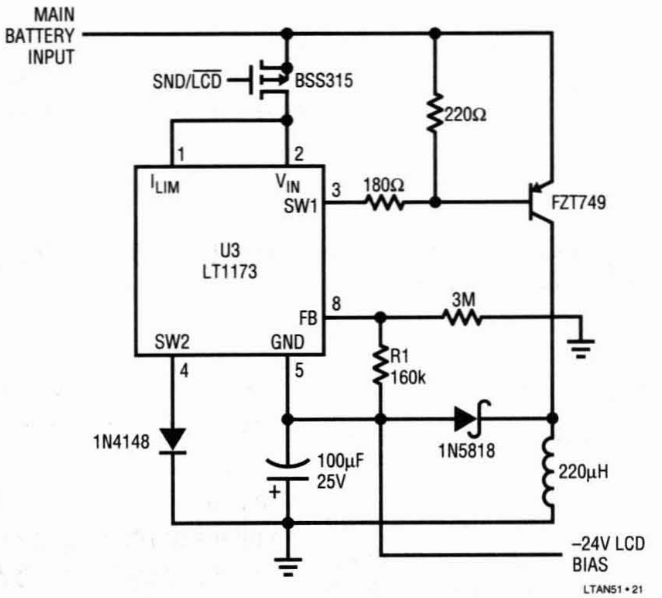


Figure 25. LCD Bias Generator Delivers –24V at 10mA

A Flash memory VPP generator is shown in Figure 26. Up to 40mA at 12V is available from the output. The converter is switched on and off via the small N-channel MOSFET connected to the 124k feedback resistor. When the MOSFET is turned on, the resistor is connected to ground and the converter generates 12V. When the MOSFET is off, the 124k resistor is disconnected and the feedback pin floats high, turning off the converter. When off, output voltage sits at battery voltage minus a diode drop. This condition is approved for Flash memory. Inadvertent programming cannot occur as the Flash chip contains a level detector. When the VPP pin voltage is less than 11.4V, the Flash chip itself will not allow programming to take place. Another low-battery detect function is provided using the LT1173's gain block. The main alkaline battery is being sensed here, and the AO pin goes low when the battery voltage falls below 4.0V.

Finally, a micropower two-terminal reference and dual comparator form a pair of battery detectors. The upper comparator in Figure 27 senses the main battery directly. When the battery voltage falls below 2.5V (a very dead battery!) or the battery is removed, BL3 will go high. If connected to the BACKUP/$\overline{\text{NORMAL}}$ signal of the lithium backup converter, the backup will take over the main logic supply line automatically. The other comparator goes low when the battery voltage falls below 3.6V.

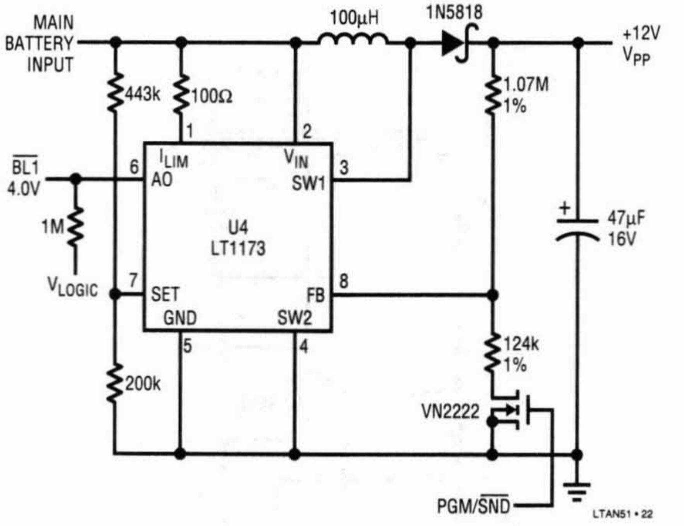

MAIN BATTERY INPUT
100μH
1N5818
+12V
V_{PP}
443k
100Ω
1.07M 1%
1
2
$\overline{BL1}$ 4.0V
6
I_{LIM}
AO
V_{IN}
SW1
3
U4
LT1173
+
47μF 16V
1M
V_{LOGIC}
7
SET
GND
FB
SW2
8
5
4
124k 1%
200k
VN2222
PGM/$\overline{SND}$
LTAN51 • 22

Figure 26. Flash Memory VPP Generator Delivers 12V, 40mA from 4 AA Input

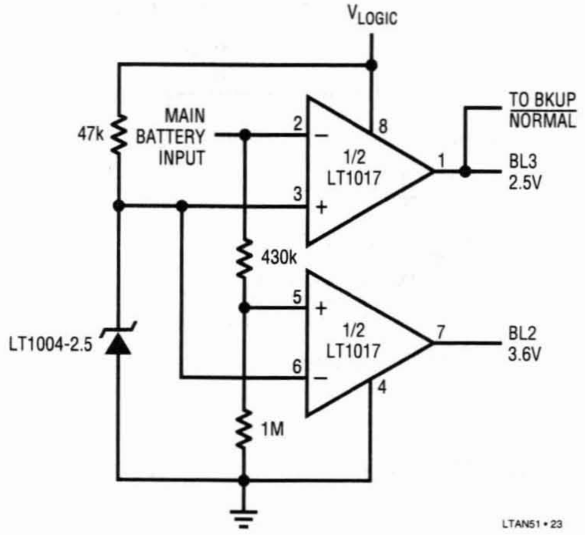
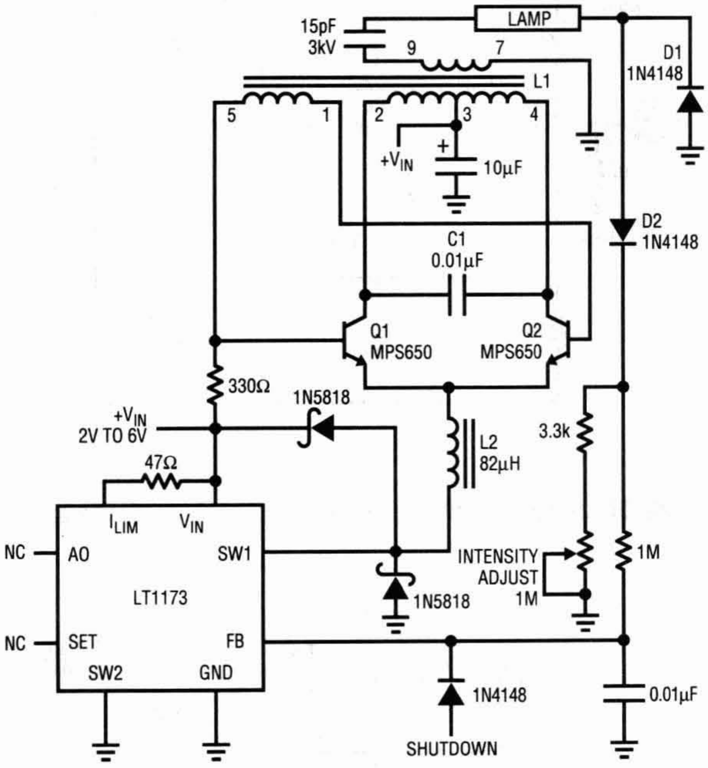

V_{LOGIC}
47k
MAIN BATTERY INPUT
2
–
8
1/2 LT1017
1
3
+
TO BKUP $\overline{\text{NORMAL}}$
BL3 2.5V
430k
5
+
1/2 LT1017
7
BL2 3.6V
LT1004-2.5
6
–
4
1M
LTAN51 • 23

Figure 27. Battery Detectors Sense Removal of Main Battery, Indicate $V_{BATT} < 3.6V$

A CCFL Backlight Driver for Palmtop Machines

Backlit displays have greatly enhanced user acceptance of portable computers. Palmtop machines have not used backlit displays because of the high power required by the inverter circuit used to drive the bulb. Figure 28's circuit, a micropower CCFL supply, overcomes this problem. A typical notebook CCFL supply drives the bulb at 5mA. This circuit, using an LT1173 micropower DC to DC converter, operates over an input range of 2.0V to 6V. Maximum bulb current is limited to 1mA. Control over bulb current is maintained down to 1µA, a very dim light! It is intended for palmtop applications where the longest possible battery life is desired.

L1, Q1, and Q2 comprise a current driven Royer class converter which oscillates at a frequency primarily set by L1's characteristics (including its load) and the 0.01µF capacitor. This entire converter is gated on and off by the burst mode operation of the LT1173. The 1M/0.01µF RC at the LT1173 feedback pin filters the half-sine appearing at the 3.3k-1M potentiometer chain. This signal represents 1/2 the lamp current. The LT1173 servos the energy in the lamp to maintain 1.25V at its feedback pin, closing a loop. For low bulb currents, the LT1173 idles most of the time, drawing only 110µA quiescent current. At the 1mA maximum bulb current, the circuit draws less than 100mA. A substantial amount of light is emitted by the bulb at an input current drain of less than 5mA.


15pF
3kV
LAMP
9
7
L1
D1
1N4148
5
1
2
3
4
+V_IN
10µF
D2
1N4148
C1
0.01µF
Q1
MPS650
Q2
MPS650
330Ω
1N5818
+V_IN
2V TO 6V
47Ω
L2
82µH
3.3k
I_LIM
V_IN
NC
AO
SW1
LT1173
INTENSITY
ADJUST
1M
1N5818
1M
NC
SET
FB
SW2
GND
1N4148
0.01µF
SHUTDOWN

C1 = MUST BE A LOW LOSS CAPACITOR.
METALIZED POLYCARB
WIMA FKP2 (GERMAN) RECOMMENDED.
L1 = SUMIDA-6345-020 OR COILTRONICS-CTX110092-1.
PIN NUMBERS SHOWN FOR COILTRONICS UNIT
L2 = TOKO 262LYF-0091K
DO NOT SUBSTITUTE COMPONENTS

LTAN51 • 24

Figure 28. Micropower CCFL Driver Delivers Up to 1mA of Bulb Current from 2 AA Cells

Application Note 52

January 1993

Linear Technology Magazine Circuit Collection, Volume 1

Richard Markell, Editor

INTRODUCTION

Over the past several years *Linear Technology*, the magazine, has come of age. From nothing, the publication has come into its own, as has its subscriber list. Many innovative circuits have seen the light of day in the pages of our now hallowed publication.

This Application Note is meant to consolidate the circuits from the first few years of the magazine in one place. Circuits herein range from laser diode driver circuits to data acquisition systems to a 50W high efficiency switcher circuit. Enough said. I'll stand aside and let the authors explain their circuits.

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A to D Converters

LTC1292: 12-BIT DATA ACQUISITION CIRCUITS

by Sammy Lum

Temperature-Measurement System

The circuit in Figure 1 shows how a transducer output, such as a platinum RTD bridge, can be digitized with one op amp. This circuit is a modification of that found in Application Note 43.[1] The differential input of the LTC1292 removes the common mode voltage. The LT1006 is used for amplification. The resistor tied between the + input of the LT1006 and the +IN input of the LTC1292 is to compensate for the loading of the bridge by resistor R_S. Full scale can be adjusted by the 500kΩ trim pot and offset can be adjusted by the 100Ω trim pot in series with R_S. A lower R_{PLAT} value than that in AN43 is used here to improve dynamic range. The signal voltage on the +IN pin must not exceed V_{REF}. The differential voltage range is V_{REF} minus approximately 100mV. This is enough range to measure 0°C to 400°C with 0.1°C resolution.

Floating, 12-Bit Data Acquisition System

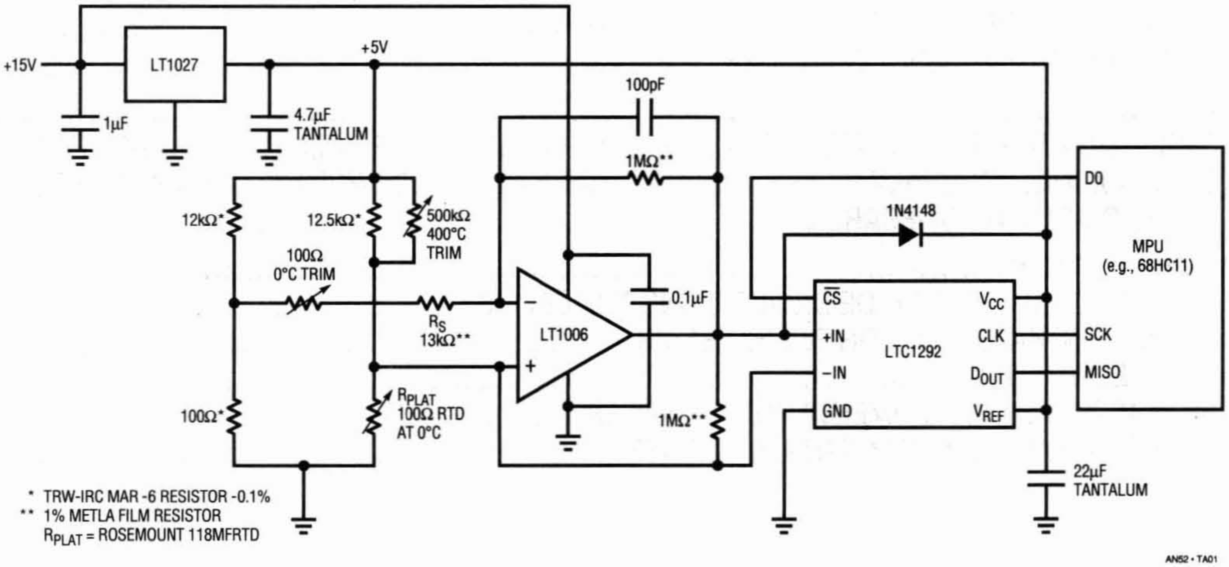
The circuit in Figure 2 demonstrates how to float the LTC1292 to make a differential measurement. This circuit will digitize a 5V range from 10V to 15V with 12 bits of resolution. The digital I/O has been level translated. The LT1019-5 is used in shunt mode to create the floating analog ground for the LTC1292. The digital I/O lines make use of 4.3V Zeners to clamp the single-transistor inverters. Opto-isolators can also be used. The floating analog ground should be laid out as a ground plane for the LTC1292. The 47µF bypass capacitor should be tied from the V_{CC} pin to the floating ground plane with minimum lead length and placed as close to the device as possible. Likewise, keep the lead length from the GND pin to the floating ground plane at a minimum (a low-profile socket is acceptable).

Differential Temperature Measurement System

The circuit in Figure 3 digitizes the difference in temperature between two locations. The two LM134s are used as temperature sensors. These are ideally suited for remote applications because they are current output devices. This allows long wires to run from the sensor back to the LTC1292 without any degradation to the signal from the sensor. Resistor R_{SET} sets the current to $1\mu A/°K$. The current is converted to a voltage by the resistor R1 connected from V^- to ground. The reference voltage and resistor were selected to give a change of 0.05°C/LSB. The resolution is given by $°C/LSB = V_{REF}/((4096)(1mA)(R1))$. The maximum temperature at each input is 125°C. Note

---

[1] Williams, Jim, "Bridge Circuits, Marrying Gain and Balance," Application Note 43, Linear Technology Corp.



+15V
LT1027
+5V
1µF
4.7µF TANTALUM
100pF
1MΩ**
12kΩ*
12.5kΩ*
500kΩ 400°C TRIM
100Ω 0°C TRIM
R_S 13kΩ**
0.1µF
LT1006
R_{PLAT} 100Ω RTD AT 0°C
100Ω*
1MΩ**
1N4148
$\overline{CS}$
+IN
–IN
GND
LTC1292
V_{CC}
CLK
D_{OUT}
V_{REF}
D0
MPU (e.g., 68HC11)
SCK
MISO
22µF TANTALUM
* TRW-IRC MAR -6 RESISTOR -0.1%
** 1% METLA FILM RESISTOR
R_{PLAT} = ROSEMOUNT 118MFRTD
AN52 • TA01

Figure 1. 0° to 400°C Temperature-Measurement System that if the temperature on the +IN pin is less than the temperature on the –IN pin, the output will be zero. Because the LTC1292 is being driven from a high source impedance, you should limit the CLK frequency to 100kHz or less.

The software code for interfacing the LTC1292 to the Motorola MC68HC11 or the Intel 8051 is found in the LTC1292 data sheet. The code needs to be modified for the circuit in Figure 2 to account for the inversion introduced by the digital level translators.

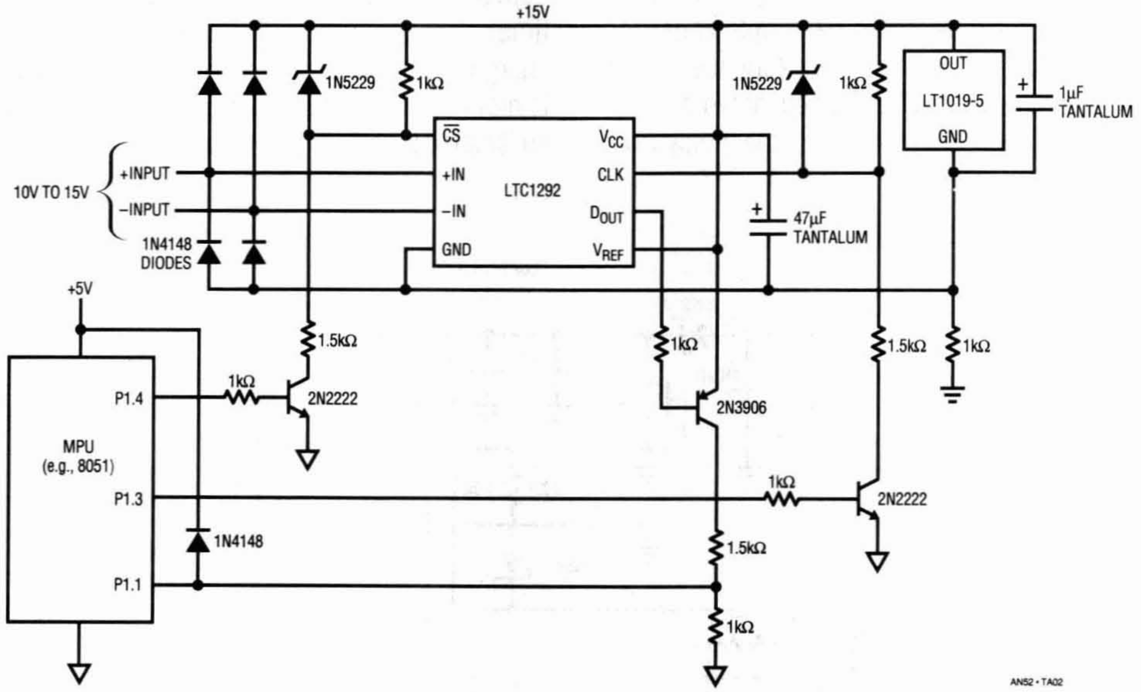
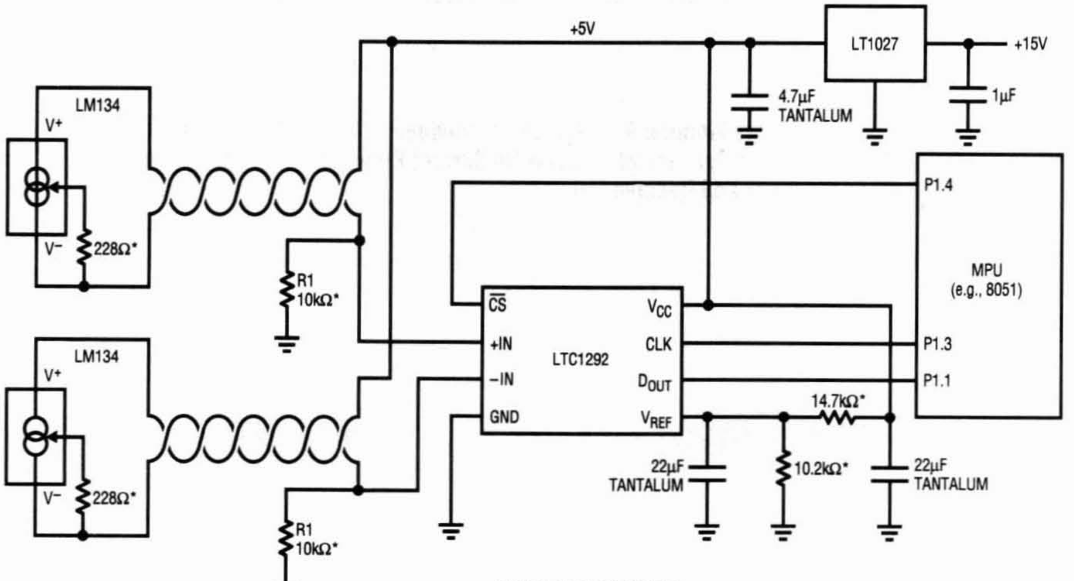

+15V
1N5229
1kΩ
1N5229
1kΩ
OUT
LT1019-5
GND
1µF
TANTALUM
$\overline{CS}$
+IN
–IN
GND
LTC1292
V_{CC}
CLK
D_{OUT}
V_{REF}
10V TO 15V
+INPUT
–INPUT
1N4148
DIODES
47µF
TANTALUM
+5V
1.5kΩ
1kΩ
1.5kΩ
1kΩ
1kΩ
2N2222
2N3906
MPU
(e.g., 8051)
P1.4
P1.3
P1.1
1N4148
1kΩ
2N2222
1.5kΩ
1kΩ
AN52 • TA02

Figure 2. Floating, 12-Bit Data Acquisition System


+5V
LT1027
+15V
4.7µF
TANTALUM
1µF
LM134
V+
V–
228Ω*
R1
10kΩ*
LM134
V+
V–
228Ω*
R1
10kΩ*
$\overline{CS}$
+IN
–IN
GND
LTC1292
V_{CC}
CLK
D_{OUT}
V_{REF}
MPU
(e.g., 8051)
P1.4
P1.3
P1.1
14.7kΩ*
22µF
TANTALUM
10.2kΩ*
22µF
TANTALUM
AN52 • TA03

*1% METAL FILM RESISTOR

Figure 3. Differential Temperature-Measurement System

MICROPOWER SO8 PACKAGED ADC CIRCUITS

by William Rempfer

Floating 8-Bit Data Acquisition System

Figure 4 shows a floating system that sends data to a grounded host system. The floating circuitry is isolated by two opto-isolators and powered by a simple capacitor-diode charge pump. The system has very low power requirements because the LTC1096 shuts down between conversions and the opto-isolators draw power only when data is being transferred. The system consumes only 50µA at a sample rate of 10Hz (1ms on-time and 99ms off-time). This is easily within the current supplied by the charge pump running at 5MHz. If a truly isolated system is required, the system's low power simplifies generating an isolated supply or powering the system from a battery.

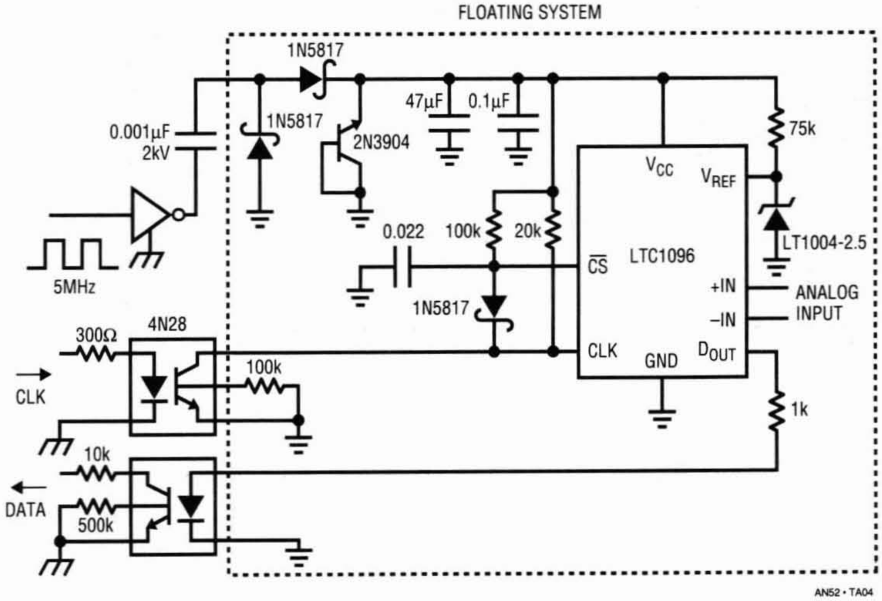

FLOATING SYSTEM
1N5817
47µF
0.1µF
0.001µF
2kV
1N5817
2N3904
75k
V_{CC}
V_{REF}
LT1004-2.5
0.022
100k
20k
$\overline{CS}$
LTC1096
+IN
–IN
ANALOG
INPUT
5MHz
1N5817
300Ω
4N28
CLK
100k
CLK
GND
D_{OUT}
1k
10k
DATA
500k
AN52 • TA04

Figure 4. Power for this Floating ADC System is Provided by a Simple Capacitor-Diode Charge Pump. The Two Opto-Isolators Draw No Current Between Samples, Turning on Only to Send the Clock and Receive Data

0°C – 70°C Thermometer

Figure 5 shows a temperature-measurement system. The LTC1096 is connected directly to the low cost silicon temperature sensor. The voltage applied to the V_{REF} pin adjusts the full scale of the ADC to the output range of the sensor. The zero point of the converter is matched to the zero output voltage of the sensor by the voltage on the LTC1096's negative input.

Operating the ADC directly off batteries can eliminate the space taken by a voltage regulator. Connecting the ADC directly to sensors can eliminate op amps and gain stages. The LTC1096/LTC1098 can operate with small, 0.1µF or 0.01µF chip bypass capacitors.

Figure 6 shows the operating sequence of the LTC1096. The converter draws power when the $\overline{\text{CS}}$ pin is low and shuts itself down when that pin is high. In systems that convert continuously, the LTC1096/LTC1098 will draw its normal operating power continuously. A 10µs wake up time must be provided to the LTC1096 after each falling $\overline{\text{CS}}$.

In systems that have significant time between conversions, lowest power drain will occur with the minimum $\overline{\text{CS}}$ low time. Bringing $\overline{\text{CS}}$ low, waiting 10µs for the wake up time, transferring data as quickly as possible, and then bringing it back high will result in the lowest current drain.

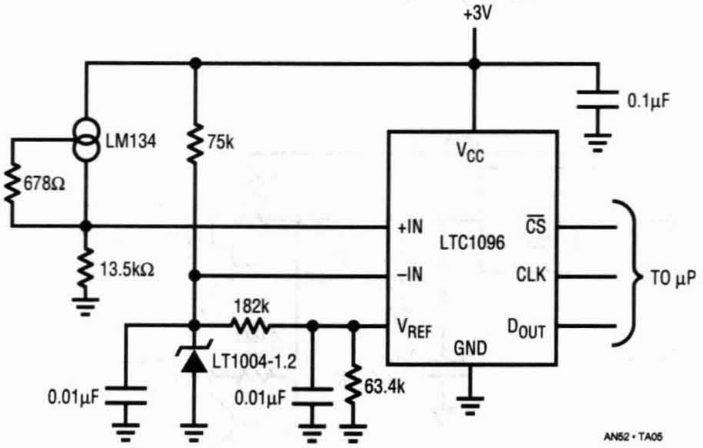

+3V
0.1µF
LM134
75k
678Ω
V_{CC}
+IN
LTC1096
$\overline{\text{CS}}$
13.5kΩ
–IN
CLK
TO µP
182k
V_{REF}
GND
D_{OUT}
LT1004-1.2
0.01µF
0.01µF
63.4k
AN52 • TA05

Figure 5. The LTC1096's High-Impedance Input Connects Directly to this Temperature Sensor, Eliminating Signal Conditioning Circuitry in this 0°C–70°C Thermometer

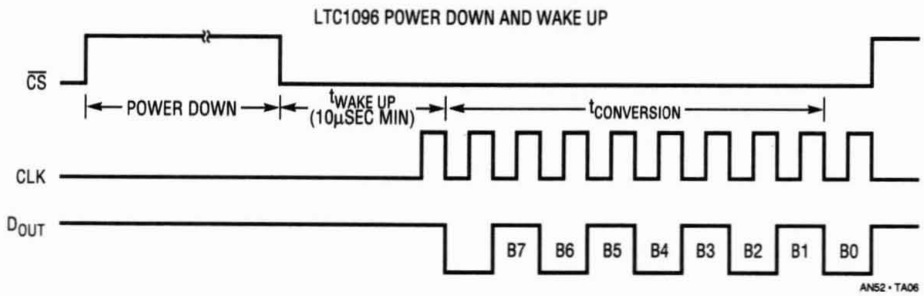

LTC1096 POWER DOWN AND WAKE UP
$\overline{\text{CS}}$
POWER DOWN
$t_{WAKE UP}$ (10µSEC MIN)
$t_{CONVERSION}$
CLK
D_{OUT}
B7
B6
B5
B4
B3
B2
B1
B0
AN52 • TA06

Figure 6. The ADC's Power Consumption Drops to Zero When $\overline{\text{CS}}$ Goes High. 10µs After CS Goes Low, the ADC is Ready to Convert. For Minimum Power Consumption Keep $\overline{\text{CS}}$ High for as Much Time as Possible Between Conversions

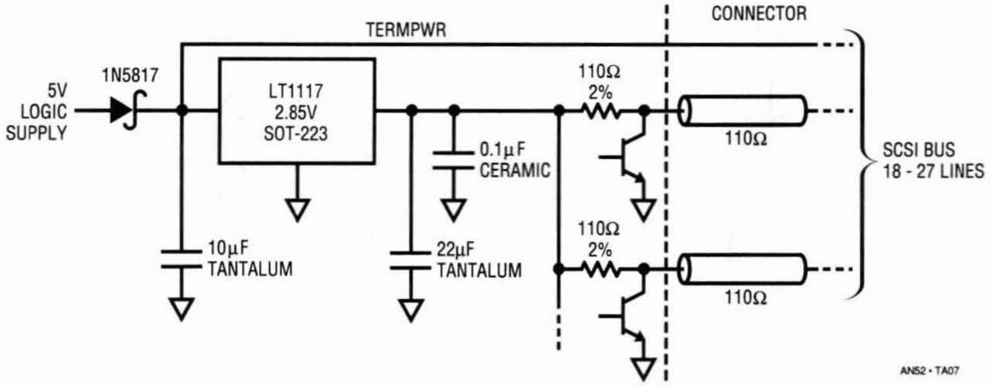
Interface

LOW DROPOUT REGULATOR SIMPLIFIES ACTIVE SCSI TERMINATORS

by Sean Gold

The circuit shown in Figure 7 uses an LT1117 low dropout three terminal regulator to control the terminator's local logic supply. The LT1117's line regulation makes the output immune to variations in TERMPWR. After accounting for resistor tolerances and variations in the LT1117's reference voltage, the absolute variation in the 2.85V output is only 4% over temperature. When the regulator drops out at TERMPWR-2.85, or 1.25V, the output linearly tracks the input with a 1V/V slope. The regulator provides effective signal termination because the 110Ω series resistor closely matches the transmission line's characteristic impedance, and the regulator provides a good AC ground.

In contrast to a passive terminator, two LT1117s require half as many termination resistors, and operate at 1/15 the quiescent current or 20mA. At these power levels, PC traces provide adequate heat sinking for the LT1117's SOT-223 package. Beyond solving basic signal conditioning problems, this LT1117 terminator handles fault conditions with short circuit current limiting, thermal shutdown, and on-chip ESD protection.



CONNECTOR
TERMPWR
5V LOGIC SUPPLY
1N5817
LT1117
2.85V
SOT-223
110Ω
2%
110Ω
0.1µF CERAMIC
SCSI BUS
18 - 27 LINES
110Ω
2%
10µF TANTALUM
22µF TANTALUM
110Ω
AN52 • TA07

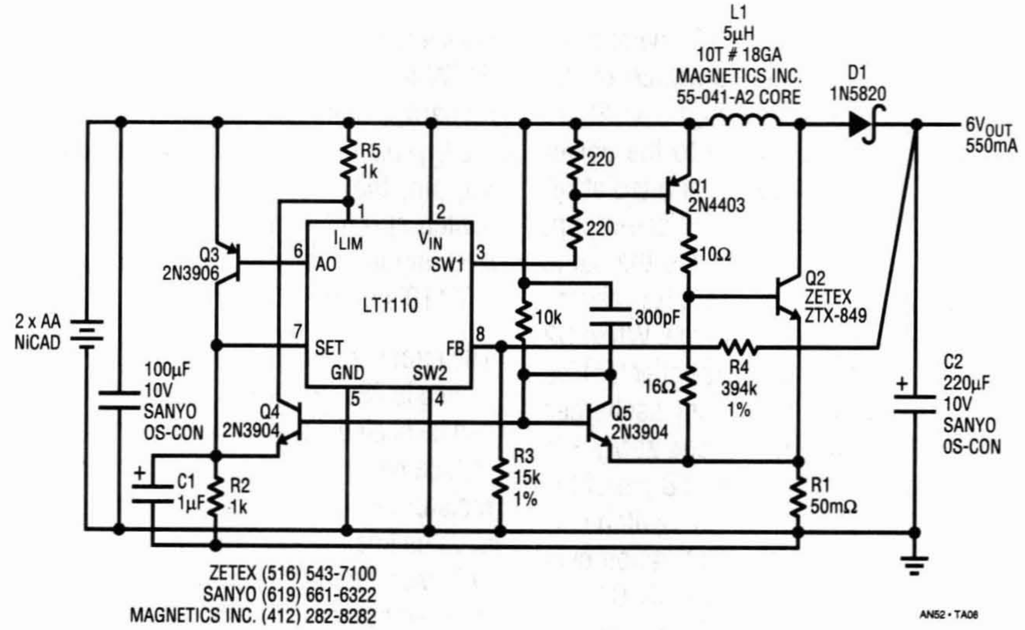
Figure 7. SCSI Active Termination

Power

LT1110 SUPPLIES 6 VOLTS AT 550mA FROM 2 AA NiCAD CELLS

by Steve Pietkiewicz

The LT1110 micropower DC-DC converter can provide 5V at 150mA when operating from two AA alkaline cells. The internal switch $V_{CE(SAT)}$ sets this power limit. Even with an external low drop switch, more power is not realistically possible. The internal impedance (typically 200mΩ fresh and 500mΩ at end-of-life) of alkaline AA cells limits peak obtainable battery power. Conversely, nickel-cadmium cells have a constant internal impedance (35mΩ–50mΩ) for AA size) that increases only when the cell is completely discharged. This allows power to be drawn from the cell at a far greater rate. The circuit in Figure 8 uses two AA NiCad cells to supply 6 volts at 550mA. The circuit, developed for pagers with transmit capability, runs at full output current for 15 minutes with two Gates Millennium AA NiCad cells. With a 250mA load, the circuit runs for 36 minutes (see Figure 9). Less heat is generated with a reduced load, resulting in the watt-hour difference observable above.


L1
5μH
10T # 18GA
MAGNETICS INC.
55-041-A2 CORE
D1
1N5820
6V_OUT
550mA
R5
1k
220
220
Q1
2N4403
10Ω
Q2
ZETEX
ZTX-849
1
2
I_LIM
V_IN
6
AO
SW1
3
LT1110
7
SET
FB
8
GND
SW2
5
4
Q3
2N3906
2 x AA
NiCAD
100μF
10V
SANYO
OS-CON
Q4
2N3904
10k
300pF
R4
394k
1%
16Ω
Q5
2N3904
C2
220μF
10V
SANYO
OS-CON
C1
1μF
R2
1k
R3
15k
1%
R1
50mΩ
AN52 • TA08

ZETEX (516) 543-7100
SANYO (619) 661-6322
MAGNETICS INC. (412) 282-8282

Figure 8. Schematic Diagram, 2 AA NiCad to +6 Volt Converter

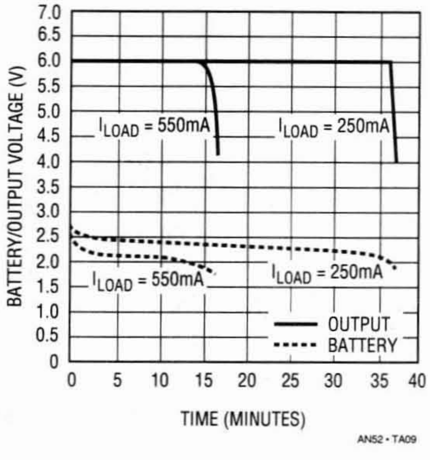


Figure 9. Operating Time at I_{LOAD} = 550mA and 250mA

The circuit uses a micropower LT1110 switching-regulator IC as a controller. The internal switch of the LT1110 furnishes base drive to Q1 through the 220Ω resistors. Q1, in turn, supplies base drive to the power switch Q2. The Zetex ZTX849 NPN device is rated at 5A current and comes in a TO-92 package. For surface-mount fans, the FZT-849, also from Zetex, provides the same performance in an SOT-223 package. The 16Ω resistor provides a turn off path for Q2's stored charge. When Q2 is on, current builds in L1. As Q2 turns off, its collector flies positive until D1 turns on. L1's built-up current discharges through D1 into C2 and the load. The voltage at V_{OUT} is divided by R4 and R3 and fed back into the FB pin of the LT1110, which controls Q2's cycling action. Switch current limit, which is necessary to ensure saturation over supply variations, is implemented by Q3–Q5. Q3, C1, R2, and the auxiliary gain block inside the LT1110, form a 220mV reference point at the LT1110's SET pin. Transistors Q4 and Q5 form a common-base differential amplifier. Q5's emitter monitors the voltage across 50mΩ resistor R1. When the voltage across R1 exceeds 220mV, Q4 turns on hard, pulling current through R5. When the voltage at the I_{LIM} pin of the LT1110 reaches a diode drop below the V_{IN} pin, the internal switch turns off. Thus, maximum switch current is maintained at 220mV/50mΩ, or 4.4A, over input variations and manufacturing spread in the LT1110's on time and frequency.

The circuit's output ripple measures $200mV_{P-P}$, and efficiency is 78% at full load with a 2.4V input. Output power can be scaled down for less demanding requirements. To reduce peak current, increase the value of R1. A 100mΩ resistor will limit current to 2.2A. L1 should be increased in value linearly as current is reduced. For a current limit of 2.2A, L1 should be 10μH. Base drive for Q2 can also be reduced by increasing the value of the 10Ω resistor. These lower peak currents are much easier on alkaline cells and will dramatically increase alkaline battery life.

50 WATT HIGH EFFICIENCY SWITCHER

by Milton Wilcox

The high efficiency 10A step-down (buck) switching regulator shown in Figure 10 illustrates how different sized MOSFETs can be driven by the LT1158 without having to worry about shoot-through currents. Since 24V is being dropped down to 5V, the duty cycle for the switch (top MOSFET) is only 5/24 or 21%. This means that the bottom MOSFET will dominate the $R_{DS(ON)}$ efficiency losses, because it is turned on nearly four times as long as the top. Therefore a smaller MOSFET is used on the top, and the bottom MOSFET is doubled up, all without having to worry about dead time.

The LT1158 uses an adaptive system that maintains dead time independent of the type, the size, and even the number of MOSFETs being driven. It does this by monitoring the gate turn-off to see that it has fully discharged before allowing the opposite MOSFET to turn on. During turn-on, the hold-off capability of the opposing driver is boosted to prevent transient shoot-through. In this way, cross-conduction is completely eliminated as a design constraint.

The non-critical Schottky diode across the bottom MOSFETs reduces reverse-recovery losses. Figure 11 shows the operating efficiency for the Figure 10 circuit.

Switching regulator applications can take advantage of an important protection feature of the LT1158: remote fault sensing. By sensing the current on the output side of the inductor and returning the LT1158 $\overline{\text{fault}}$ pin to the PWM soft-start pin, a true current-mode loop is formed. The Figure 10 circuit regulates maximum current in the inductor to 15A with no output voltage overshoot upon recovery from a short circuit.

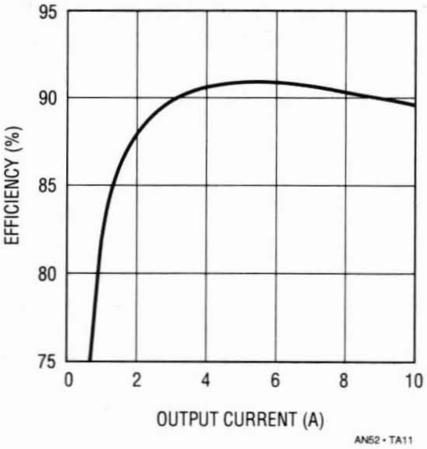


Figure 11. Operating Efficiency for Figure 10 Circuit. Current Limit is Set at 15A

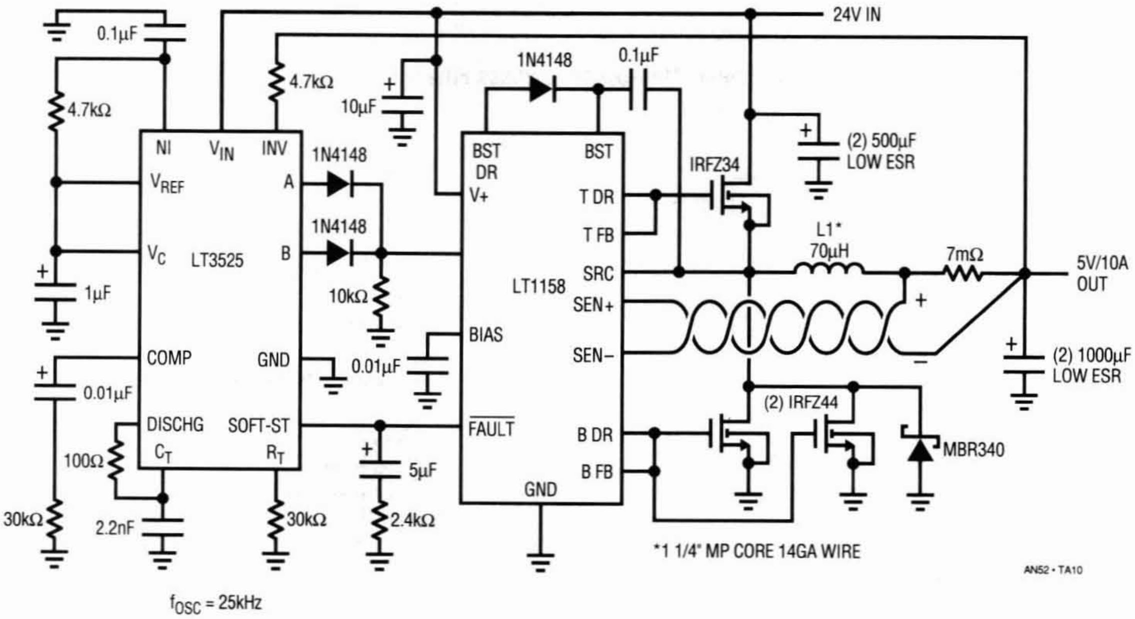

24V IN
0.1µF
4.7kΩ
4.7kΩ
10µF
1N4148
0.1µF
NI
V_{IN}
INV
V_{REF}
A
1N4148
1N4148
V_C
LT3525
B
1µF
10kΩ
COMP
GND
0.01µF
0.01µF
DISCHG
SOFT-ST
C_T
R_T
100Ω
5µF
30kΩ
2.2nF
30kΩ
2.4kΩ
BST
DR
V+
BST
T DR
T FB
SRC
SEN+
SEN–
LT1158
BIAS
$\overline{\text{FAULT}}$
B DR
B FB
GND
IRFZ34
(2) 500µF
LOW ESR
L1*
70µH
7mΩ
5V/10A
OUT
+
–
(2) 1000µF
LOW ESR
(2) IRFZ44
MBR340
*1 1/4" MP CORE 14GA WIRE
AN52 • TA10
f_{OSC} = 25kHz

Figure 10. 50W High Efficiency Switching Regulator Illustrates the Design Ease Afforded by Adaptive Dead Time Generation

CASCADED 8TH-ORDER BUTTERWORTH FILTERS PROVIDE STEEP ROLL-OFF LOWPASS FILTER

by Philip Karantzalis and Richard Markell

Sometimes a design requires a filter that exceeds the specifications of the standard "dash-number" filter. In this case, the requirement was a low-distortion (–70dB) filter with roll-off faster than that of an 8th-order Butterworth. An elliptic filter was ruled out because its distortion specifications are too high. Two low power LTC1164-5s were wired in cascade to investigate the specifications that could be achieved with this architecture. The LTC1164-5 is a low power (4 milliamperes with ±5 volt supplies), clock-tunable, 8th-order filter, which can be configured for a Butterworth or Bessel response by strapping a pin. Figure 12 shows the schematic diagram of the two-filter system. The frequency response is shown in Figure 13, where it can be seen that the filter's attenuation is 80dB at 2.3 times the cutoff frequency. The distortion, as shown in Figure 14, is nothing less than spectacular. From 100Hz to 1kHz, the two filters have less than –74dB distortion specifications. At the standard measurement frequency of 1kHz, the specification is –78dB.

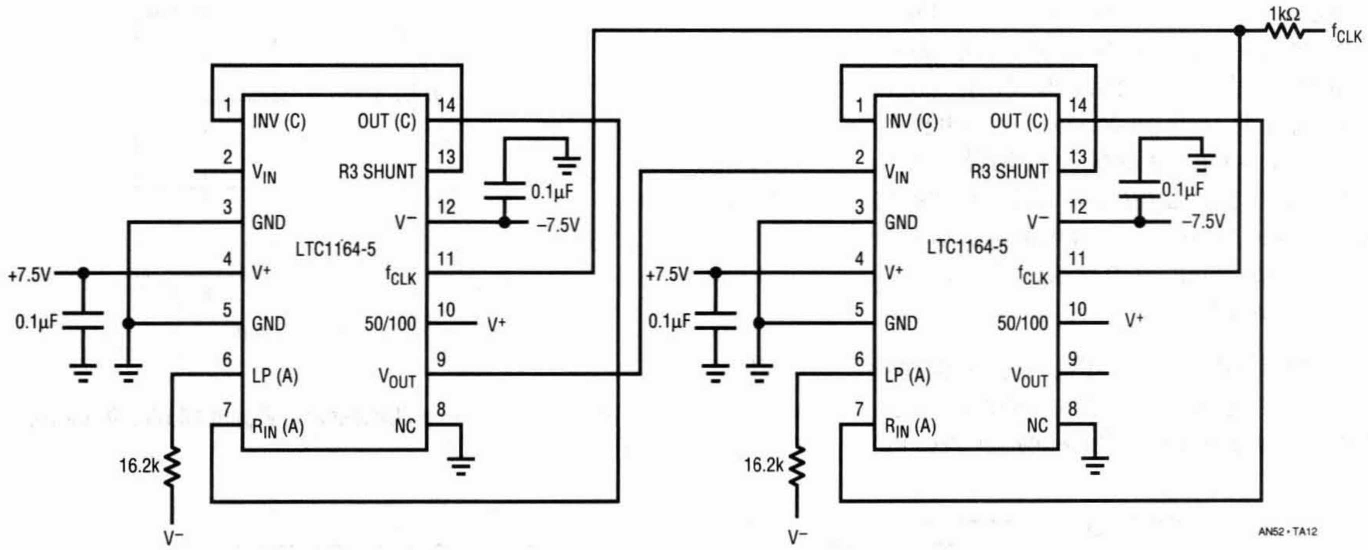


Figure 12. Schematic Diagram: Low Power, 16th-Order Lowpass Filter (Two 8th-Order Butterworths Cascaded)

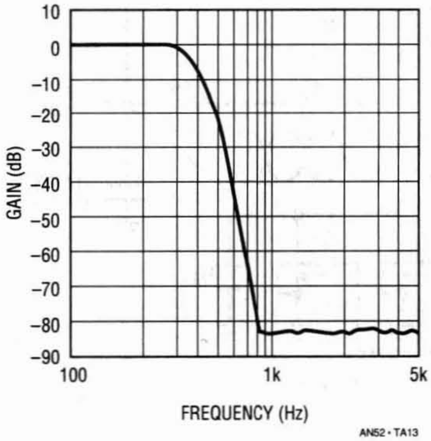


Figure 13. Frequency Response for f_{CLK} = 20kHz

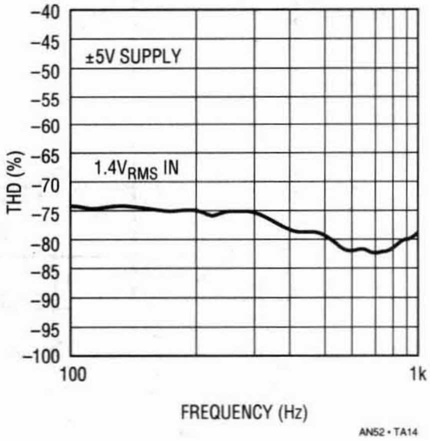


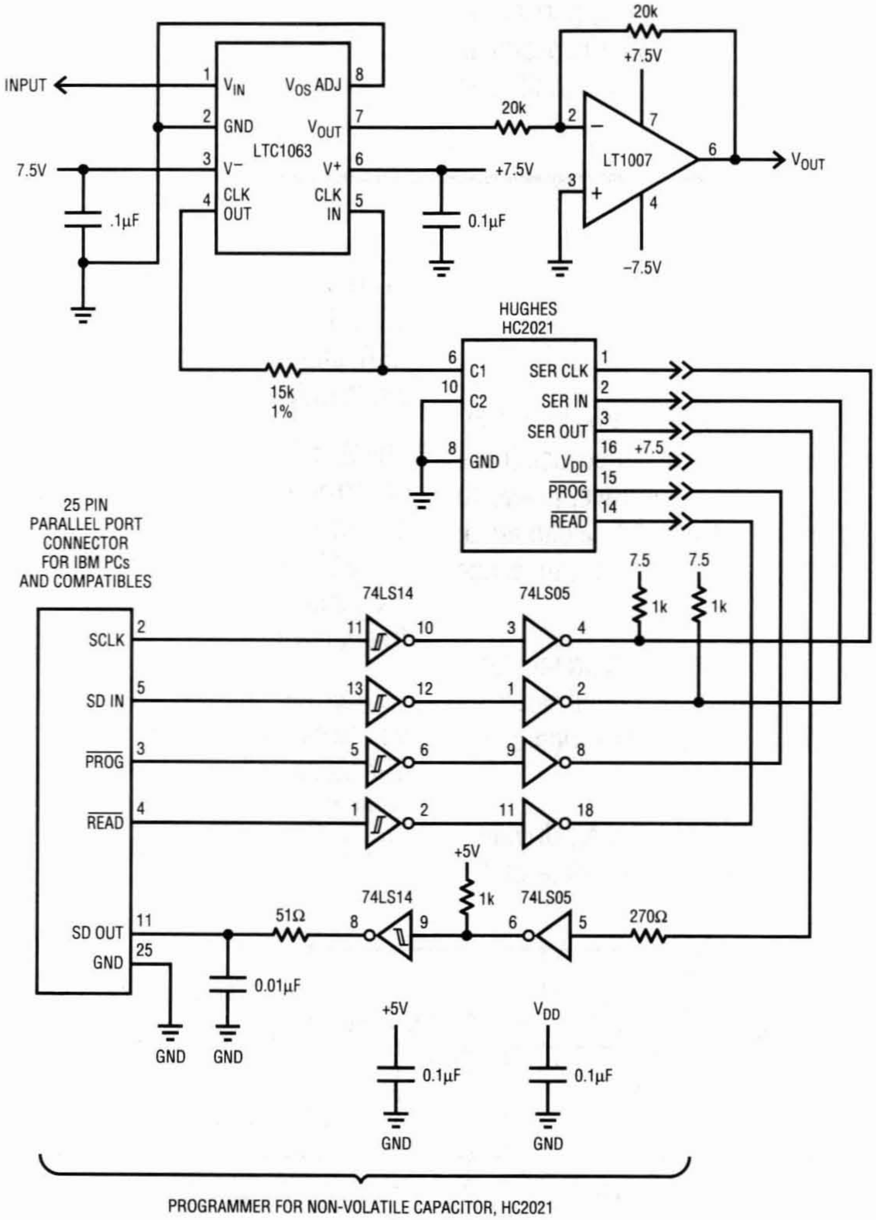
Figure 14. Distortion Performance: Two LTC1164-5s, f_{CLK} = 60kHz (57:1) Pin 10 Connected to V+

DC-ACCURATE, PROGRAMMABLE-CUTOFF, FIFTH-ORDER BUTTERWORTH LOWPASS FILTER REQUIRES NO ON-BOARD CLOCK

by Richard Markell

The new LTC1063 is a clock-tunable, monolithic filter with low-DC output offset (1mV typical with ±5V supplies). The frequency response of the filter closely approximates a fifth-order Butterworth polynomial.

Most users choose to tune the filter with an on-board microprocessor and/or timer. This is quite convenient if these components are available. If a clock is not available, the LTC1063 can be tuned with an external resistor and capacitor. The scheme shown here allows the filter's cutoff frequency to be programmed using an external microprocessor or the parallel port of a personal computer. This allows the cutoff frequency of the filter to be set before the product is shipped.


INPUT
7.5V
.1µF
LTC1063
V_{IN}
GND
V−
CLK OUT
V_{OS} ADJ
V_{OUT}
V+
CLK IN
+7.5V
0.1µF
20k
20k
+7.5V
LT1007
−7.5V
V_{OUT}
15k 1%
HUGHES HC2021
C1
C2
GND
SER CLK
SER IN
SER OUT
V_{DD}
PROG
READ
+7.5
25 PIN PARALLEL PORT CONNECTOR FOR IBM PCs AND COMPATIBLES
SCLK
SD IN
PROG
READ
SD OUT
GND
74LS14
74LS05
7.5
7.5
1k
1k
+5V
1k
51Ω
270Ω
0.01µF
GND
GND
+5V
V_{DD}
0.1µF
0.1µF
GND
GND
PROGRAMMER FOR NON-VOLATILE CAPACITOR, HC2021

NOTES:
1. THE HC2021 SHOULD BE LOCATED CLOSE TO THE LTC1063 FOR BEST RESULTS.
2. $+3.5 \le V_{DD} \le +18.8$.
3. POSITIVE POWER SUPPLY FOR DEVICES 74LS05 AND 74LS14 IS +5V.
4. HUGHES TELEPHONE NUMBER (714) 759-2665.

AN52 • TA15

Figure 15. Schematic Diagram of LTC1063 with Programmable Cutoff Frequency

The tuning scheme makes use of non-volatile, tunable capacitors available from Hughes Semiconductor. These capacitors allow approximately a decade of tuning range. More range could be obtained by using dual devices. Figure 15 shows the schematic diagram of the application. Be sure to place the variable capacitor as close as possible to the LTC1063 to minimize parasitic elements. Figure 16 shows the frequency response of the filter when the capacitor is varied from minimum to half-value, and then to maximum capacitance. The programming part of the circuit may be disconnected once the variable capacitor is set. The capacitor will remember its value until it is reprogrammed.

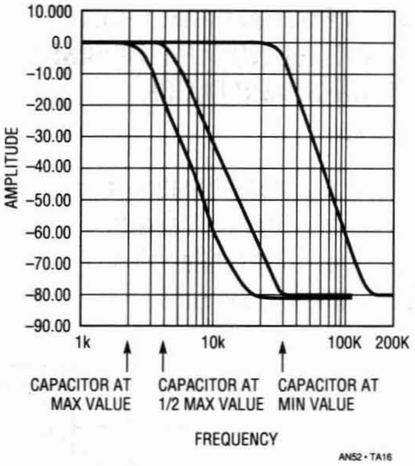


Figure 16. LTC1063 Frequency Response

Miscellaneous Circuits

A SINGLE CELL LASER DIODE DRIVER USING THE LT1110

by Steve Pietkiewicz

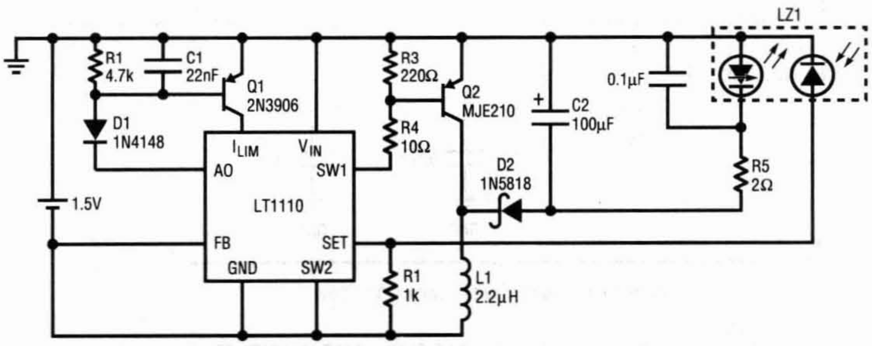
Recently available visible lasers can be operated from 1.5V supplies, given appropriate drive circuits. Because these lasers are exceptionally sensitive to overdrive, power to the laser must be carefully controlled lest it be damaged. Over-currents as brief as 2 microseconds can cause damage.

In the circuit of Figure 17, an LT1110 switching regulator serves as the controller within the single cell powered laser diode driver. The LT1110 regulator is a high speed LT1073.

The LT1110 is used here as an FM controller, driving a PNP power switch Q2, with a typical "ON" time of 1.5 microseconds. Current in L1 reaches a peak value of about 1.0A. The output capacitor C2 has been specified for low ESR, and should not be substituted (damage to the laser diode may result).

The Gain Block output of the LT1110 functions with Q1 as an error amplifier. The differential inputs compare the photodiode current developed as a voltage across R2 to the 212mV reference. The amplifier drives Q1, which modulates current into the I_{LIM} pin. This varies oscillator frequency to control average current.

Overall frequency compensation is provided by R1 and C1, values carefully chosen to eliminate power-up overshoot. The value of current sense resistor R2 determines the laser diode power, as shown the 1000 ohms results in about a 0.8 milliwatt output.



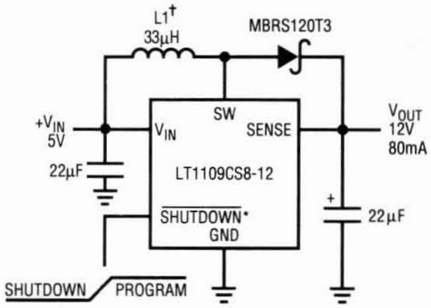
L1 = TOKO 262LYF - 0076K
C2 = SANYO OS-CON
LZ1 = TOSHIBA TOLD9211

Figure 17. LT1110 Laser Diode Driver Operating from a Single Cell

LT1109 GENERATES VPP FOR FLASH MEMORY

by Steve Pietkiewicz

Flash memory chips such as the Intel 28F020 2Megabit device require a VPP program supply of 12 volts at 30mA. A DC-DC converter may be used to generate 12 volts from the 5 volt logic supply. The converter must be physically small, available in surface-mount packaging, and have logic-controlled shutdown. Additionally, the converter must have carefully controlled rise time and zero overshoot. VPP excursions beyond 14 volts for 20ns or longer will destroy the ETOX[2]-process based device.


L1†
33μH
MBRS120T3
SW
+VIN
5V
VIN
SENSE
VOUT
12V
80mA
22μF
LT1109CS8-12
SHUTDOWN*
GND
22μF
SHUTDOWN / PROGRAM

* 8-PIN PACKAGE ONLY
† L1 = COILTRONICS CTX 33-1 OR SUMIDA CD54-330
COILTRONICS (305) 781-8900
SUMIDA (708) 956-0666

AN52 • TA18

Figure 18. All Surface Mount Flash Memory VPP Generator

Figure 18's circuit is well suited for providing VPP power for single or multiple flash memory chips. All associated components, including the inductor, are surface mount devices. The $\overline{\text{SHUTDOWN}}$ input turns off the converter, reducing quiescent current to 300μA when pulled to a logic 0. VPP rises in a controlled fashion, reaching 12 volts ±5% in under 4ms. Output voltage goes to V_{CC} minus a diode drop when the converter is in shutdown mode. This is an acceptable condition for Intel flash memories and does not harm the memory.

RF LEVELING LOOP

by Jim Williams

Leveling loops are often a requirement for RF transmission systems. More often than not, low cost is more important than absolute accuracy. Figure 19 shows such a circuit.

The RF input is applied to A1, an LT1228 operational transconductance amplifier. A1's output feeds A2, the LT1228's current feedback amplifier. A2's output, the output of the circuit, is sampled by the A3-based gain control configuration. This arrangement closes a gain control loop back at A1. The 4pF capacitor compensates rectifier diode capacitance, enhancing output flatness vs frequency. A1's I_{SET} input current controls its gain, allowing overall output level control. This approach to RF leveling is simple and inexpensive, and provides low output drift and distortion.

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[2] ETOX is a trademark of Intel Corporation.

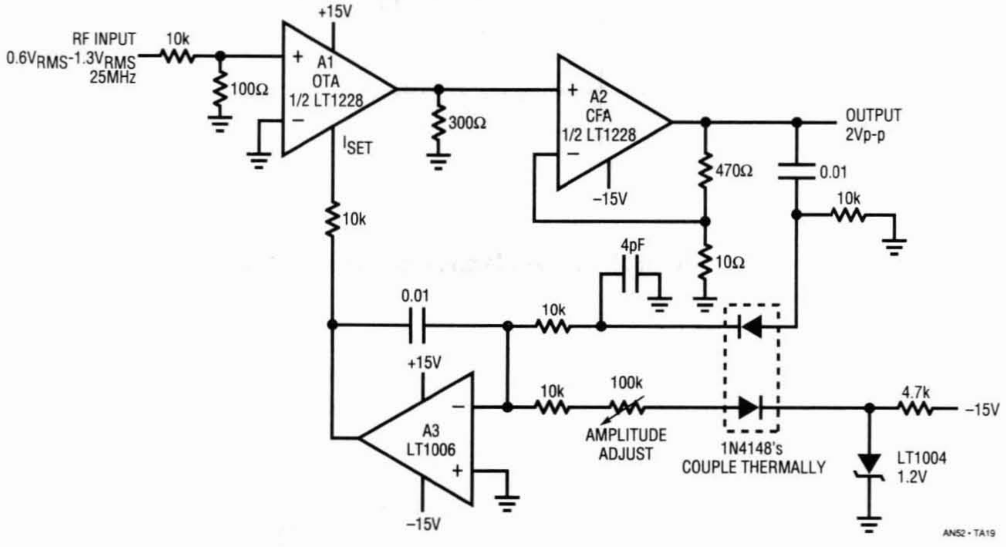

+15V
RF INPUT
0.6VRMS-1.3VRMS
25MHz
10k
100Ω
A1
OTA
1/2 LT1228
ISET
300Ω
A2
CFA
1/2 LT1228
–15V
OUTPUT
2Vp-p
470Ω
0.01
10k
10k
4pF
10Ω
0.01
10k
+15V
A3
LT1006
–15V
10k
100k
AMPLITUDE ADJUST
1N4148's
COUPLE THERMALLY
4.7k
–15V
LT1004
1.2V
AN52 • TA19

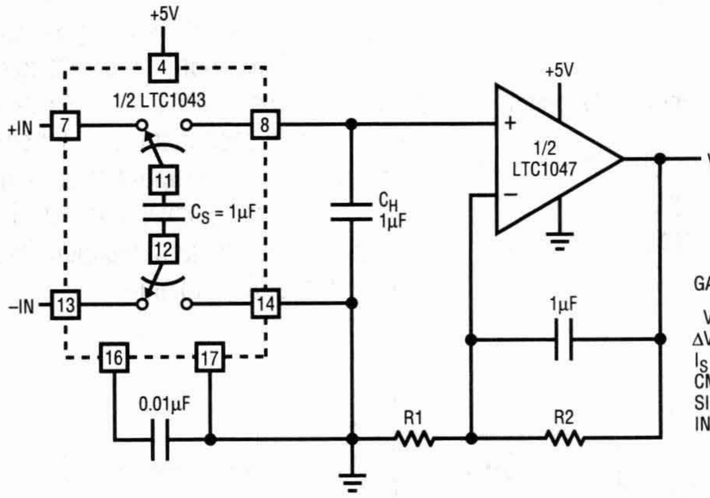
Figure 19. Simple RF Leveling Loop

HIGH ACCURACY INSTRUMENTATION AMPLIFIER

by Dave Dwelley

The LTC1043 and the LTC1047 combine to make a high performance low frequency instumentation amplifier as shown in Figure 20. The LTC1043 switched capacitor block is configured as a sampling front end, providing exceptional CMRR and rail-to-rail input operation. It works by attaching a 1µF capacitor across the two inputs, letting it charge to the input voltage. Once charged, the capacitor is disconnected from the input terminals and reconnected to the output terminals, where it transfers its charge to the 1µF capacitor at the LTC1047's input. Any common mode voltage present at the inputs is subjected to a capacitive divider between the 1µF flying cap and the IC's parasitic capacitance. With the LTC1043's parasitics typically below 1pF, this gives AC CMRR above 120dB. The analog switches in the LTC1043 are purely resistive, so they add no DC offset to the signal.

The output signal (with the common mode stripped off) is then amplified by the LTC1047, a precision, micropower zero-drift op amp. The LTC1047 amplifies the signal by the desired amount, adding less than 10µV offset and 0.05µV/°C drift. The sampling frequency of the LTC1043 with single 5V supply is about 400Hz, allowing differential signals below 200Hz to be amplified with no aliasing. Note that common mode signals are not sampled; thus they will not alias regardless of frequency until the common mode/differential mode signal ratio approaches 120dB! The entire system draws 60µA with a single 5V supply and provides two independent channels.



$\text{GAIN} = 1 + \frac{R2}{R1}$

V_{OS} = 10µV

ΔV_{OS} = 50nV/°C

I_S = 30µA/SIDE

CMRR > 120dB AT 60Hz

SINGLE 5V SUPPLY

INPUT RANGE INCLUDES BOTH SUPPLIES

AN52 • TA20

Figure 20. High Accuracy Instrumentation Amplifier

A FAST, LINEAR, HIGH CURRENT LINE DRIVER

by Walt Jung and Rich Markell

Among linear applications not usually seen are those which require high speed combined with either very low DC error, or high load current. Such applications can be solved by combining the best attributes of two ICs, either one of which may not be capable by itself of the entire requirement.

A case in point is the line driver of Figure 21, which uses an LT1122 JFET input op amp as the gain element combined with an LT1010 buffer. This provides the output current of the LT1010 (typically 150mA) but with the basic DC and low level AC characteristics of the LT1122. The circuit is capable of driving loads as low as 100Ω with very low distortion. The input referred DC error is the low DC offset of the LT1122, typically 0.5mV or less. Large signal characteristics are also very good, due to the 80V/µs symmetrical SR of the LT1122.

The circuit as shown is configured as a precise gain of 5 non-inverting amplifier by gain set resistors R2 and R1, with the LT1010 unity gain voltage follower inside the overall feedback loop. This provides current buffering to the op amp, allowing it to operate most linearly. Small signal bandwidth is set by the time constant of R2 and C1, and is 1MHz as shown, with a corresponding risetime of about 400ns.

Performance with ±18V supplies is shown in Figures 22a and 22b, with output generally $5V_{RMS}$ or equivalent, driving 100Ω directly. THD is shown in Figure 22a, with input level swept up to output clipping level, at a fixed 10kHz frequency. The distortion is generally well below 0.01%, and improves substantially for lower frequencies.

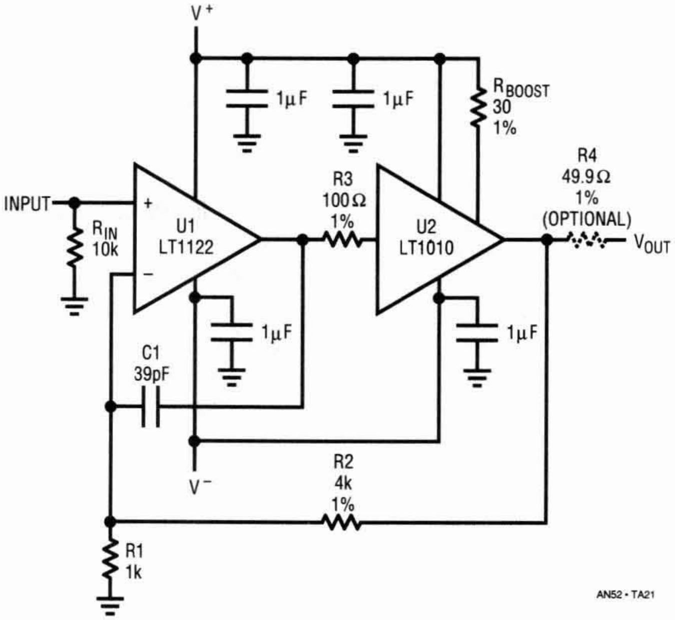


Figure 21. Line Driver

CCIF IM distortion performance of the circuit for similar loading is shown in Figure 22b, driving a load of 100Ω at a swept level, again up to output clipping. The LT1122 amplifier is represented by the lower of the two curves, with distortion around the 0.0001% level. Also shown for comparison in this plot is the distortion of a type 156 JFET op amp (also driving the LT1010 buffer with other conditions the same). The 156 op amp uses a design topology with an intrinsically *asymmetric* SR. This manifests itself as rising even order distortion for methods such as this CCIF test. For this example, the distortion is more than an order of magnitude higher than that of the faster, symmetric slewing LT1122 for the same conditions.

Applications of this circuit include low offset linear buffers such as for A/D inputs, line drivers for instrumentation use, and audio frequency range buffers such as very high quality headphone use.

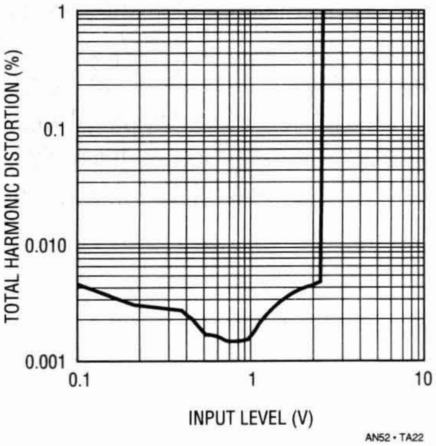


Figure 22a. THD vs Input Level

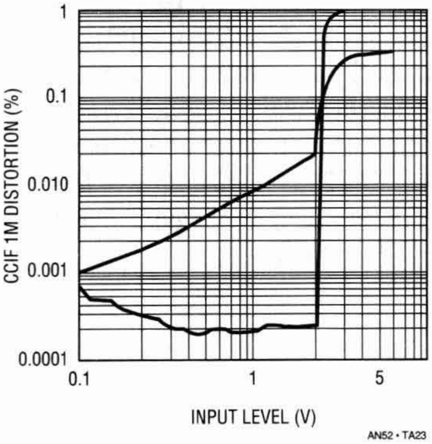


Figure 22b. CCIF IM Distortion vs Input Level

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LINEAR TECHNOLOGY
Application Note 53
January 1993

Micropower High Side MOSFET Drivers

Tim Skovmand

Portable electronic equipment, such as notebook and palmtop computers, portable medical instruments and battery powered tools, are increasingly dependent upon efficient power management to meet the challenge of extracting more useful energy (time) from less battery volume and weight.

One link in the power management chain which has received increasing scrutiny, as power supply efficiencies soar above 90%, is the logic controlled power switch. Large sections of a typical notebook computer system, for example, are powered via topside or "high side" MOSFET switches. These switches can become significant sources of power loss if not properly designed.

At first glance, P-channel MOSFETs appear to be the natural choice for high side switching. Unfortunately, the $R_{DS(ON)}$ exhibited by most P-channels is prohibitively high. (Mother Nature has decreed that electron mobility shall exceed hole mobility in silicon by about 2.5 times, so that a P-channel MOSFET with the same $R_{DS(ON)}$ and voltage rating as its N-channel counterpart is roughly 2 to 3 times larger and more expensive.) Also, the gate drive for a P-channel switch is limited to the supply voltage which may not fully enhance the switch as the supply voltage drops.

N-channel MOSFETs may seem less attractive because they require a gate voltage higher than the power supply voltage to become fully enhanced in high side switching applications. This limitation is eliminated by high side MOSFET drivers such as the LTC1155, which have built-in charge pumps to fully enhance N-channel switches.

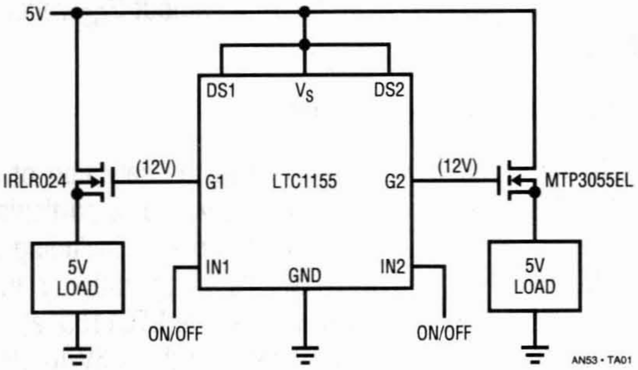


Figure 1. High Efficiency Dual High Side Switch

The LTC1155, dual micropower MOSFET driver, generates 12V from a 5V rail to fully enhance logic-level N-channel switches with no external components required (see Figure 1). Further, the supply current is typically 85μA with the switch fully enhanced and 8μA with the LTC1155 in the standby mode (both inputs off). This combination of low-drop N-channel MOSFET switch and micropower driver is the most efficient means of powering complex electrical loads. Switch efficiencies in the 98% to 99%+ range are easily attained with practical and economic N-channel switches.

MOSFET SWITCH SELECTION

N-channel MOSFET switches fall into two main categories: logic-level and standard.

Logic-Level MOSFET Switches

Although there is some variation among manufacturers, logic-level MOSFET switches are typically rated with $V_{GS} = 4.0V$ with a maximum continuous V_{GS} rating of ±10V. $R_{DS(ON)}$ and maximum V_{DS} ratings are similar to standard MOSFETs and there is generally little price differential. Logic-level MOSFETs are frequently designated by an "L" and are usually available in surface mount packaging.

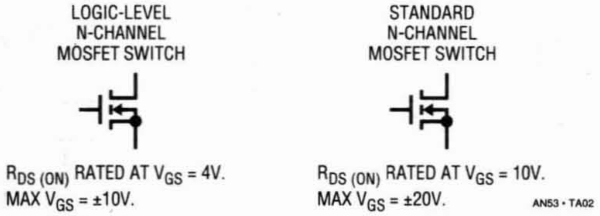

LOGIC-LEVEL N-CHANNEL MOSFET SWITCH
STANDARD N-CHANNEL MOSFET SWITCH
$R_{DS(ON)}$ RATED AT $V_{GS} = 4V$.
MAX $V_{GS} = \pm 10V$.
$R_{DS(ON)}$ RATED AT $V_{GS} = 10V$.
MAX $V_{GS} = \pm 20V$.
AN53 • TA02

Figure 2. Logic-Level and Standard N-channel MOSFET V_{GS} Ratings

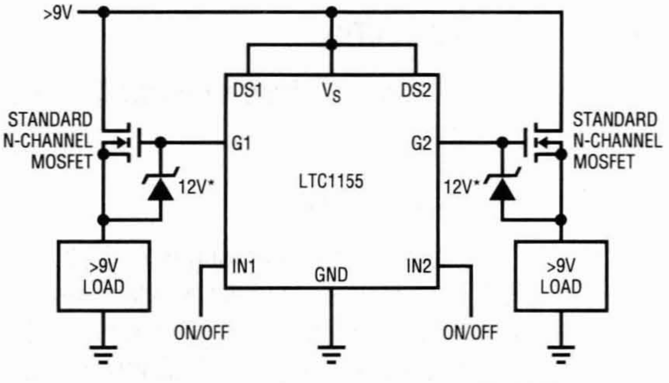
Standard MOSFET Switches

Standard N-channel MOSFET switches are rated with V_{GS} = 10V and are generally restricted to a maximum of ±20V. Again, there is some variation among MOSFET manufacturers and individual data sheets should be consulted before making a final selection. (E.g., MOSFETs with ±30V maximum V_{GS} ratings can be used without V_{GS} voltage clamps.)

MOSFET/Driver Selector Guide

Table 1 is a guide which simplifies the selection of a MOSFET switch and micropower driver for a particular supply voltage range. A family of drivers, including a single, dual and quad, are available for operation in the 4.5V to 18V range. A related device, the LTC1153, electronic circuit breaker, also operates in the 4.5V to 18V range.

The LTC1157, dual 3.3V micropower MOSFET driver, is designed specifically for low voltage operation between 2.7V and 5.5V. Finally, the LTC1255, dual high side MOSFET driver, is designed to work in the 9V to 24V automotive and industrial range.



* 1N5242B (THROUGH HOLE) OR MMBZ5242B (SURFACE MOUNT) ZENERS AN53 • TA03

Figure 3. Adding 12V V_{GS} Clamps when V_S > 9V

Each driver works with either logic-level or standard MOSFETs over a portion of the supply voltage range and is designed to work with 12V V_{GS} Zener clamp diodes when the supply range exceeds 9V as shown in Figure 3.

APPLICATIONS

Powering Large Capacitive Loads

Electrical subsystems in portable battery powered equipment are typically bypassed with large filter capacitors to reduce supply transients and supply induced glitching. If not properly switched however, these capacitors may themselves become the source of supply induced glitching.

For example, if a 100µF capacitor is powered through a P-channel switch as shown in Figure 4, and the slew rate of the switch is 0.1V/µs, the current during start-up is:

$$
\begin{aligned}
I_{START} &= C(dV/dt) \\
&= (100 \times 10^{-6})(1 \times 10^{5}) \\
&= 10A
\end{aligned}
$$

Obviously, this is too much current for the regulator to supply and the output glitches by many volts!

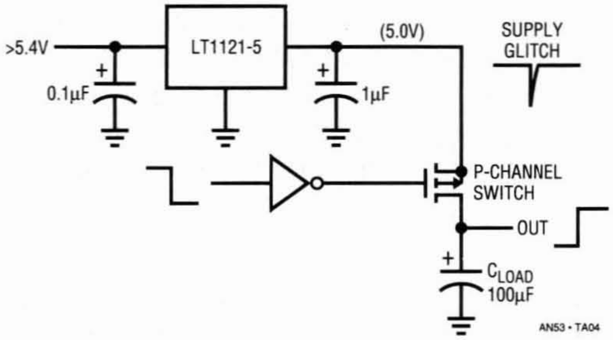


Figure 4. Power Up Supply "Glitch" Produced by Fast Starting a Large Capacitive Load

Table 1. MOSFET/Driver Selector Guide

DEVICE	DESCRIPTION	SUPPLY RANGE	USE LL FET	USE STD FET	STD FET & 12V CLAMP
LTC1153	Electronic Circuit Breaker	4.5V – 18V	4.5V – 5.5V	5.5V – 9V	9V – 18V
LTC1154	Single Micropower MOSFET Driver	4.5V – 18V	4.5V – 5.5V	5.5V – 9V	9V – 18V
LTC1155	Dual Micropower MOSFET Driver	4.5V – 18V	4.5V – 5.5V	5.5V – 9V	9V – 18V
LTC1156	Quad Micropower MOSFET Driver	4.5V – 18V	4.5V – 5.5V	5.5V – 9V	9V – 18V
LTC1157	Dual 3.3V high Side/Low Side Driver	2.7V – 5.5V	2.7V – 4.0V	4.0V – 5.5V	NA
LTC1255	Dual Industrial MOSFET Driver	9V – 24V	NA	NA	9V – 24V

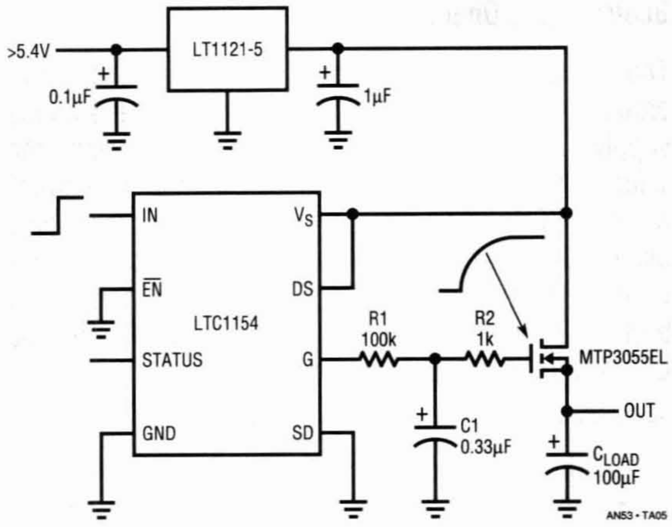

>5.4V
LT1121-5
0.1µF
1µF
IN
VS
EN
DS
LTC1154
STATUS
G
GND
SD
R1
100k
R2
1k
MTP3055EL
OUT
C1
0.33µF
CLOAD
100µF
AN53 • TA05

Figure 5. Slew Rate Reduction Network for Powering "Large" Capacitive Loads

The start-up current can be substantially reduced by reducing the slew rate at the gate of an N-channel switch as shown in Figure 5. The gate drive output of the LTC1154, single micropower MOSFET driver, is passed through a simple RC network, R1 and C1, which substantially slows the slew rate of the MOSFET gate to approximately 1.5 x 10^{-4}V/µs. Since the MOSFET is operating as a source follower, the slew rate at the source is essentially the same as that at the gate, reducing the start-up current to approximately 15mA which is easily managed by the system regulator. R2 is required to eliminate the possibility of parasitic MOSFET oscillations during switch transitions. Also, it is good practice to isolate the gates of paralleled MOSFETs with 1k resistors to decrease the possibility of interaction between switches.

Bidirectional Switch

Sometimes it is necessary to use "back-to-back" MOSFET switches to completely isolate the power source from the load, or from another power source, when the switch is turned off. This is the case when the supply voltage is higher or lower than the load voltage when powered by a secondary source.

A switched battery application, as shown in Figure 6, illustrates a bidirectional (fully isolated) switch. When the wall unit power supply is connected to V_{IN}, the load is disconnected from the battery by a fully isolated switch which allows the load voltage to fluctuate above or below the battery voltage without forcing current into the battery or pulling current out of it.

The bidirectional battery switch shown in Figure 7 illustrates how the LTC1154 drives two "back-to-back" low

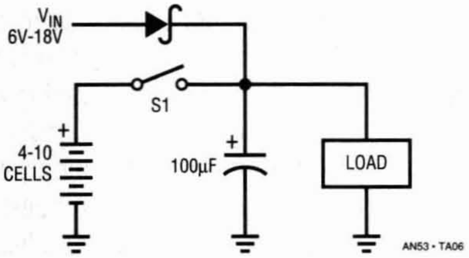

VIN
6V-18V
S1
4-10
CELLS
100µF
LOAD
AN53 • TA06

Figure 6. Switched Battery Application

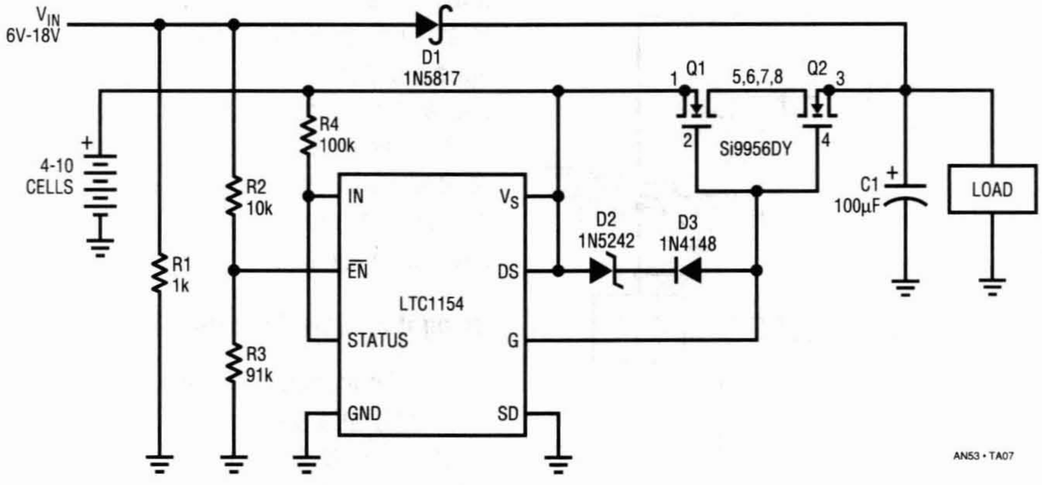

VIN
6V-18V
D1
1N5817
1
Q1
5,6,7,8
Q2
3
2
Si9956DY
4
4-10
CELLS
R4
100k
R2
10k
R1
1k
R3
91k
IN
VS
EN
DS
LTC1154
STATUS
G
GND
SD
D2
1N5242
D3
1N4148
C1
100µF
LOAD
AN53 • TA07

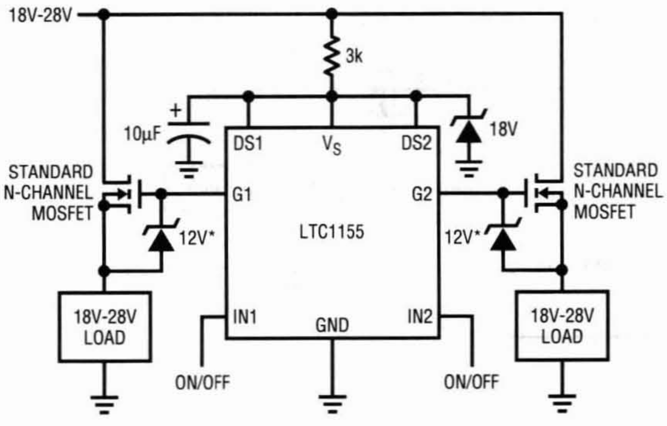
Figure 7. Bidirectional Switch Using Two "Back-to-Back" MOSFETs

$R_{DS(ON)}$ N-channel MOSFETs, Q1 and Q2, to fully disconnect the battery from the load immediately after the wall unit power supply is connected to V_{IN}. The two body diodes in Q1 and Q2 are also connected "back-to-back" and therefore no current can flow through the switch when the gate drive is removed.

The LTC1154 $\overline{\text{ENABLE}}$ input senses when the wall unit voltage exceeds 3V and inverts the action of the switch so that the two MOSFETs are turned off when the wall unit power supply is connected. The battery is subsequently reconnected immediately after the wall unit power supply is disconnected. D2 and D3 are only required for battery voltages above 9V and limit the gate drive voltage to the MOSFET switches to 12V above the battery voltage. C1 supplies load current during the short period of time (tens of microseconds) when the wall unit is disconnected and the battery switch is turned back on. R1 acts as a bleed resistor to ensure that the V_{IN} line is pulled down quickly after the the wall unit is unplugged.

18V – 28V Operation

Although designed for operation in the 4.5V to 18V range, the LTC1154/LTC1155/LTC1156 family of drivers can be operated in the 18V to 28V range by clamping the supply pin to 18V as shown in Figure 8. These drivers typically produce 36V of gate drive from an 18V supply which fully enhances an N-channel MOSFET switch operating from 18V to 28V. (12V Zener clamps should be added to ensure that the maximum MOSFET V_{GS} is never exceeded.)



* 1N5242B (THROUGH HOLE) OR MMBZ5242B (SURFACE MOUNT) ZENERS

Figure 8. Using the LTC1155 from 18V to 28V

Bootstrapped Operation

The circuit shown in Figure 9 should be used if micropower standby operation is required. The standby supply current is reduced to < 30μA by increasing the value of R1 from 3k to 330k and adding a "bootstrap" network, R2 and D2, from each switch output to the supply pin. In this way, the extra supply current is provided *only* when the switch is turned ON. The supply current drops back to 30μA when the switch is turned OFF and the LTC1155 returned to the standby mode.

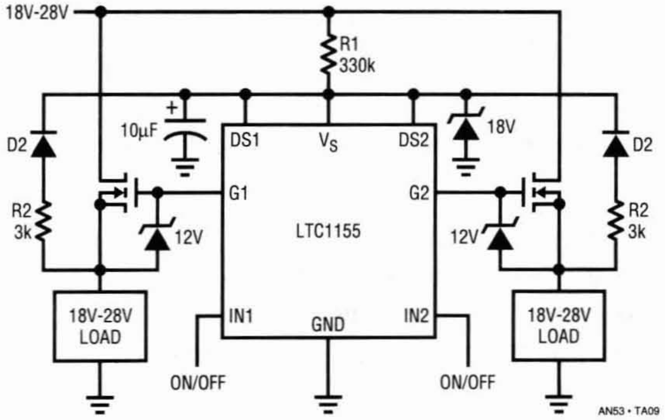


Figure 9. Bootstrapping the Supply

MOSFET SWITCH PROTECTION

Contrary to popular belief, power MOSFETs are not indestructible. They are more rugged, in some regards, than bipolar power transistors, but are still limited to operation within well defined current, voltage and power boundaries. Care must be taken to limit each of these quantities to safe operating levels to ensure that the MOSFET package is not permanently altered! (There is a power MOSFET package hanging in my office which was permanently altered by a colleague. I posted it there as a constant reminder of this truth.) Even greater care must be taken with surface mount MOSFETs because of their extremely small package and heat sink sizes.

Using the "Safe Operating Area" Graph

MOSFET manufacturers provide information, in the form of graphs and specification tables, which facilitate the design of protection circuits. A Safe Operating Area (SOA) graph is provided on the manufacturer's data sheet which establishes the electrical and physical limitations of the

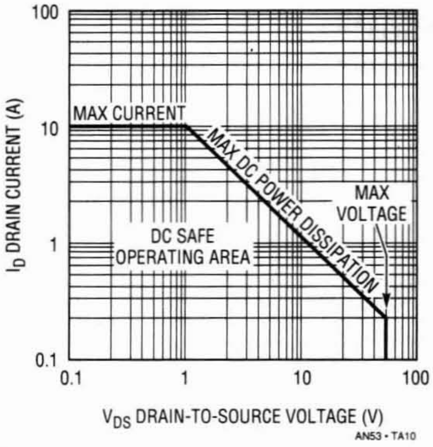


Figure 10. Typical Surface Mount MOSFET DC Safe Operating Area Graph

MOSFET in a particular package. Figure 10 is a generalized graph for a surface mount MOSFET. The X axis of the graph is drain-to-source voltage and the Y axis is drain current.

The DC Safe Operating "Box"

Three intersecting lines, along with the two axes, establish a "box" which bounds the DC Safe Operating Area (SOA) of the power MOSFET. Any excursion outside of these lines is considered destructive and must be avoided.

A horizontal line at the top of the graph specifies the maximum continuous drain current which can be conducted without damaging the leads or bond wires. Larger peak currents can be sustained for short periods and are sometimes indicated with a dotted horizontal line above the DC line.

A second line defines the maximum DC power that can be dissipated by the MOSFET package. The angle of the constant power line is –45°, as it is simply the product of voltage and current; i.e., the power dissipated at 1V and 10A is the same as that dissipated at 10V and 1A. So, a straight line intersecting these two points defines a maximum DC power dissipation limit of 10W. Note that there is no curvature in this line, as is typical in bipolar SOA graphs, because power MOSFETs do not suffer from the secondary breakdown characteristic exhibited by bipolar power transistors.

The *position* of the maximum power dissipation line is heavily dependent on the thermal resistance of the package and the external heat sinking. Surface mount packaged MOSFETs have substantially higher thermal resistance than those housed in metal cans or large plastic packages because of their small physical size and small heat sink footprint. Some surface mount MOSFET packages are scarcely larger than the silicon die they house. Therefore, surface mount MOSFETs have relatively low maximum DC power dissipation lines, typically in the range of 1W to 10W.

A third, vertical line, at the right-hand side of the graph, sets the upper limit of voltage exposure. This limit is set lower than the actual breakdown voltage of the MOSFET and should not be exceeded in normal operation. If the MOSFET is required to operate in the avalanche mode, the total energy dissipated must be held within the bounds set by the manufacturer in the Maximum Avalanche Energy graph which is sometimes given as a secondary measure of ruggedness.

The AC Safe Operating Area "Box"

Another set of lines on the SOA graph, as shown in Figure 11, establish the AC or pulsed capabilities of the MOSFET. These lines are dotted, and are drawn at the same –45° angle as the continuous DC power line, but have shorter and shorter time periods associated with them as they "move up" the graph. These lines define the maximum power which can be safely dissipated by the package and the heat sink for a given length of time. Because of their smaller package mass, surface mount MOSFETs are less able to dissipate energy (power × time) than those housed in large metal cans or plastic packages with large copper tabs (TO-220, etc.). And, therefore, greater care must be

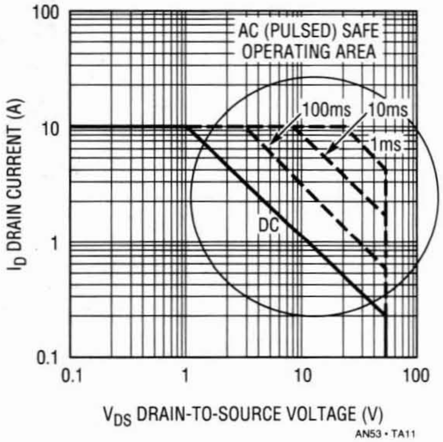


Figure 11. Typical Surface Mount MOSFET AC (Pulsed) Safe Operating Area Graph

taken to limit both the DC power dissipation and the AC (pulsed) power dissipation to safe levels.

Keeping the MOSFET Inside the "Box": A "Real" World Example

Armed with this information, it is now possible to develop protection schemes which ensure that the MOSFET stays inside the Safe Operating Area "box" and *inside the plastic package*! This process starts with an analysis of the electrical characteristics of the power source.

A NiCad battery pack, for example, is capable of supplying peak currents well in excess of the normal operating current of a typical load. The internal resistance of a typical NiCad cell is in the 0.025Ω to 0.1Ω range and therefore currents in the 10A to 50A range are possible. This is why NiCad batteries are not recommended for applications which might experience short circuit or "near" short circuit conditions, e.g. stalled motors. A surface mounted MOSFET switch powered from a NiCad battery pack, as shown in Figure 12, must be protected if it is to survive a momentary short across the motor or a sustained stall condition.

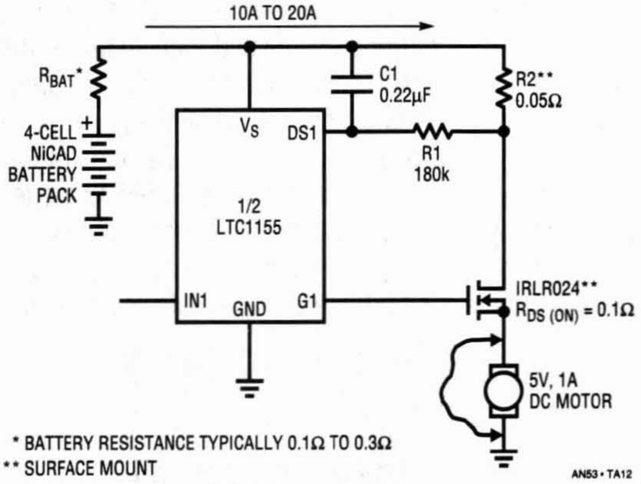


Figure 12. Protecting a Surface Mount MOSFET Switch

Surface Mount MOSFET SOA Protection

The LTC1154/LTC1155/LTC1156 drivers have built-in protection circuitry to guard against the destruction of a surface mount MOSFET, and the surrounding printed circuit board area, in the event of a short or "soft" short circuit condition. This protection is provided by a continuous drain current monitor. A small valued resistor or current shunt, R2, creates an IR drop which is used by the LTC1155 to detect excessive current flow. The drop across the resistor is very small in normal operation and therefore very little power is lost. (See the "Surface Mount Current Shunts" section for more detail.)

The MOSFET gate is reset (discharged) any time the drain sense pin of the LTC1155 falls more than 100mV below the supply voltage. R1 and C1 make up a simple RC network which delays the current sense signal long enough to start a high inrush current load, such as an incandescent lamp or DC motor, but short enough to keep the MOSFET inside the AC SOA "box."

Selecting R_{DELAY} and C_{DELAY}

Figure 13 is a graph of normalized over current shutdown time versus normalized MOSFET current. This graph is used to select the maximum RC time constant which will protect the MOSFET. The Y axis is normalized to one RC time constant. The X axis is normalized to the set current.

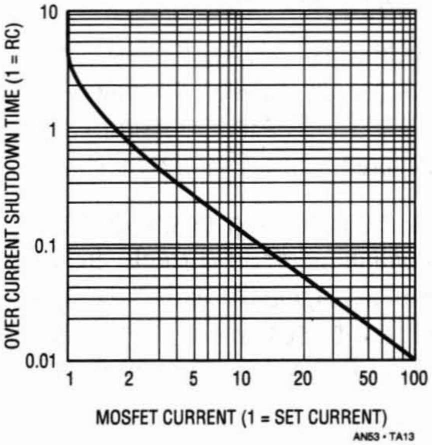


Figure 13. Shutdown Time vs MOSFET Current

The SOA graph for the surface mount MOSFET shown in Figure 11 indicates that it should not conduct 20A at V_{DS} = 5V for more than 10ms. The set current in our example is 2A (the set current is defined as the current required to develop 100mV across the drain sense resistor). 20A is 10 times the set current of 2A. By drawing a line up from 10 and reflecting it off the curve, we establish that the shutdown time at 20A is 0.1 × RC. The maximum RC time constant should therefore be set at 10 times 10ms, or 100ms. This time constant should be viewed as a maximum safe delay time and should be reduced if the competing requirement of starting a high inrush current load is less stringent; i.e. if the inrush time period is known to be

20ms, the RC time constant should be set at roughly 2 or 3 times this time period and not at the maximum of 100ms. A 40ms time constant would be produced with a 180k resistor and a 0.22µF capacitor as shown in Figure 12.

Note that the shutdown time in Figure 13 is shorter and shorter for increasing levels of MOSFET current — similar to a circuit breaker. It turns out that this is what is required by the MOSFET AC SOA graph; i.e. the product of power and time (energy) must be limited if the MOSFET is to be fully protected.

LOAD PROTECTION

As a general rule, the switch current should be terminated as quickly as possible during a short circuit or overload event. This rule is complicated somewhat by the nature of the load that is being protected.

Resistive Loads

Loads that are primarily resistive should be protected with as short a delay as possible to minimize the amount of time that the MOSFET and load are subjected to an overload condition. The drain sense circuitry has a built-in delay of approximately 10µs to eliminate false triggering by power supply or load transient conditions. This delay is sufficient to "mask" short load current transients and the starting of a small capacitor (<1µF) in parallel with the load. The drain sense pin can therefore be connected directly to the drain current sense resistor as shown in Figure 14.

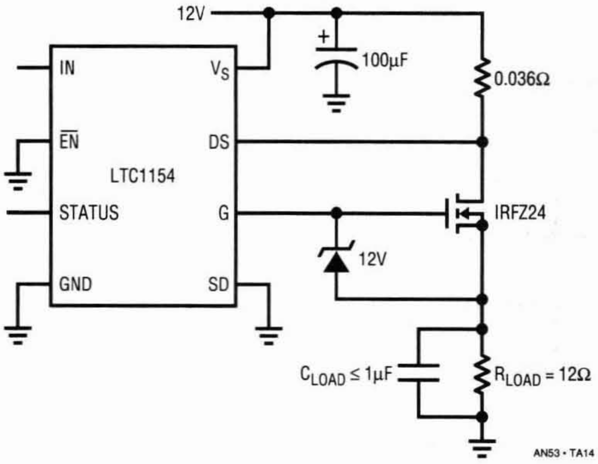


Figure 14. Protecting a Resistive Load

Inductive Loads

Loads that are primarily inductive, such as: relays, solenoids and stepper-motor windings should also be protected with as short a delay as possible to minimize the amount of time that the MOSFET and load are subjected to an over load condition. The built-in 10µs delay will ensure that the over current protection is not false triggered by a supply or load transient. No external delay components are required as shown in Figure 15.

Large inductive loads (>0.1mH) may require diodes connected directly across the inductor to safely divert the stored energy to ground. Many inductive loads have these diodes included. If not, a diode of the proper current rating should be connected across the load, as shown in Figure 15, to safely divert the stored energy.

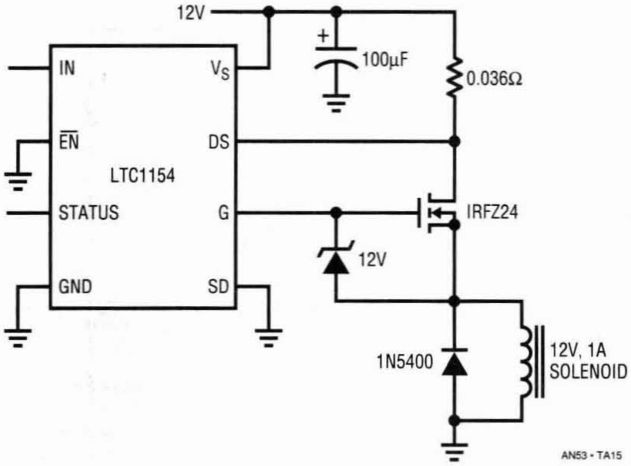


Figure 15. Protecting an Inductive Load

Capacitive Loads

Large capacitive loads, such as complex electrical systems with large bypass capacitors, should be powered using the circuit shown in Figure 16. The gate drive to the power MOSFET is passed through an RC delay network, R1 and C1, which greatly reduces the turn on ramp rate of the switch. And since the MOSFET source voltage follows the gate voltage, the load is powered smoothly and slowly from ground. This dramatically reduces the start-up current flowing into the supply capacitor(s) which, in turn, reduces supply transients and allows for slower activation of sensitive electrical loads. Diode, D1, provides a direct path for the LTC1154 protection circuitry to quickly discharge the gate in the event of an over current condition.

The RC network, R_D and C_D, in series with the drain sense input should be set to trip based on the expected characteristics of the load *after* start-up; i.e., with this circuit, it is possible to power a large capacitive load and still react quickly to an over current condition. The ramp rate at the output of the switch as it lifts off of ground is approximately:

$$dV/dt = (V_{GATE} - V_{TH})/(R1 \times C1)$$

And therefore the current flowing into the capacitor during start-up is approximately:

$$I_{START\text{-}UP} = C_{LOAD} \times dV/dt$$

Using the values shown in Figure 16, the start-up current is less than 100mA and does not false trigger the drain sense circuitry which is set at 2.7A with a 1ms delay.

Lamp Loads

The inrush current created by a lamp during turn on can be 10 to 20 times greater than the rated operating current. The circuit shown in Figure 17 shifts the current limit threshold up by a factor of 11:1 (to 30A) for 100ms when the bulb is first turned on. The current limit then drops down to 2.7A after the inrush current has subsided.

Using a Speed-Up Diode

To reduce the amount of time that the power MOSFET is in a short circuit condition, "bypass" the delay resistor with a small signal diode as shown in Figure 18. The diode will engage when the drop across the drain sense resistor exceeds about 0.7V, providing a direct path to the sense pin and dramatically reducing the amount of time the

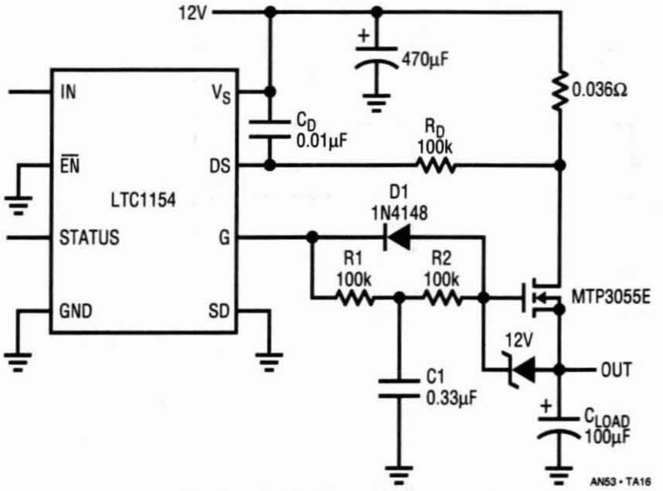

12V
470µF
0.036Ω
IN
V_S
C_D 0.01µF
R_D 100k
$\overline{EN}$
DS
LTC1154
D1 1N4148
STATUS
G
R1 100k
R2 100k
MTP3055E
GND
SD
12V
C1 0.33µF
OUT
C_{LOAD} 100µF
AN53 • TA16

Figure 16. Powering a Large Capacitive Load

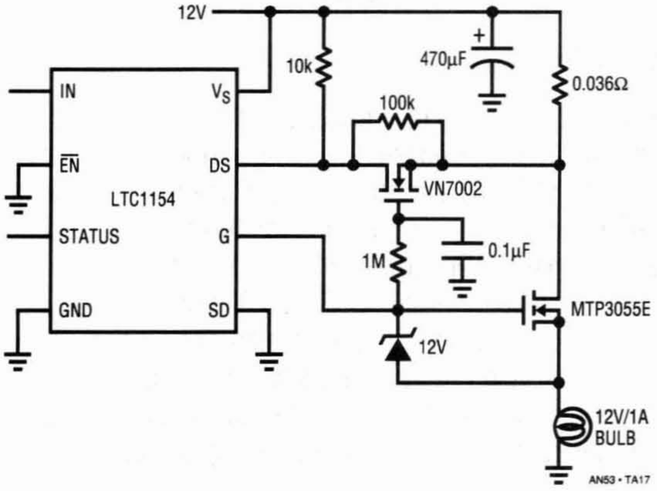

12V
10k
470µF
0.036Ω
IN
V_S
100k
$\overline{EN}$
DS
VN7002
LTC1154
STATUS
G
0.1µF
1M
GND
SD
MTP3055E
12V
12V/1A BULB
AN53 • TA17

Figure 17. Protecting a Lamp Load

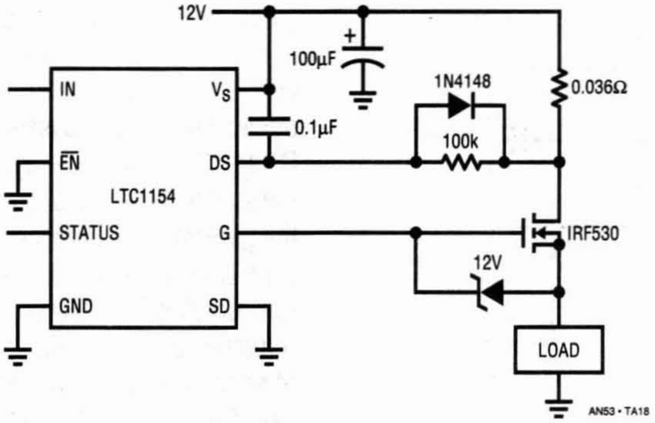

12V
100µF
1N4148
0.036Ω
IN
V_S
0.1µF
100k
$\overline{EN}$
DS
LTC1154
STATUS
G
IRF530
12V
GND
SD
LOAD
AN53 • TA18

Figure 18. Using a Speed-Up Diode

MOSFET is in an over load condition. The drain sense resistor value is selected to limit the maximum DC current to 2.8A. The diode conducts when the drain current exceeds 20A and reduces the turn-off time to 15μs.

Reverse Battery Protection

The LTC1154/LTC1155/LTC1156 family of MOSFET drivers can be protected against reverse battery conditions by connecting a resistor in series with the ground lead as shown in Figure 19. The resistor limits the supply current to less than 50mA with –12V applied. Since the LTC1154 draws very little current while in normal operation, the drop across the ground resistor is minimal. The 5V μP (or control logic) is protected by the 10k resistors in series with the input, enable and status pins.

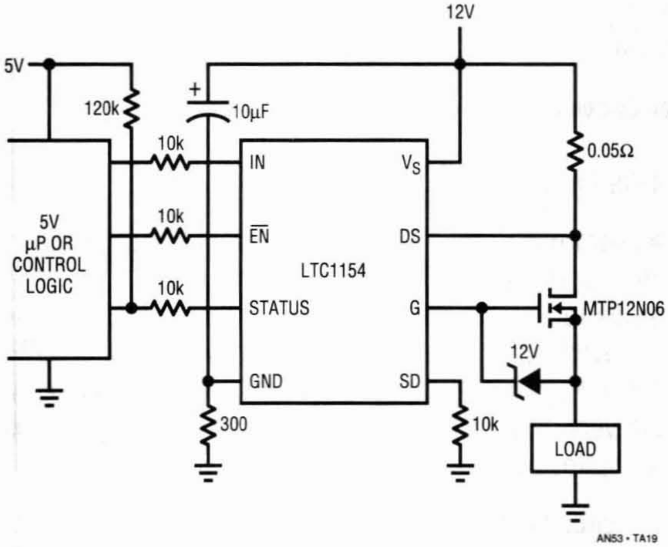


Figure 19. Reverse Battery Protection

Current Limited Power Supplies

The LTC1154/LTC1155/LTC1156 family of drivers require at least 3.5V at the supply pin to ensure proper operation. It is therefore necessary that the supply pin be held higher than 3.5V at all times, even when the output of the switch is short-circuited to ground. The output voltage of a current limited regulator may drop very quickly during short circuit and pull the supply pin of the LTC1154 below 3.5V before the shutdown circuitry has had time to respond and remove drive from the gate of the power MOSFET. A supply filter should be added as shown in Figure 20 which holds the supply pin of the LTC1154 high long enough for the over current shutdown circuitry to respond and fully discharge the gate.

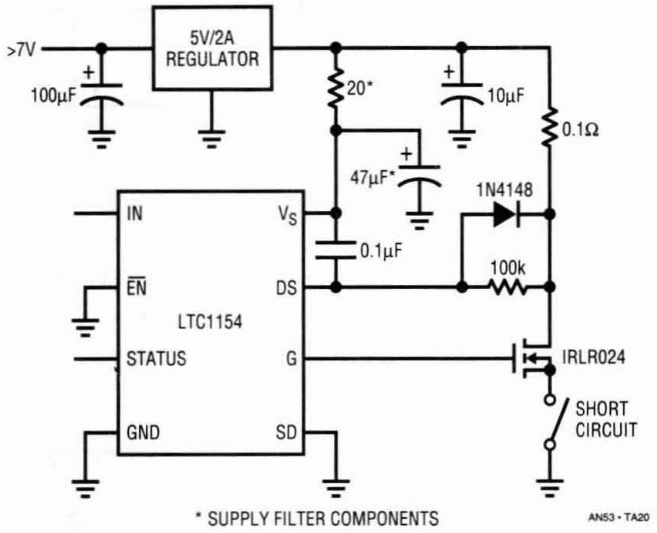


Figure 20. Supply Filter for Current Limited Supplies

5V linear regulators with small output capacitors are the most difficult to protect as they can "switch" from a normal voltage mode to a current limited mode very quickly. The large output capacitors on many switching regulators, on the other hand, may be able to hold the supply pin of the micropower driver above 3.5V sufficiently long that this extra filtering is not required.

Because all of the drivers are micropower in both the standby and ON state, the voltage drop across the supply filter is less than 2mV, and does not significantly alter the accuracy of the 100mV drain sense threshold voltage.

NOTEBOOK COMPUTER POWER MANAGEMENT

Notebook computers are dependent upon low loss MOSFET switches to efficiently manage power and maximize the operating time from a single battery charge. High efficiency switching regulators and micropower standby circuits have also become crucial elements in the quest for increased operating time.

Notebook Load Management

One technique which is frequently used in notebook computers to conserve power is to disable high current loads when not in use. Figure 21 demonstrates how the LTC1156 quad MOSFET driver is used to power and protect four low loss

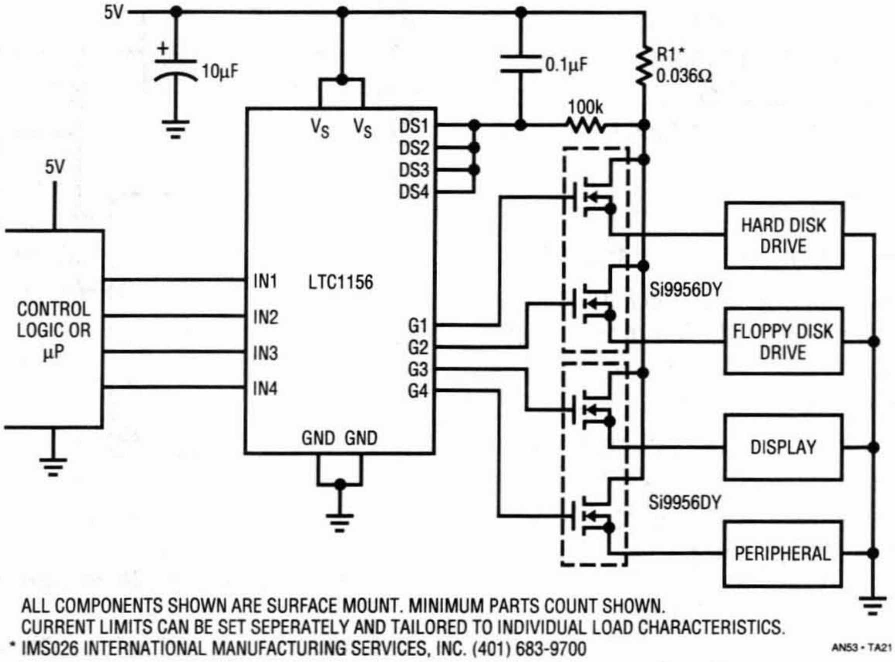

5V
10µF
0.1µF
R1*
0.036Ω
100k
V_S V_S
DS1
DS2
DS3
DS4
5V
CONTROL LOGIC OR µP
IN1
IN2
IN3
IN4
LTC1156
G1
G2
G3
G4
GND GND
Si9956DY
HARD DISK DRIVE
FLOPPY DISK DRIVE
DISPLAY
Si9956DY
PERIPHERAL
ALL COMPONENTS SHOWN ARE SURFACE MOUNT. MINIMUM PARTS COUNT SHOWN.
CURRENT LIMITS CAN BE SET SEPERATELY AND TAILORED TO INDIVIDUAL LOAD CHARACTERISTICS.
* IMS026 INTERNATIONAL MANUFACTURING SERVICES, INC. (401) 683-9700
AN53 • TA21

Figure 21. Quad High Side Switch for Laptop Computer Power Load Management

switches in a notebook computer power management system. Each load is a complex system which is only activated by the µP when it is required to process or display information. The rest of the time is spent in the standby mode where quiescent current is reduced to microamp levels to conserve power. The standby current of the LTC1156 is typically 16µA with all four inputs turned OFF.

The total current through the four switches is monitored by a very small valued resistor, R1, which drops less than 100mV at 2A. The LTC1156 current sense circuitry continuously monitors this resistor and ensures that the offending switch is turned OFF in the event the voltage drop exceeds 100mV. A short delay has been added to eliminate false triggering. The switches are re-engaged after the short circuit condition is removed by turning the inputs OFF and then back ON. It should be noted that the circuit shown in Figure 21 is the minimum parts count implementation. The LTC1156 contains four separate current limit circuits which can be tailored to the individual load characteristics. All the components shown in Figure 21 are available in surface mount packaging, including the current sense resistor (see the Current Shunt section for more detail).

4-Cell NiCad Computer Power Management

As shown in Figure 22, a 4-cell NiCad battery pack generates approximately 5.6V when fully charged. This voltage drops to about 5.2V shortly after the battery charger is removed and then drops smoothly down to about 5.0V, where it spends the majority of time during discharge. At the very end of the discharge cycle, the voltage drops precipitously below 4.6V.

The circuit of Figure 23 demonstrates how the first channel of an LTC1156 is used to regulate the output of a

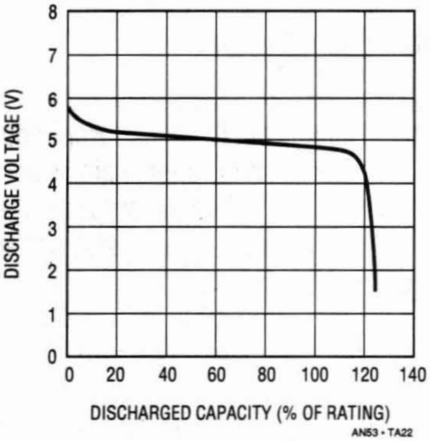
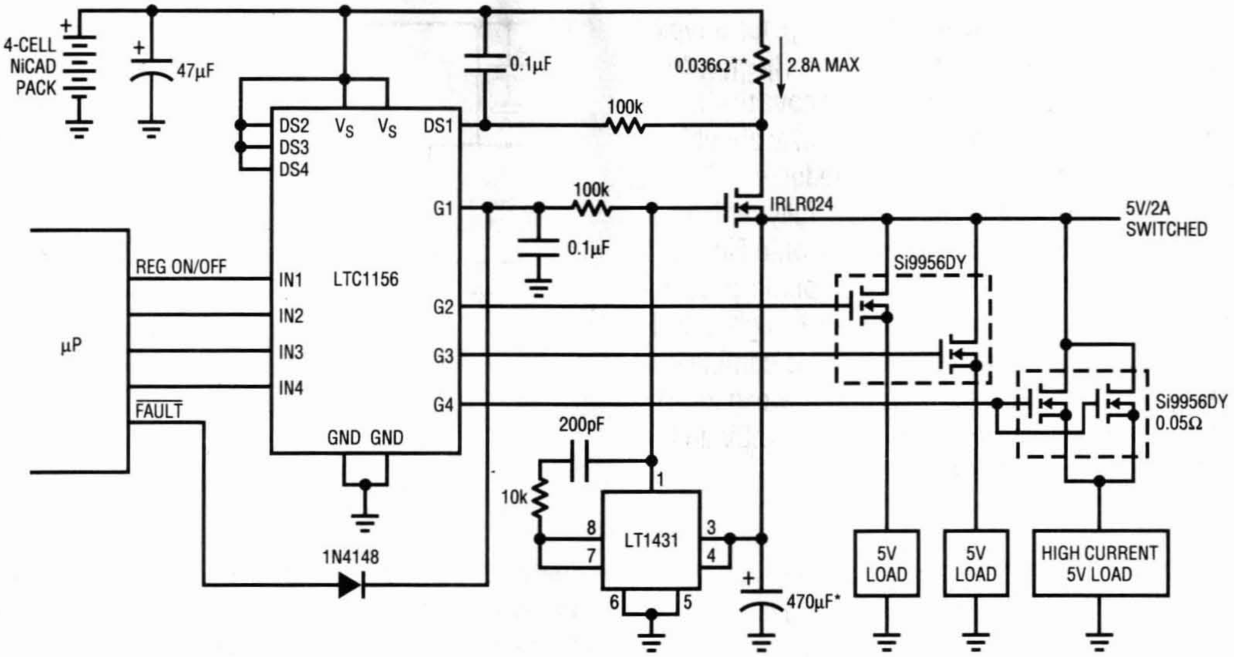


Figure 22. Typical 4-cell NiCad Discharge Characteristic


4-CELL NiCAD PACK
47µF
0.1µF
0.036Ω**
2.8A MAX
100k
DS2
DS3
DS4
VS
VS
DS1
G1
100k
0.1µF
IRLR024
5V/2A SWITCHED
REG ON/OFF
IN1
LTC1156
IN2
G2
Si9956DY
µP
IN3
G3
IN4
G4
Si9956DY 0.05Ω
FAULT
GND GND
200pF
10k
1
8
LT1431
3
7
4
6
5
1N4148
470µF*
5V LOAD
5V LOAD
HIGH CURRENT 5V LOAD

* CAPACITOR ESR < 0.5Ω
** IMS026 INTERNATIONAL MANUFACTURING SERVICES, INC. (401) 683-9700

AN53 • TA23

Figure 23. A 4-cell NiCad Computer Power Management System

four-cell NiCad battery pack to power a notebook or palmtop computer system. This approach forgoes the expense and complexity of a switching regulator to convert the battery voltage to 5V. The regulator consists of the first channel of the LTC1156 and an LT1431 programmable reference. As long as the input voltage to the regulator is sufficient to produce 5V at the output, the regulator output will limit at 5V. When the battery pack voltage drops below 5V, the MOSFET becomes fully enhanced and acts as a direct connection between the battery and the computer circuitry. A simple battery voltage monitor in the µP decides when the battery voltage drops off below 4.6V and house keeping is performed (storing data, etc.) before the batteries are completely discharged. The other three channels of the LTC1156 act as simple switches under µP control to intelligently power the other 5V sections of the computer. The number of switches can be increased by adding more LTC1155 or LTC1156 circuits as needed. All of the components shown in Figure 23, with the exception of the regulator output capacitor, are surface mount and occupy a very small amount of board space. The large capacitor value is required to maintain good load regulation during large changes in load current.

High Side Switching at 3.3V

Many circuits in notebook and palmtop computers are being designed to operate at 3.3V. The LTC1157, dual low voltage MOSFET driver, is specifically designed for operation between 2.7V and 5.5V where P-channel switches are less attractive because they are not rated with V_{GS} below 4.0V.

The LTC1157 internal charge pump boosts the gate drive voltage 5.4V above the positive rail (8.7V above ground) as shown in Figure 24, fully enhancing a logic-level N-channel MOSFET for 3.3V high side switching applications.

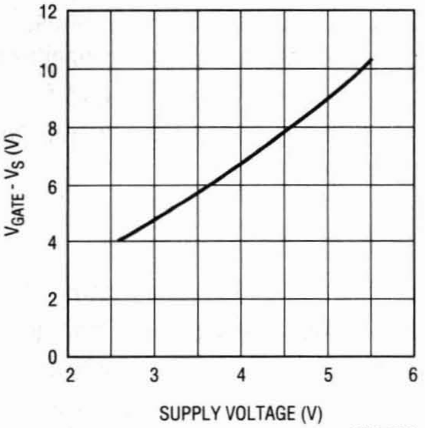


Figure 24. LTC1157 Gate Voltage *Above* Supply

Figure 25 is a graph of $R_{DS(ON)}$ versus V_{GS} for a typical logic-level, N-channel MOSFET switch. The $R_{DS(ON)}$ drops dramatically as the gate voltage is taken above the threshold voltage (1V-2V) and begins to flatten off at about 3.5V. Further gate drive does not significantly reduce the $R_{DS(ON)}$ because the MOSFET channel is already "fully" enhanced. By mapping the LTC1157 supply voltage onto Figure 25, it can be seen that the on-chip charge pump produces ample gate voltage to drive a logic-level, high side N-channel switch into full enhancement. This combination of low $R_{DS(ON)}$ MOSFET switch and micropower gate drive produces the maximum switch efficiency in 3.3V and 5V high side switch applications.

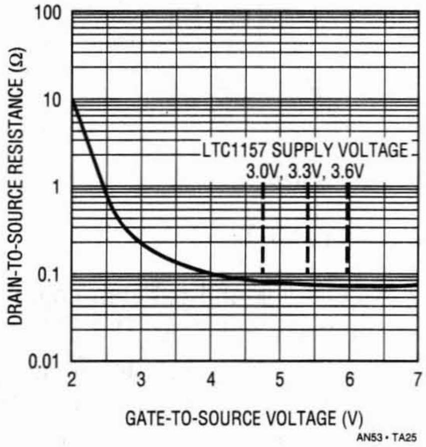


Figure 25. Typical Logic-Level N-Channel MOSFET $R_{DS(ON)}$

Figure 26 demonstrates how two surface mount MOSFETs and the LTC1157 (also available in 8-pin SO packaging) can be used to switch two 3.3V loads. The gate rise and fall time is typically in the tens of microseconds, but can be slowed by adding two resistors and a capacitor as shown on the second channel. Slower rise and fall times are sometimes required to reduce the start-up current demands of large supply capacitors.

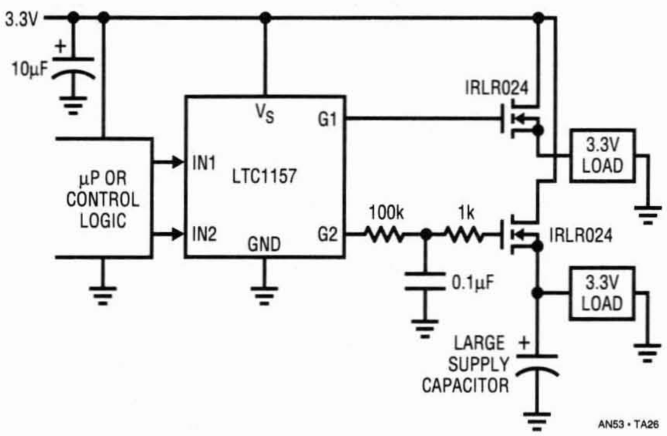


Figure 26. Dual High Side 3.3V Switch

CURRENT SHUNTS

Small valued resistors (<0.1Ω) are some times called "current shunts." This is because resistors in this range were almost exclusively used in the past to divert or shunt current in large DC ammeters. These were large four terminal devices with the smaller terminals connected to the meter and the larger ones connected to the circuit under test. This is still the picture some people get when the word "shunt" is used or when they see a small valued resistor drawn on a schematic. *Nothing could be farther from the truth!* Current shunts (small valued resistors) are now used in a wide variety of current sensing applications including: motor controllers, switching regulators, industrial and automotive load switches and portable computer power management systems, and in significantly smaller packaging.

Surface Mount Current Shunts

All of the current shunts shown in this application note are small surface mount resistors which occupy a tiny fraction of the board space once required to sense large (1A-30A) currents. This is true, not only because of advances in surface mount package technology, but because the small voltage drops (<100mV) required by the LTC1154/LTC1155/LTC1156 to sense current reduces the power dissipation in the sense resistor to surprisingly small levels.

Figure 27 is a graph of power dissipation versus set current for a sense resistor used with the LTC1154/LTC1155/LTC1156. The set current is defined as the current required to develop 100mV across the resistor. It is assumed in this calculation that the nominal load current is 50% of the set current and therefore the nominal drop across the resistor is 50mV. Note that the power dissipation and, therefore the resistor power rating, is quite small even at large set currents. For example, the

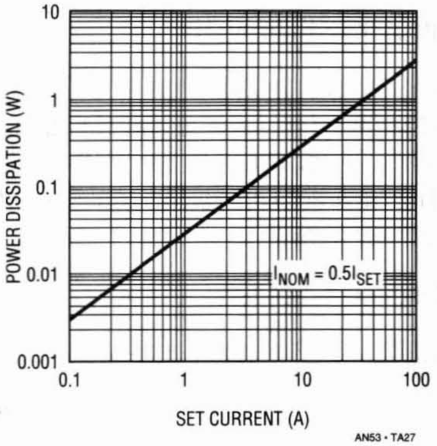


Figure 27. Sense Resistor Power Dissipation vs Set Current

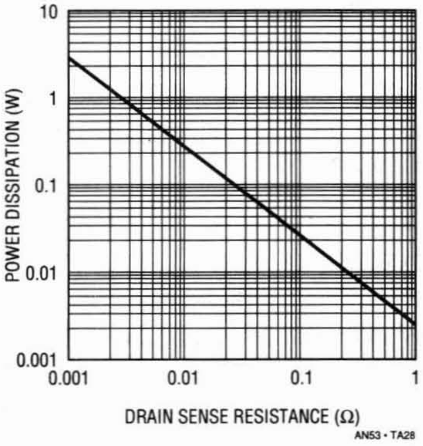


Figure 28. Sense Resistor Power Dissipation vs Sense Resistance

Table 2. Surface Mount Shunt Manufacturers

MANUFACTURER	PART NUMBERS
Dale Electronics, Inc. 1122 23rd Street Columbus, NE 68601 (402) 563-6506	WSC-1/2 WSC-1 WSC-2
International Manufacturing Services, Inc. 50 Schoolhouse Lane Portsmouth, R.I. 02871 (401) 683-9700	IMS026
International Resistive Company, Inc. P.O. Box 1860 Boone, NC 28607 (704) 264-8861	MSM-1 MSM-2 LR2010 LR2512
Isotek Corporation 566 Wilbur Ave. Swansea, MA 02777 (508) 673-2900	SMR SMV
Ohmite Manufacturing Co. 3601 Howard St. Skokie, IL 60076 (708) 675-2600	RW1S0BA RW1S5CA RW2S0CB
KRL/Bantry Components, Inc. 160 Bouchard St. Manchester, NH 03103 (603) 668-3210	SL-1 SL-2 SL-3

power dissipated by a 0.05Ω resistor (I_{SET} = 2A) is only 50mW and is therefore extremely small (the same size as a standard value surface mount resistor). The power dissipated by a 0.01Ω resistor (I_{SET} = 10A) is only 0.25W and is still quite small.

Figure 28 is similar to Figure 27, except the X axis has been converted from set current to sense resistor value. Either graph can be used to determine the power rating of the sense resistor.

Current Shunt Manufacturers

Table 2 is a list of surface mount resistors suitable for sensing MOSFET drain current. Both two terminal and four terminal resistors are available. Kelvin connections are usually not required however above 0.01Ω if the printed circuit board is designed carefully, i.e. with the "force" traces leading to the power supply and MOSFET drain, and the "sense" traces leading to the driver.

Printed Circuit Board Shunts

A carefully designed printed circuit board trace can be used in place of a current shunt in applications where tolerances can be relaxed, and where sufficient board space is available. This technique is inherently less accurate than using a 2 or 4 wire low resistance current shunt, but is sufficiently accurate for many applications.

Printed circuit board copper is expressed in units of ounces of copper per square foot, i.e. 1/2oz., 1oz., 2oz., etc. The thickness of 1oz. copper clad is approximately 1.35 mils (0.00343 cm). Since the resistivity of pure copper is 1.822 μΩ-cm, the "sheet" resistance of a 0.00343 cm thick layer of copper is approximately 530μΩ/

square. This means that a section of 1oz. copper clad, one unit long by one unit wide, has a resistance of 530μΩ regardless of the unit size.

For example, a 0.01Ω resistor to sense 10A, would be approximately 20 squares long, i.e. the strip would be 1 unit wide by 20 units long. The area of the trace must be large enough to dissipate the power produced by a 10A current flow without over stressing the copper or the laminate beneath it. A maximum current density of 50A/inch width of 1oz. copper is considered conservative and therefore a 10A, 0.01Ω, 1oz. copper clad shunt should be 0.2 inches wide and 4 inches long as shown in Figure 29.

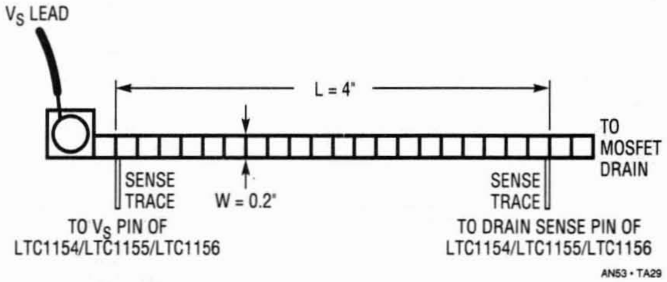

V_S LEAD
L = 4"
TO MOSFET DRAIN
SENSE TRACE
W = 0.2"
SENSE TRACE
TO V_S PIN OF LTC1154/LTC1155/LTC1156
TO DRAIN SENSE PIN OF LTC1154/LTC1155/LTC1156
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Figure 29. 0.01Ω Printed Circuit Board Current Shunt

Note that there are four connections to the shunt. The two "force" connections are made to the power supply and the drain of the MOSFET. The smaller "sense" connections are made along the length of the shunt. The length of the resistor is defined by the distance between the two sense traces and not by the total length of the force trace.

It is also possible to turn corners with the shunt as shown in Figure 30. Each corner square however is counted as 0.6 squares (318μΩ) instead of a "whole" square (530μΩ). This is because the current flowing through the corner square does not flow uniformly but is concentrated at the inside corner. The total resistance is calculated by adding the number of corner squares times 0.6 plus the number of mid body squares and multiplying by the per square resistance as shown in Figure 30.

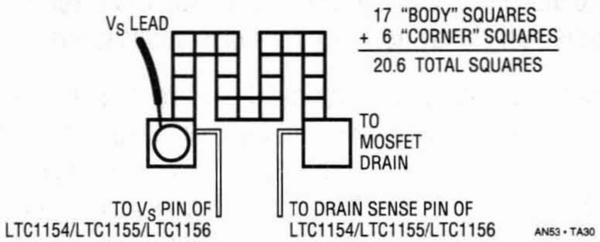


Figure 30. 'Serpentine' 0.01Ω Printed Circuit Board Current Shunt

Copper Clad Shunt "Rule-of-Thumb"

The following "rule-of-thumb" has been developed for simplifying the design of 1oz. copper clad shunts in the range of 1A to 20A for use with the LTC1154/LTC1155/LTC1156. This rule adheres to the conservative design approach outlined above:

Shunt length = 4 inches

Shunt width = 0.02 × Shunt current

Scale the width and length dimensions for other copper clad thicknesses.

Further Considerations

The printed circuit board manufacturer and circuit board etcher should be consulted for copper clad thickness and etching tolerances which ultimately determine the copper clad shunt tolerance.

Also, copper has a rather high positive temperature coefficient, approximately +0.39%/°C, which means that the printed circuit board temperature will have a strong effect on shunt resistance. The increasing shunt resistance with increasing temperature may be used to advantage however in applications where it is desirable to reduce the current limit as the circuit board temperature rises.

LTC1153: Electronic Circuit Breaker

The LTC1153 electronic circuit breaker is related to the LTC1154/LTC1155/LTC1156 family of micropower MOSFET drivers and is most similar to the LTC1154. The LTC1153 is designed to work with a low cost, N-channel power MOSFET to interrupt power to a sensitive electronic load in the event of an over current condition. The breaker is tripped by an over current condition and remains tripped for a period of time programmed by an external timing capacitor, C_T. The switch is then automatically reset and the load momentarily retried. If the load current is still too high, the switch is shutdown again. This cycle continues until the over current condition is removed, thereby protecting the sensitive load and the power MOSFET.

The gate voltage for the high side MOSFET N-channel switch is generated completely on-chip by a high frequency charge pump, similar to the LTC1154/LTC1155/LTC1156.

Programmable Timing

The trip current, trip delay time and auto-reset period are programmable over a wide range to accommodate a variety of load impedances. Figure 31 demonstrates how the LTC1153 is used in a typical circuit breaker application. The DC trip current is set by a small valued resistor, R_{SEN}, in series with the drain lead which drops 100mV when the current limit is reached. In the circuit of Figure 31, the DC trip current is set at 1A ($R_{SEN} = 0.1\Omega$).

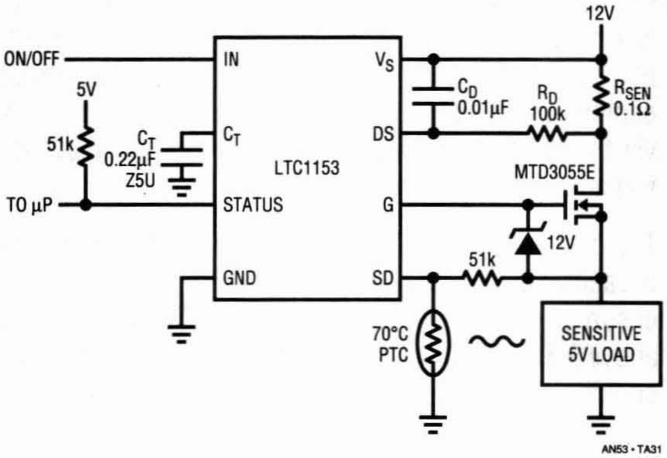


Figure 31. LTC1153 5V/1A Circuit Breaker with Thermal Shutdown

The trip delay time is set by the two delay components, R_D and C_D which establish an RC time constant in series with the drain sense resistor, producing a trip delay which is shorter for increasing breaker current (similar to a mechanical circuit breaker). Figure 32 is a graph of the trip delay time versus the circuit breaker current for a 1ms RC time constant. Note that the trip time is 0.63ms at 2A, but falls to 55μs at 20A. This characteristic ensures that the load, and the MOSFET switch, are protected against a wide range of overload conditions.

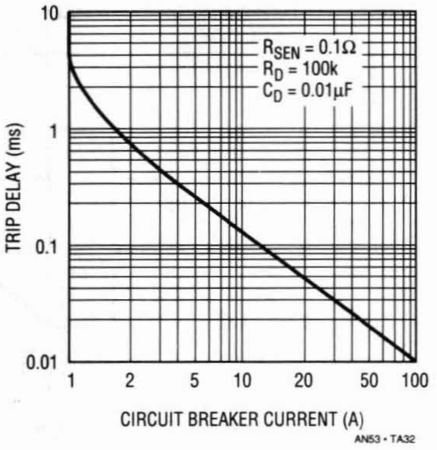


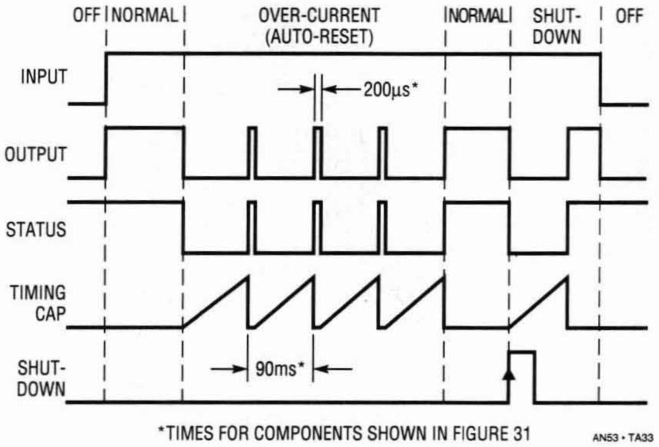
Figure 32. Trip Delay Time versus Breaker Current (for circuit shown in Figure 31).

Auto Reset Function

The auto-reset time is typically set in the range of tens of milliseconds to a few seconds by selecting the timing capacitor, C_T. The auto-reset period for the circuit in Figure 31 is 200ms, i.e. the circuit breaker is automatically reset (retried) every 200ms until the overload condition is removed. The switch then returns to normal operation and continues to power the load until another fault condition is encountered.

An open drain status output is provided to warn the host μP whenever the circuit breaker has been tripped. The μP can either wait for the auto-reset function to reset the load, or shut the switch OFF after a fixed number of retries.

A shutdown input is also provided which interfaces directly with a PTC thermistor to sense over temperature conditions and trip the circuit breaker whenever the load temperature, or MOSFET switch temperature, exceeds a safe level. The thermistor shown in Figure 31 trips the circuit breaker when the load temperature exceeds approximately 70°C.



*TIMES FOR COMPONENTS SHOWN IN FIGURE 31

Figure 33. LTC1153 Typical Timing Diagram

Figure 33 is a timing diagram with some typical waveforms generated by the circuit breaker in the normal operating mode, the overload mode and the shutdown mode. Note that the timing capacitor, C_T, is held low until a fault condition is encountered and then charged by a small internal current source until the threshold is reached and the switch turned back on. This cycle continues until the overload is removed and the switch returned to normal operation.

SCSI Termination Power

The termination power for a SCSI interface is protected to avoid damaging the drivers, the connectors and the printed circuit board in the event of a short circuiting of the connector or interconnecting cable. This protection is provided by the circuit breaker circuit shown in Figure 34. With the component values shown, the DC current is limited to 1A with a trip delay time constant of 1ms. The breaker will trip if the cable or connector is accidently shorted and will retry every second until the short circuit is removed. The termination power will then return to normal and the interface will be re-connected. The µP can continuously monitor the status of the termination power via the fault flag output of the LTC1153 and may take further action if the fault condition persists.

The gate voltage ramp is slowed to smoothly start large capacitive loads. A power supply filter has been added to ensure that the supply pin to the LTC1153 is maintained above 3.5V until the gate is fully discharged during a short circuit.

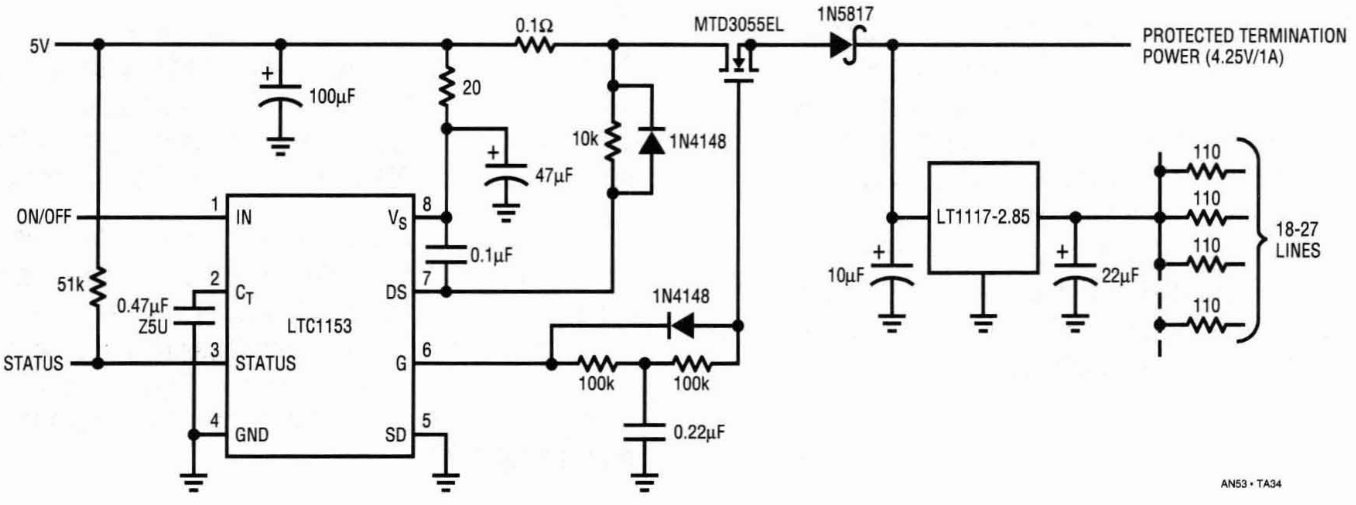

5V
100µF
0.1Ω
20
47µF
10k
1N4148
MTD3055EL
1N5817
PROTECTED TERMINATION POWER (4.25V/1A)
ON/OFF
1
IN
8
VS
0.1µF
51k
2
CT
0.47µF Z5U
DS
7
LTC1153
3
STATUS
G
6
STATUS
4
GND
SD
5
1N4148
100k
100k
0.22µF
LT1117-2.85
10µF
22µF
110
110
110
110
18-27 LINES
AN53 • TA34

Figure 34. LTC1153 SCSI Termination Power Protection

Application Note 54

March 1993

Power Conversion from Milliamps to Amps at Ultra-High Efficiency (Up to 95%)

Brian Huffman

Randy Flatness

INTRODUCTION

Efficiency is frequently the main goal for power supplies of portable computers and hand-held equipment. High efficiency converters are necessary in these applications to minimize power drain on the input source (batteries, etc.) and reduce heat buildup in the power components, allowing for smaller and lighter systems. As a result, power conversion efficiency must be in the 90% range in order to meet these goals. This application note features power supply circuits that satisfy these design requirements as well as attain efficiency in excess of 90% in a wide variety of applications.

The recent development of the LTC1147, LTC1148, and LTC1149 makes ultra-high efficiency conversion possible. In addition, the LTC1148 and LTC1149 are synchronous switching regulators, achieving high efficiency conversion at output currents in excess of 10A. These controllers feature a current-mode architecture which has an automatic low current operating mode called Burst Mode™ operation, making 90% efficiencies possible at output currents as low as 10mA. This feature maximizes battery life while a product is in a sleep or standby mode.

This is a preliminary release of Application Note 55. The complete application note will soon be available; therefore, contact your local Linear Technology representative or call the factory (408-432-1900) to receive the final version when it becomes available. In the meantime, application information can be found in the LTC1147, LTC1148, and LTC1149 Data Sheets. **Pay particular attention to the board layout information on decoupling and ground routing to achieve optimum performance.**

Burst Mode™ is a trademark of Linear Technology Corporation.

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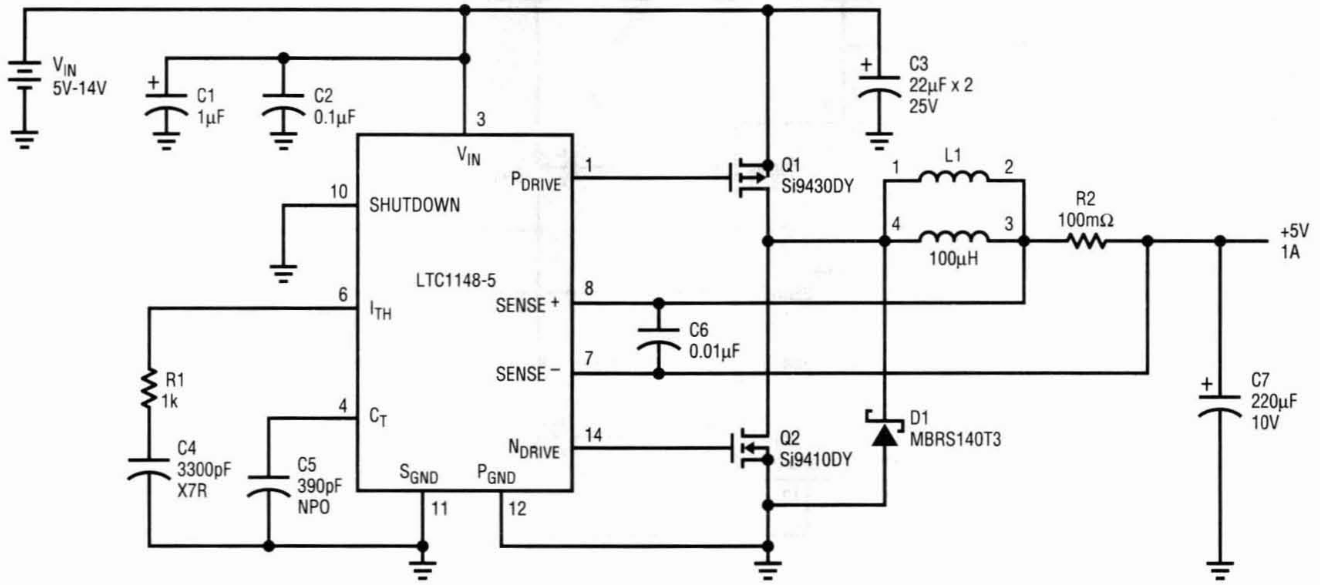
Boost

LTC1148: (2V-5V to 5V/1A) Boost Converter .... Figure 19 AN54-21

Appendix A

Suggested Manufacturers AN54-22


VIN
5V-14V
C1
1µF
C2
0.1µF
3
VIN
LTC1148-5
10
SHUTDOWN
PDRIVE
1
6
ITH
SENSE+
8
SENSE−
7
4
CT
NDRIVE
14
SGND
PGND
11
12
R1
1k
C4
3300pF
X7R
C5
390pF
NPO
C6
0.01µF
C3
22µF x 2
25V
Q1
Si9430DY
Q2
Si9410DY
L1
1
2
4
3
100µH
R2
100mΩ
+5V
1A
D1
MBRS140T3
C7
220µF
10V

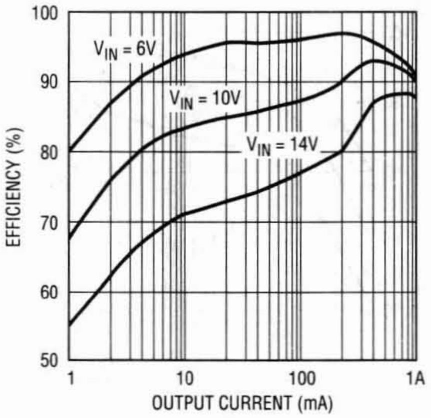
C1	(TA)
C3	AVX (TA) TPSD226K025R0200 ESR = 0.200Ω I_{RMS} = 0.775A
C7	AVX (TA) TPSE227K010R0080 ESR = 0.080Ω I_{RMS} = 1.285A
Q1	SILICONIX PMOS BV_{DSS} = 20V RDS_{ON} = 0.100Ω C_{RSS} = 400pF Q_g = 50nC
Q2	SILICONIX NMOS BV_{DSS} = 30V RDS_{ON} = 0.050Ω C_{RSS} = 160pF Q_g = 30nC
D1	MOTOROLA SCHOTTKY VBR = 40V
R2	KRL SP-1/2-A1-0R100J Pd = 0.75W
L1	COILTRONICS CTX100-4 DCR = 0.175Ω KOOL Mµ CORE

ALL OTHER CAPACITORS ARE CERAMIC

QUIESCENT CURRENT = 180µA
TRANSITION CURRENT (BURST MODE™ OPERATION/CONTINUOUS OPERATION) = 200mA

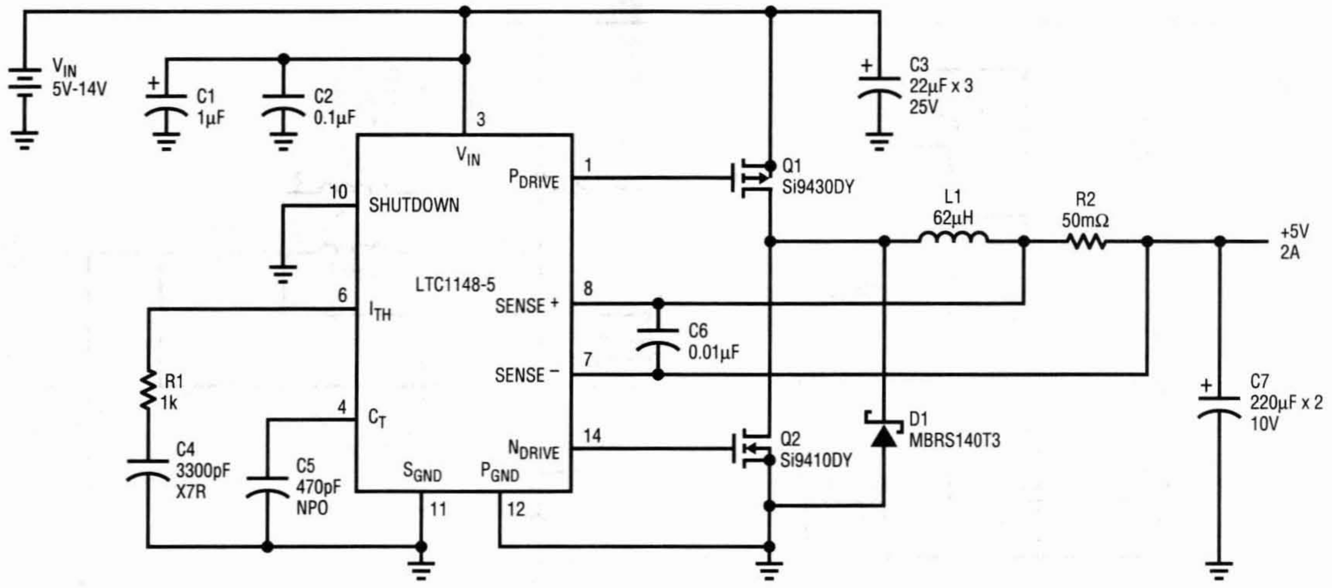
AN54 • TA01

Figure 1A. LTC1148: (5V-14V to 5V/1A) Buck Converter with Surface Mount Technology



AN54 • TA02

Figure 1B. LTC1148: (5V-14V to 5V/1A) Buck Converter Measured Efficiency


V_{IN} 5V-14V
C1 1μF
C2 0.1μF
3
V_{IN}
10
SHUTDOWN
P_{DRIVE}
1
Q1 Si9430DY
C3 22μF x 3 25V
L1 62μH
R2 50mΩ
+5V 2A
LTC1148-5
6
I_{TH}
SENSE +
8
C6 0.01μF
SENSE −
7
R1 1k
4
C_T
N_{DRIVE}
14
Q2 Si9410DY
D1 MBRS140T3
C7 220μF x 2 10V
C4 3300pF X7R
C5 470pF NPO
S_{GND}
P_{GND}
11
12

C1 (TA)
C3 AVX (TA) TPSD226K025R0200 ESR = 0.200Ω I_{RMS} = 0.775A
C7 AVX (TA) TPSE227K010R0080 ESR = 0.080Ω I_{RMS} = 1.285A
Q1 SILICONIX PMOS BV_{DSS} = 20V RDS_{ON} = 0.100Ω C_{RSS} = 400pF Q_g = 50nC
Q2 SILICONIX NMOS BV_{DSS} = 30V RDS_{ON} = 0.050Ω C_{RSS} = 160pF Q_g = 30nC
D1 MOTOROLA SCHOTTKY VBR = 40V
R2 KRL SL- 1-C1-0R050J Pd = 1W
L1 COILTRONICS CTX62-2-MP DCR = 0.040Ω MMP CORE (THROUGH HOLE)

ALL OTHER CAPACITORS ARE CERAMIC

QUIESCENT CURRENT = 180μA
TRANSITION CURRENT (BURST MODE™ OPERATION/CONTINUOUS OPERATION) = 400mA

AN54 • TA03

Figure 2A. LTC1148: (5V-14V to 5V/2A) Buck Converter with Surface Mount Technology

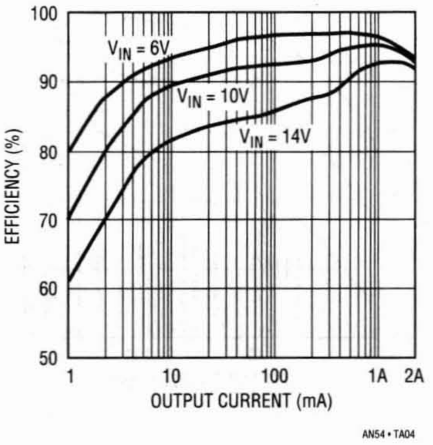
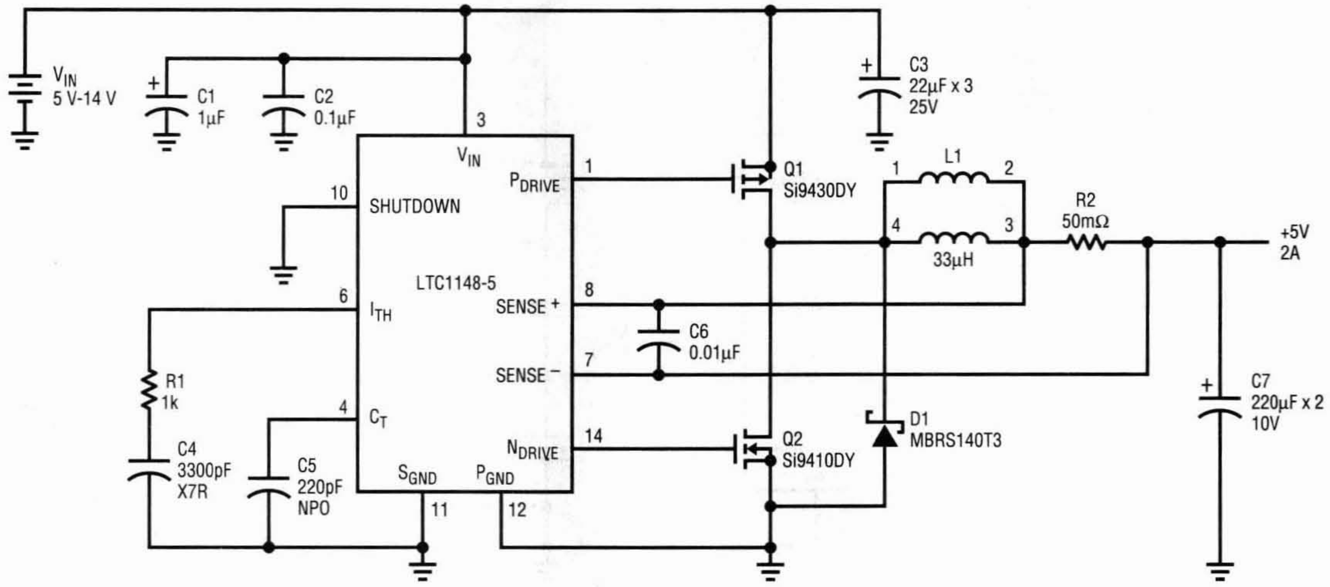


Figure 2B. LTC1148: (5V-14V to 5V/2A) Buck Converter Measured Efficiency


VIN
5V-14V
C1
1μF
C2
0.1μF
3
VIN
10
SHUTDOWN
LTC1148-5
6
ITH
R1
1k
4
CT
C4
3300pF
X7R
C5
220pF
NPO
SGND
PGND
11
12
PDRIVE
1
SENSE+
8
SENSE−
7
NDRIVE
14
C6
0.01μF
Q1
Si9430DY
Q2
Si9410DY
C3
22μF x 3
25V
L1
1
2
4
3
33μH
R2
50mΩ
D1
MBRS140T3
+5V
2A
C7
220μF x 2
10V

C1	(TA)
C3	AVX (TA) TPSD226K025R0200 ESR = 0.200Ω I_{RMS} = 0.775A
C7	AVX (TA) TPSE227K010R0080 ESR = 0.080Ω I_{RMS} = 1.285A
Q1	SILICONIX PMOS BV_{DSS} = 20V RDS_{ON} = 0.100Ω C_{RSS} = 400pF Q_g = 50nC
Q2	SILICONIX NMOS BV_{DSS} = 30V RDS_{ON} = 0.050Ω C_{RSS} = 160pF Q_g = 30nC
D1	MOTOROLA SCHOTTKY VBR = 40V
R2	KRL SL-1-C1-0R050J Pd = 1W
L1	COILTRONICS CTX33-4 DCR = 0.06Ω KOOL Mμ CORE

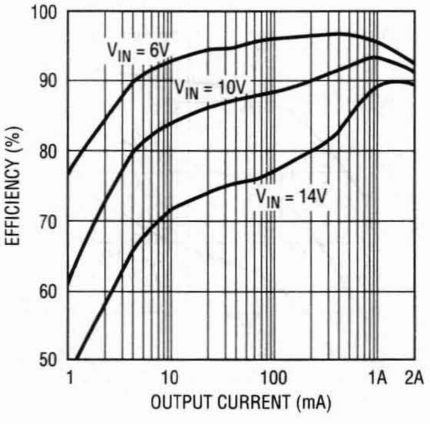
ALL OTHER CAPACITORS ARE CERAMIC

QUIESCENT CURRENT = 180μA

TRANSITION CURRENT (BURST MODE™ OPERATION/CONTINUOUS OPERATION) = 400mA

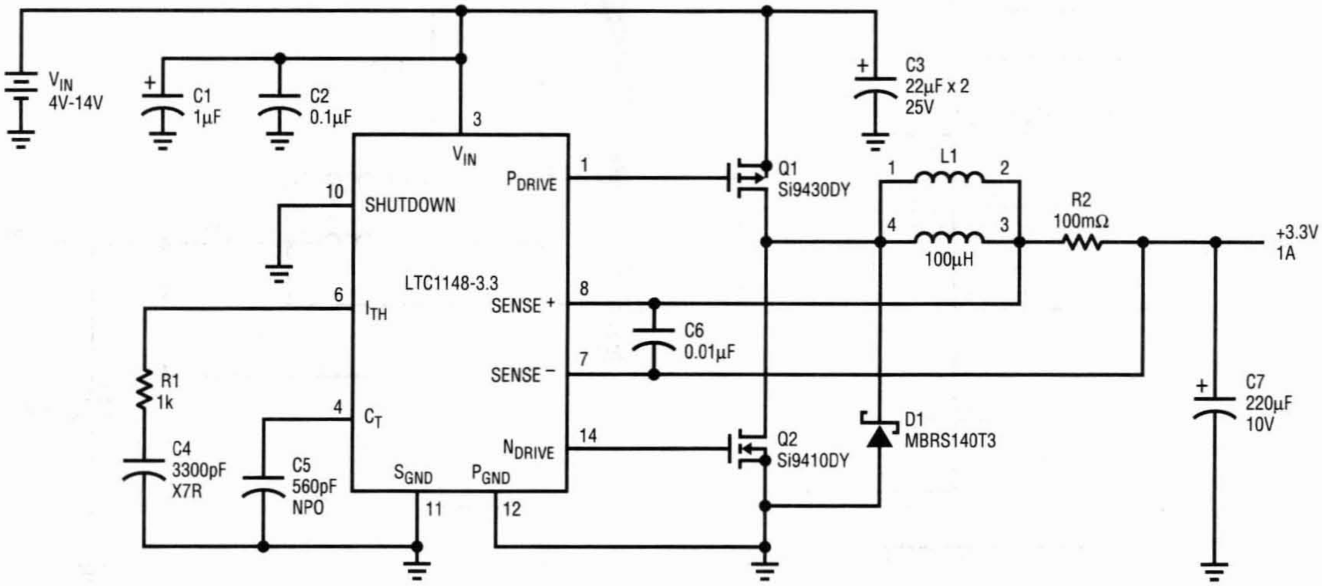
AN54 • TA05

Figure 3A. LTC1148: (5V-14V to 5V/2A) High Frequency Buck Converter with Surface Mount Technology



AN54 • TA06

Figure 3B. LTC1148: (5V-14V to 5V/2A) High Frequency Buck Converter Measured Efficiency



VIN 4V-14V
C1 1µF
C2 0.1µF
3
VIN
PDRIVE
1
10
SHUTDOWN
LTC1148-3.3
6
ITH
8
SENSE +
7
SENSE –
4
CT
14
NDRIVE
SGND
PGND
11
12
R1 1k
C4 3300pF X7R
C5 560pF NPO
C6 0.01µF
Q1 Si9430DY
Q2 Si9410DY
D1 MBRS140T3
C3 22µF x 2 25V
L1
1
2
4
3
100µH
R2 100mΩ
+3.3V 1A
C7 220µF 10V

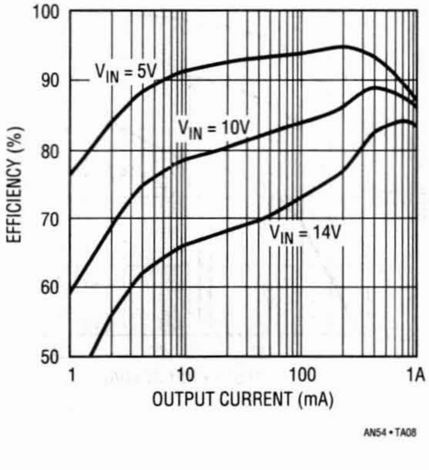
C1 (TA)
C3 AVX (TA) TPSD226K025R0200 ESR = 0.200Ω I_{RMS} = 0.775A
C7 AVX (TA) TPSE227K010R0080 ESR = 0.080Ω I_{RMS} = 1.285A
Q1 SILICONIX PMOS BV_{DSS} = 20V RDS_{ON} = 0.100Ω C_{RSS} = 400pF Q_g = 50nC
Q2 SILICONIX NMOS BV_{DSS} = 30V RDS_{ON} = 0.050Ω C_{RSS} = 160pF Q_g = 30nC
D1 MOTOROLA SCHOTTKY VBR = 40V
R2 KRL SP-1/2-A1-0R100J Pd = 0.75W
L1 COILTRONICS CTX100-4 DCR = 0.175Ω KOOL Mµ CORE

ALL OTHER CAPACITORS ARE CERAMIC

QUIESCENT CURRENT = 180µA
TRANSITION CURRENT (BURST MODE™ OPERATION/CONTINUOUS OPERATION) = 250mA

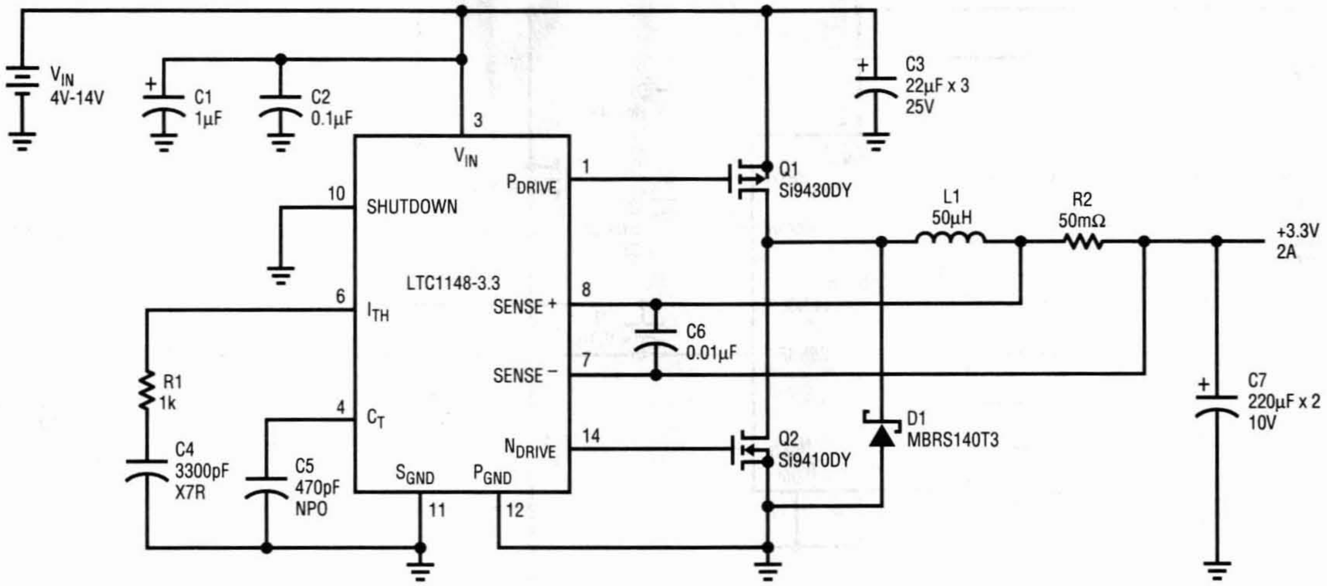
AN54 • TA07

Figure 4A. LTC1148: (4V-14V to 3.3V/1A) Buck Converter with Surface Mount Technology



AN54 • TA08

Figure 4B. LTC1148: (4V-14V to 3.3V/1A) Buck Converter Measured Efficiency


V_{IN}
4V-14V
C1
1µF
C2
0.1µF
3
V_{IN}
10
SHUTDOWN
P_{DRIVE}
1
LTC1148-3.3
6
I_{TH}
SENSE +
8
SENSE –
7
4
C_T
N_{DRIVE}
14
S_{GND}
P_{GND}
11
12
R1
1k
C4
3300pF
X7R
C5
470pF
NPO
C6
0.01µF
C3
22µF x 3
25V
Q1
Si9430DY
Q2
Si9410DY
L1
50µH
R2
50mΩ
D1
MBRS140T3
+3.3V
2A
C7
220µF x 2
10V

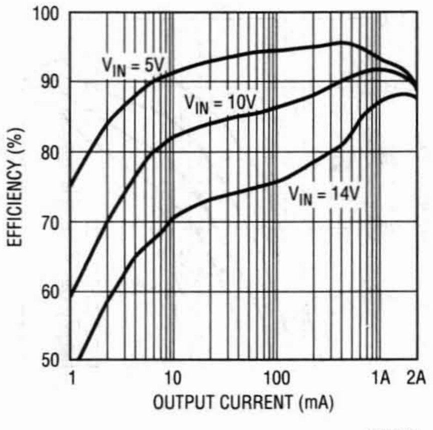
C1 (TA)
C3 AVX (TA) TPSD226K025R0200 ESR = 0.200Ω I_{RMS} = 0.775A
C7 AVX (TA) TPSE227K010R0080 ESR = 0.080Ω I_{RMS} = 1.285A
Q1 SILICONIX PMOS BV_{DSS} = 20V RDS_{ON} = 0.100Ω C_{RSS} = 400pF Q_g = 50nC
Q2 SILICONIX NMOS BV_{DSS} = 30V RDS_{ON} = 0.050Ω C_{RSS} = 160pF Q_g = 30nC
D1 MOTOROLA SCHOTTKY VBR = 40V
R2 KRL SL-1-C1-0R050J Pd = 1W
L1 COILTRONICS CTX50-2-MP DCR = 0.032Ω MMP CORE (THROUGH HOLE)

ALL OTHER CAPACITORS ARE CERAMIC

QUIESCENT CURRENT = 180µA
TRANSITION CURRENT (BURST MODE™ OPERATION/CONTINUOUS OPERATION) = 450mA

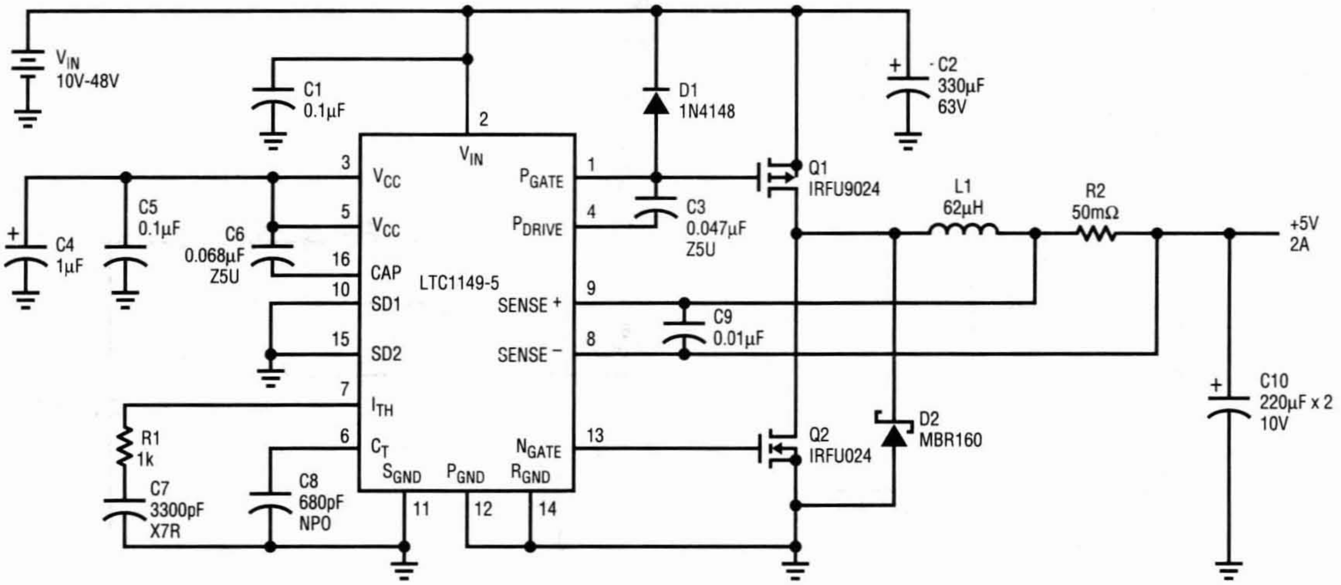
AN54 • TA09

Figure 5A. LTC1148: (4V-14V to 3.3V/2A) Buck Converter with Surface Mount Technology



AN54 • TA10

Figure 5B. LTC1148: (4V-14V to 3.3V/2A) Buck Converter Measured Efficiency


V_{IN}
10V-48V
C1
0.1µF
2
V_{IN}
D1
1N4148
C2
330µF
63V
3
V_{CC}
P_{GATE}
1
Q1
IRFU9024
C5
0.1µF
5
V_{CC}
P_{DRIVE}
4
C3
0.047µF
Z5U
L1
62µH
R2
50mΩ
+5V
2A
C4
1µF
C6
0.068µF
Z5U
16
CAP
LTC1149-5
10
SD1
SENSE⁺
9
C9
0.01µF
15
SD2
SENSE⁻
8
7
I_{TH}
C10
220µF x 2
10V
R1
1k
6
C_T
N_{GATE}
13
Q2
IRFU024
D2
MBR160
C7
3300pF
X7R
C8
680pF
NPO
S_{GND}
P_{GND}
R_{GND}
11
12
14

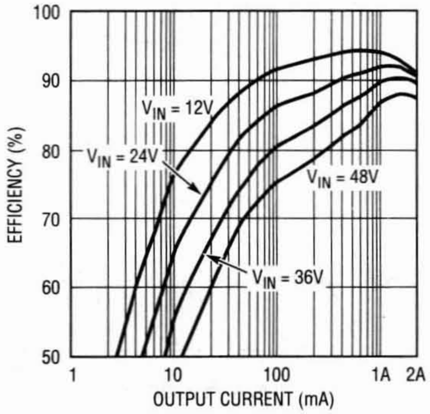
C2 UNITED CHEMI-CON (AL) LXF63VB331M12.5 x 30 ESR = 0.170Ω I_{RMS} = 1.280A
C4 (TA)
C10 SANYO (OS-CON) 10SA220M ESR = 0.035Ω I_{RMS} = 2.360A
Q1 IR PMOS BV_{DSS} = 60V RDS_{ON} = 0.280Ω C_{RSS} = 65pF Q_g = 19nC
Q2 IR NMOS BV_{DSS} = 60V RDS_{ON} = 0.100Ω C_{RSS} = 79pF Q_g = 28nC
D1 SILICON VBR = 75V
D2 MOTOROLA SCHOTTKY VBR = 60V
R2 KRL NP-1A-C1-0R050J Pd = 1W
L1 COILTRONICS CTX62-2-MP DCR = 0.040Ω MMP CORE

ALL OTHER CAPACITORS ARE CERAMIC

QUIESCENT CURRENT = 1.5mA
TRANSITION CURRENT (BURST MODE™ OPERATION/CONTINUOUS OPERATION) = 570mA

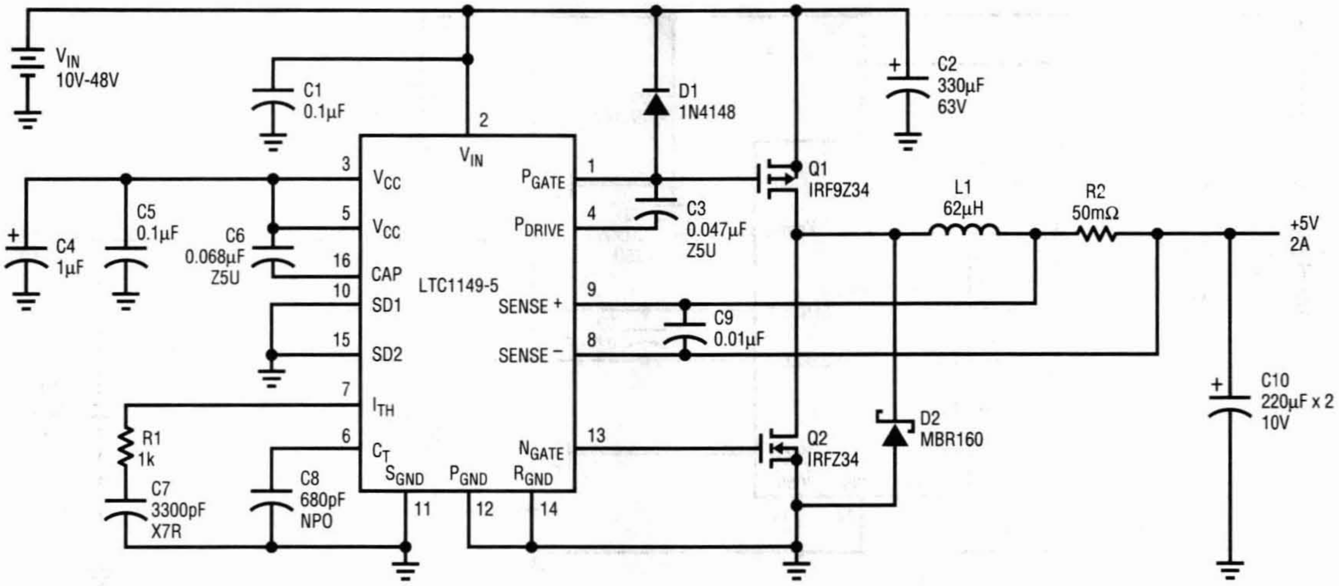
AN54 • TA11

Figure 6A. LTC1149: (10V-48V to 5V/2A) High Voltage Buck Converter



AN54 • TA12

Figure 6B. LTC1149: (10V-48V to 5V/2A) High Voltage Buck Converter Measured Efficiency


VIN
10V-48V
C1
0.1µF
2
D1
1N4148
C2
330µF
63V
3
VCC
VIN
PGATE
1
Q1
IRF9Z34
L1
62µH
R2
50mΩ
+5V
2A
5
VCC
PDRIVE
4
C3
0.047µF
Z5U
C4
1µF
C5
0.1µF
C6
0.068µF
Z5U
16
CAP
LTC1149-5
10
SD1
SENSE +
9
C9
0.01µF
15
SD2
SENSE –
8
C10
220µF x 2
10V
7
ITH
D2
MBR160
R1
1k
6
CT
NGATE
13
Q2
IRFZ34
C7
3300pF
X7R
C8
680pF
NPO
SGND
PGND
RGND
11
12
14

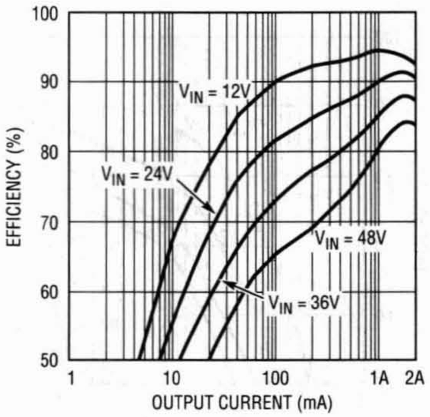
C2 UNITED CHEMI-CON (AL) LXF63VB331M12.5 x 30 ESR = 0.170Ω I_{RMS} = 1.280A
C4 (TA)
C10 SANYO (OS-CON) 10SA220M ESR = 0.035Ω I_{RMS} = 2.360A
Q1 IR PMOS BV_{DSS} = 60V RDS_{ON} = 0.140Ω C_{RSS} = 100pF Q_g = 34nC
Q2 IR NMOS BV_{DSS} = 60V RDS_{ON} = 0.050Ω C_{RSS} = 100pF Q_g = 32nC
D1 SILICON VBR = 75V
D2 MOTOROLA SCHOTTKY VBR = 60V
R2 KRL NP-1A-C1-0R050J Pd = 1W
L1 COILTRONICS CTX62-2-MP DCR = 0.040Ω MMP CORE

ALL OTHER CAPACITORS ARE CERAMIC

QUIESCENT CURRENT = 1.5mA
TRANSITION CURRENT (BURST MODE™ OPERATION/CONTINUOUS OPERATION) = 560mA

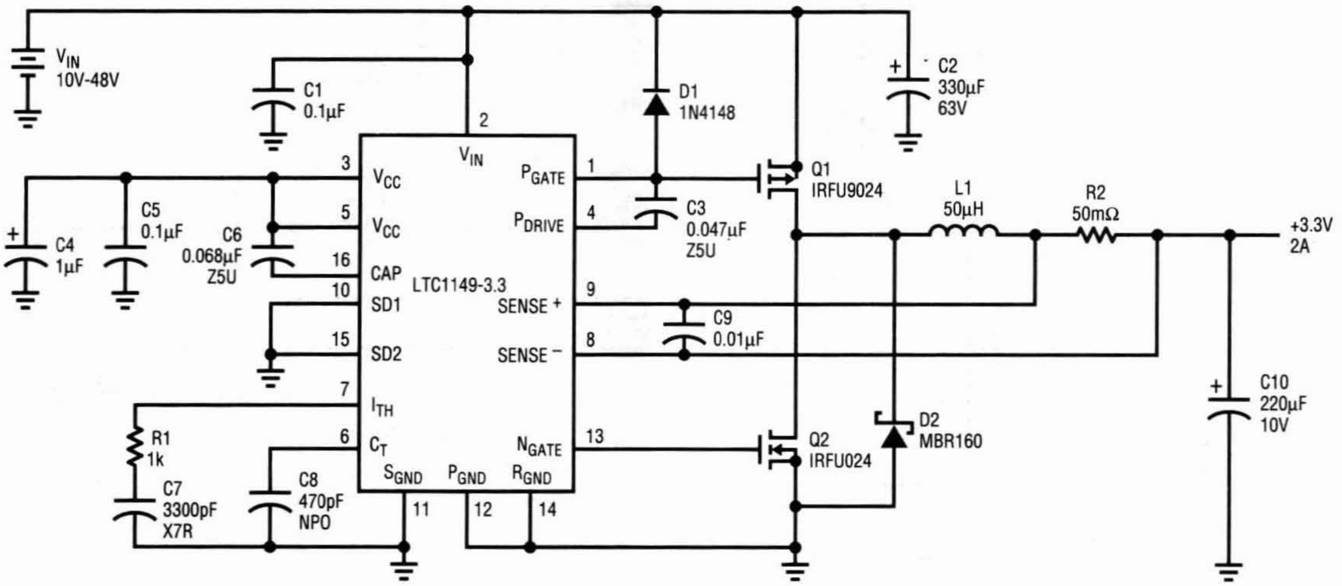
AN54 • TA13

Figure 7A. LTC1149: (10V-48V to 5V/2A) High Voltage Buck Converter with Large P-Channel and N-Channel MOSFETs



AN54 • TA14

Figure 7B. LTC1149: (10V-48V to 5V/2A) Measured Efficiency with Large P-Channel and N-Channel MOSFETs


V_IN
10V-48V
C1
0.1μF
2
V_IN
D1
1N4148
C2
330μF
63V
3
V_CC
P_GATE
1
Q1
IRFU9024
5
V_CC
P_DRIVE
4
C3
0.047μF
Z5U
L1
50μH
R2
50mΩ
+3.3V
2A
C4
1μF
C5
0.1μF
C6
0.068μF
Z5U
16
CAP
LTC1149-3.3
10
SD1
SENSE⁺
9
C9
0.01μF
15
SD2
SENSE⁻
8
7
I_TH
C10
220μF
10V
R1
1k
6
C_T
N_GATE
13
Q2
IRFU024
D2
MBR160
C7
3300pF
X7R
C8
470pF
NPO
S_GND
P_GND
R_GND
11
12
14

C2	UNITED CHEMI-CON (AL) LXF63VB331M12.5 x 30 ESR = 0.170Ω I_{RMS} = 1.280A
C4	(TA)
C10	SANYO (OS-CON) 10SA220M ESR = 0.035Ω I_{RMS} = 2.360A
Q1	IR PMOS BV_{DSS} = 60V RDS_{ON} = 0.280Ω C_{RSS} = 65pF Q_g = 19nC
Q2	IR NMOS BV_{DSS} = 60V RDS_{ON} = 0.100Ω C_{RSS} = 79pF Q_g = 28nC
D1	SILICON VBR = 75V
D2	MOTOROLA SCHOTTKY VBR = 60V
R2	KRL NP-1A-C1-0R050J Pd = 1W
L1	COILTRONICS CTX50-2-MP DCR = 0.032Ω MMP CORE

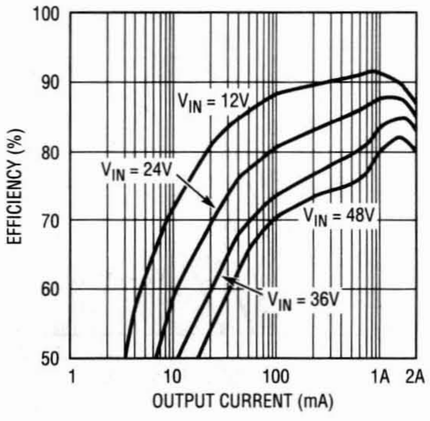
ALL OTHER CAPACITORS ARE CERAMIC

QUIESCENT CURRENT = 1.5mA

TRANSITION CURRENT (BURST MODE™ OPERATION/CONTINUOUS OPERATION) = 570mA

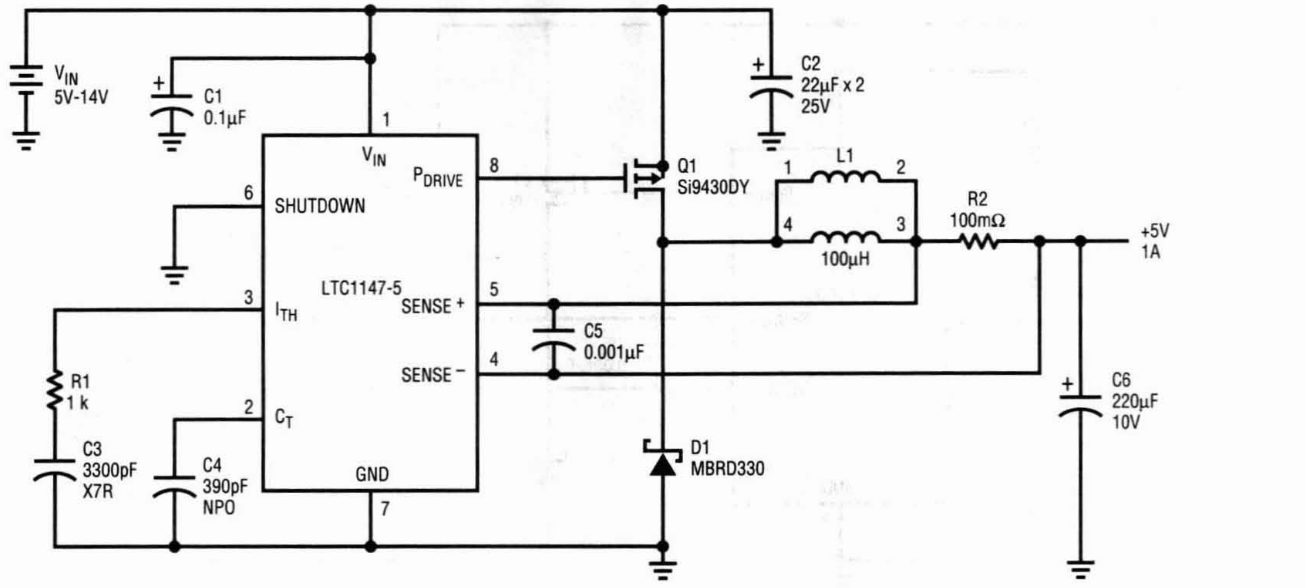
AN54 • TA15

Figure 8A. LTC1149: (10V-48V to 3.3V/2A) High Voltage Buck Converter



AN54 • TA16

Figure 8B. LTC1149: (10V-48V to 3.3V/2A) High Voltage Buck Converter Measured Efficiency



V_IN 5V-14V
C1 0.1μF
C2 22μF x 2 25V
1
V_IN
P_DRIVE
8
Q1 Si9430DY
L1
1
2
4
3
100μH
R2 100mΩ
+5V 1A
6
SHUTDOWN
LTC1147-5
3
I_TH
SENSE⁺
5
C5 0.001μF
SENSE⁻
4
R1 1 k
2
C_T
C6 220μF 10V
C3 3300pF X7R
C4 390pF NPO
GND
7
D1 MBRD330

C2 AVX (TA) TPSD226K025R0200 ESR = 0.200Ω I_{RMS} = 0.775A
C5 AVX (TA) TPSE227K010R0080 ESR = 0.080Ω I_{RMS} = 1.285A
Q1 SILICONIX PMOS BV_{DSS} = 20V RDS_{ON} = 0.100Ω C_{RSS} = 400pF Q_g = 50nC
D1 MOTOROLA SCHOTTKY VBR = 30V
R2 KRL SP-1/2-A1-0R100J Pd = 0.75W
L1 COILTRONICS CTX100-4 DCR = 0.175Ω KOOL Mμ CORE

ALL OTHER CAPACITORS ARE CERAMIC

QUIESCENT CURRENT = 190μA
TRANSITION CURRENT (BURST MODE™ OPERATION/CONTINUOUS OPERATION) = 170mA

AN54 • TA17

Figure 9A. LTC1147: (5V-14V to 5V/1A) Buck Converter with Surface Mount Technology

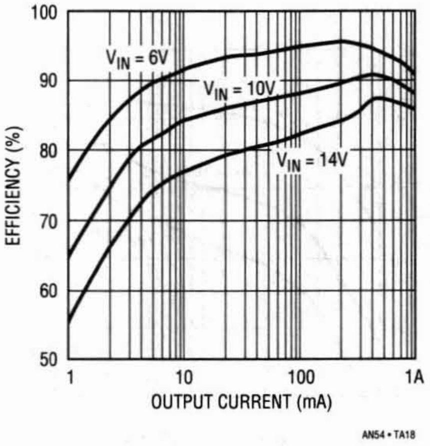
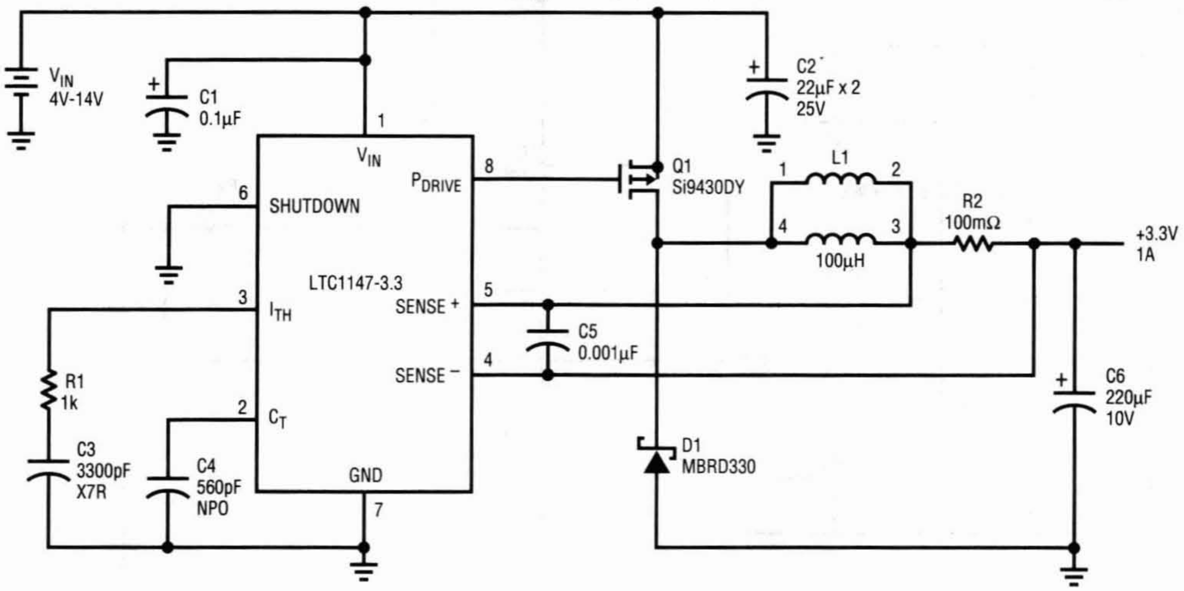


Figure 9B. LTC1147: (5V-14V to 5V/1A) Buck Converter Measured Efficiency

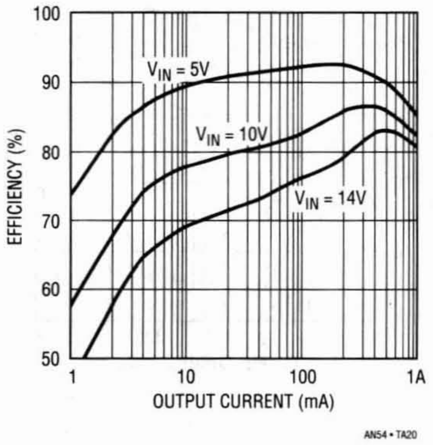

V_{IN}
4V-14V
C1
0.1μF
1
V_{IN}
P_{DRIVE}
8
6
SHUTDOWN
LTC1147-3.3
3
I_{TH}
SENSE +
5
SENSE –
4
R1
1k
2
C_T
C3
3300pF
X7R
C4
560pF
NPO
GND
7
C2
22μF x 2
25V
Q1
Si9430DY
L1
1
2
4
3
100μH
R2
100mΩ
+3.3V
1A
C5
0.001μF
C6
220μF
10V
D1
MBRD330

C2 AVX (TA) TPSD226K025R0200 ESR = 0.200Ω I_{RMS} = 0.775A
C6 AVX (TA) TPSE227K010R0080 ESR = 0.080Ω I_{RMS} = 1.285A
Q1 SILICONIX BV_{DSS} = 20V DCR_{ON} = 0.100Ω C_{RSS} = 400pF Q_g = 50nC
D1 MOTOROLA
R2 KRL SP-1/2-A1-0R100 Pd = 0.75W
L1 COILTRONICS CTX100-4 DCR = 0.175Ω KOOL Mμ CORE

QUIESCENT CURRENT = 170μA
TRANSITION CURRENT (BURST MODE™ OPERATION/CONTINUOUS OPERATION) = 170mA

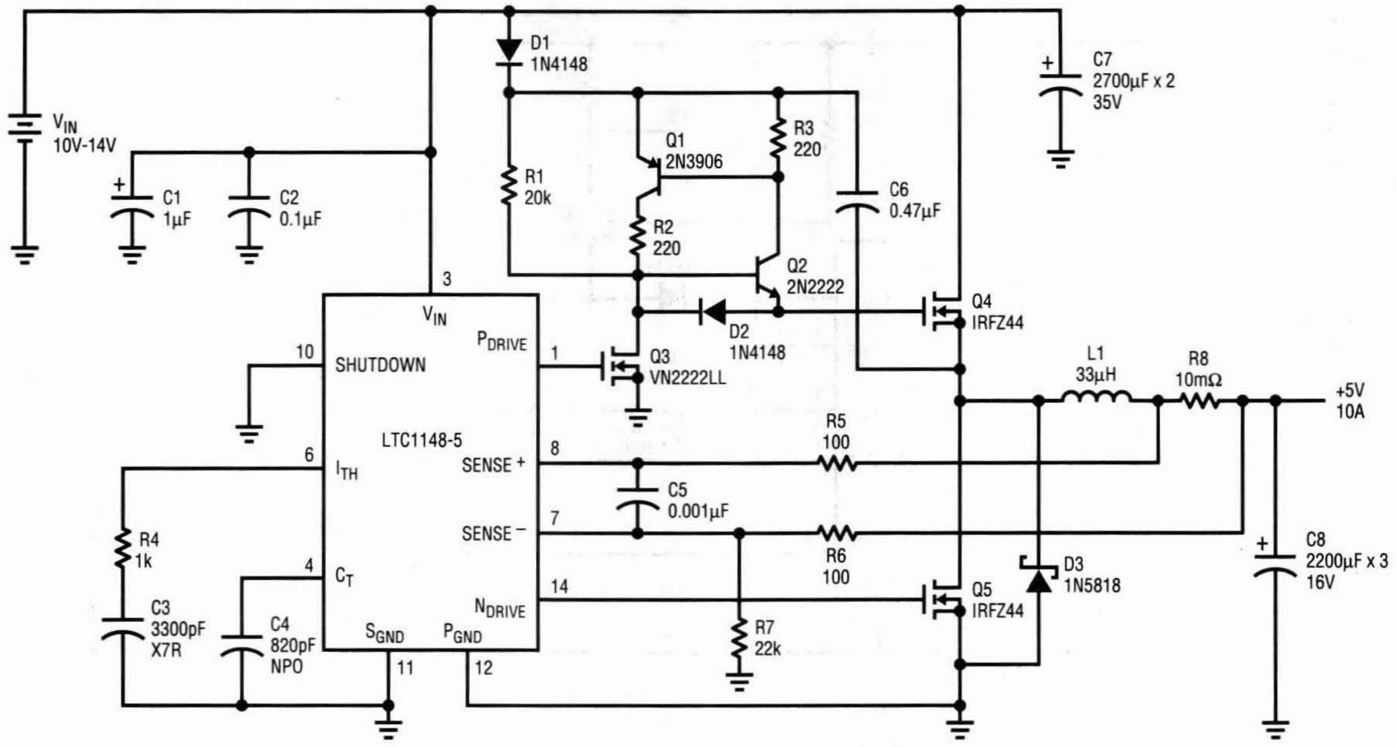
AN54 • TA19

Figure 10A. LTC1147: (4V-14V to 3.3V/1A) Buck Converter with Surface Mount Technology



AN54 • TA20

Figure 10B. LTC1147: (4V-14V to 3.3V/1A) Buck Converter Measured Efficiency


V_{IN}
10V-14V
C1
1µF
C2
0.1µF
D1
1N4148
R1
20k
Q1
2N3906
R2
220
R3
220
Q2
2N2222
C6
0.47µF
C7
2700µF x 2
35V
Q4
IRFZ44
D2
1N4148
Q3
VN2222LL
LTC1148-5
V_{IN}
3
10
SHUTDOWN
P_{DRIVE}
1
6
I_{TH}
SENSE +
8
SENSE –
7
4
C_T
N_{DRIVE}
14
S_{GND}
11
P_{GND}
12
R4
1k
C3
3300pF
X7R
C4
820pF
NPO
C5
0.001µF
R5
100
R6
100
R7
22k
L1
33µH
R8
10mΩ
+5V
10A
Q5
IRFZ44
D3
1N5818
C8
2200µF x 3
16V

C1	(TA)
C7	UNITED CHEMI-CON (AL) LXF35VB272M16 X 40 ESR = 0.018Ω I_{RMS} = 2.900A
C8	NICHICON (AL) UPL1C222MRH ESR = 0.028Ω I_{RMS} = 2.010A
Q4, Q5	IR NMOS BV_{DSS} = 60V DCR_{ON} = 0.028Ω C_{RSS} = 310pF Q_g = 69nC
D1, D2	MOTOROLA SILICON VBR = 75V
D3	MOTOROLA SCHOTTKY VBR = 30V
R8	KRL NP-2A-C1-0R010J Pd = 3W
L1	COILTRONICS CTX33-10-KM DCR = 0.010Ω KOOL Mµ CORE

QUIESCENT CURRENT = 22mA

ALL OTHER CAPACITORS ARE CERAMIC

AN54 • TA21

Figure 11A. LTC1148: (10V-14V to 5V/10A) High Current Buck Converter

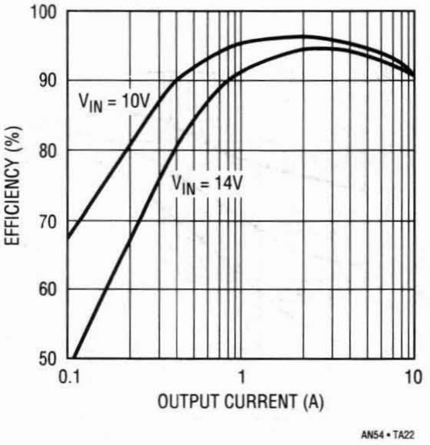
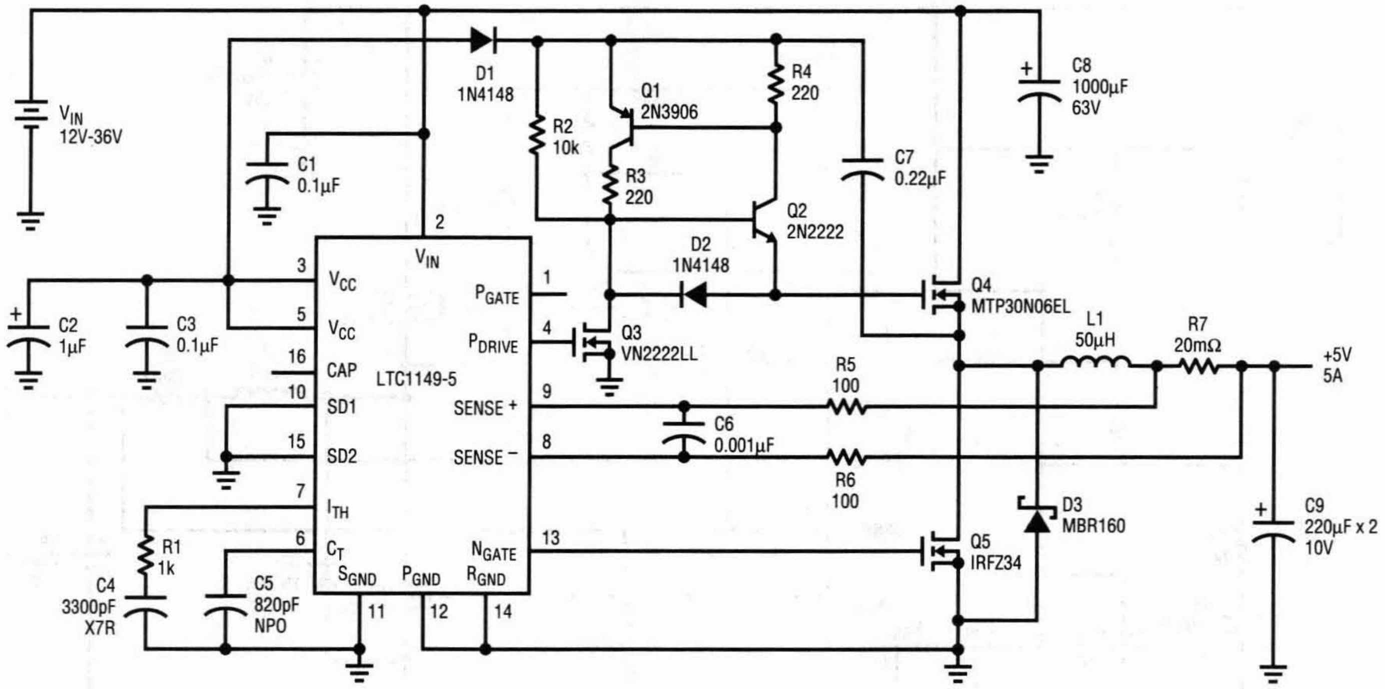


Figure 11B. LTC1148: (10V-14V to 5V/10A) High Current Buck Converter Measured Efficiency



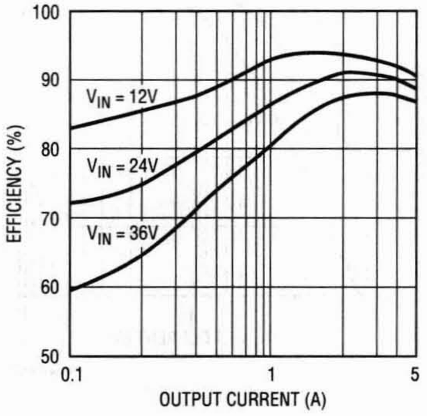
V_{IN} 12V-36V
C1 0.1µF
D1 1N4148
R2 10k
Q1 2N3906
R3 220
R4 220
Q2 2N2222
D2 1N4148
C7 0.22µF
C8 1000µF 63V
C2 1µF
C3 0.1µF
LTC1149-5
V_{IN}
V_{CC}
V_{CC}
CAP
SD1
SD2
I_{TH}
C_T
S_{GND}
P_{GND}
R_{GND}
N_{GATE}
SENSE –
SENSE +
P_{DRIVE}
P_{GATE}
1
2
3
4
5
6
7
8
9
10
11
12
13
14
15
16
Q3 VN2222LL
Q4 MTP30N06EL
L1 50µH
R7 20mΩ
+5V 5A
R5 100
C6 0.001µF
R6 100
D3 MBR160
Q5 IRFZ34
C9 220µF x 2 10V
R1 1k
C4 3300pF X7R
C5 820pF NPO

C2	(TA)
C8	NICHICON (AL) UPL1J102MRH ESR = 0.027Ω I_{RMS} = 2.370A
C9	SANYO (OS-CON) 10SA220M ESR = 0.035Ω I_{RMS} = 2.360A
Q1	PNP BV_{CEO} = 30V
Q2	NPN BV_{CEO} = 40V
Q3	SILICONIX NMOS BV_{DSS} = 60V RDS_{ON} = 5.000Ω
Q4	MOTOROLA NMOS BV_{DSS} = 60V RDS_{ON} = 0.050Ω C_{RSS} = 100pF Q_g = 40nC
Q5	IR NMOS BV_{DSS} = 60V RDS_{ON} = 0.050Ω C_{RSS} = 100pF Q_g = 32nC
D1, D2	SILICON VBR = 75V
D3	MOTOROLA SCHOTTKY VBR = 60V
R7	KRL NP-2A-C1-0R020J Pd = 3W
L1	COILTRONICS CTX50-5-52 DCR = 0.021Ω #52 IRON POWDER CORE

ALL OTHER CAPACITORS ARE CERAMIC

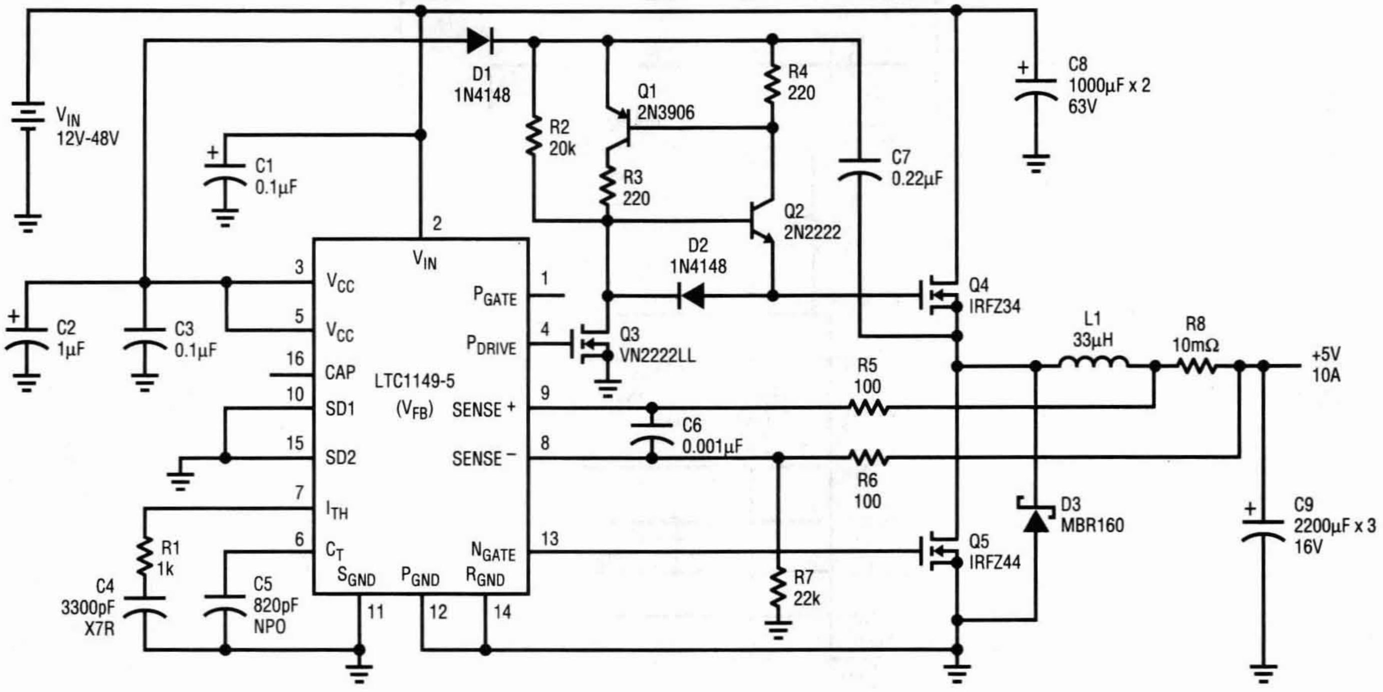
AN54 • TA23

Figure 12A. LTC1149: (12V-36V to 5V/5A) High Current, High Voltage Buck Converter



AN54 • TA24

Figure 12B. LTC1149: (12V-36V to 5V/5A) High Current, High Voltage Buck Converter Measured Efficiency

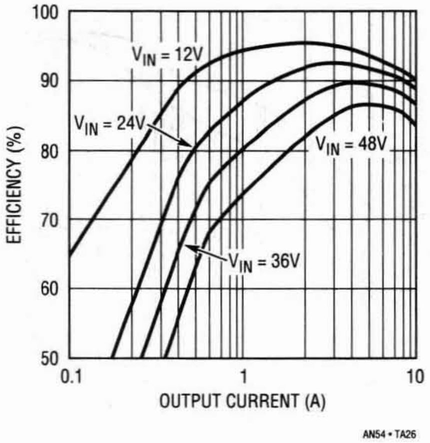

VIN
12V-48V
C1
0.1µF
D1
1N4148
R2
20k
Q1
2N3906
R4
220
R3
220
Q2
2N2222
C7
0.22µF
C8
1000µF x 2
63V
D2
1N4148
Q4
IRFZ34
Q3
VN2222LL
C2
1µF
C3
0.1µF
LTC1149-5
(VFB)
VIN
VCC
VCC
CAP
SD1
SD2
ITH
CT
SGND
PGND
RGND
PGATE
PDRIVE
SENSE +
SENSE −
NGATE
2
3
5
16
10
15
7
6
11
12
14
1
4
9
8
13
L1
33µH
R8
10mΩ
+5V
10A
R5
100
C6
0.001µF
R6
100
D3
MBR160
C9
2200µF x 3
16V
Q5
IRFZ44
R7
22k
R1
1k
C4
3300pF
X7R
C5
820pF
NPO

C2	(TA)	
C8	NICHICON (AL) UPL1J102MRH ESR = 0.027Ω I_{RMS} = 2.370A	
C9	NICHICON (AL) UPL1C222MRH ESR = 0.028Ω I_{RMS} = 2.010A	
Q1	PNP BV_{CEO} = 30V	
Q2	NPN BV_{CEO} = 40V	
Q3	SILICONIX NMOS BV_{DSS} = 60V RDS_{ON} = 5.000Ω	
Q4	IR NMOS BV_{DSS} = 60V RDS_{ON} = 0.050Ω C_{RSS} = 100pF Q_g = 32nC	
Q5	IR NMOS BV_{DSS} = 60V RDS_{ON} = 0.028Ω C_{RSS} = 310pF Q_g = 69nC	
D1, D2	SILICON VBR = 75V	
D3	MOTOROLA SCHOTTKY VBR = 60V	
R8	KRL NP-2A-C1-0R010J Pd = 3W	
L1	COILTRONICS CTX33-10-KM DCR = 0.010Ω KOOL Mµ CORE	QUIESCENT CURRENT = 26mA

ALL OTHER CAPACITORS ARE CERAMIC

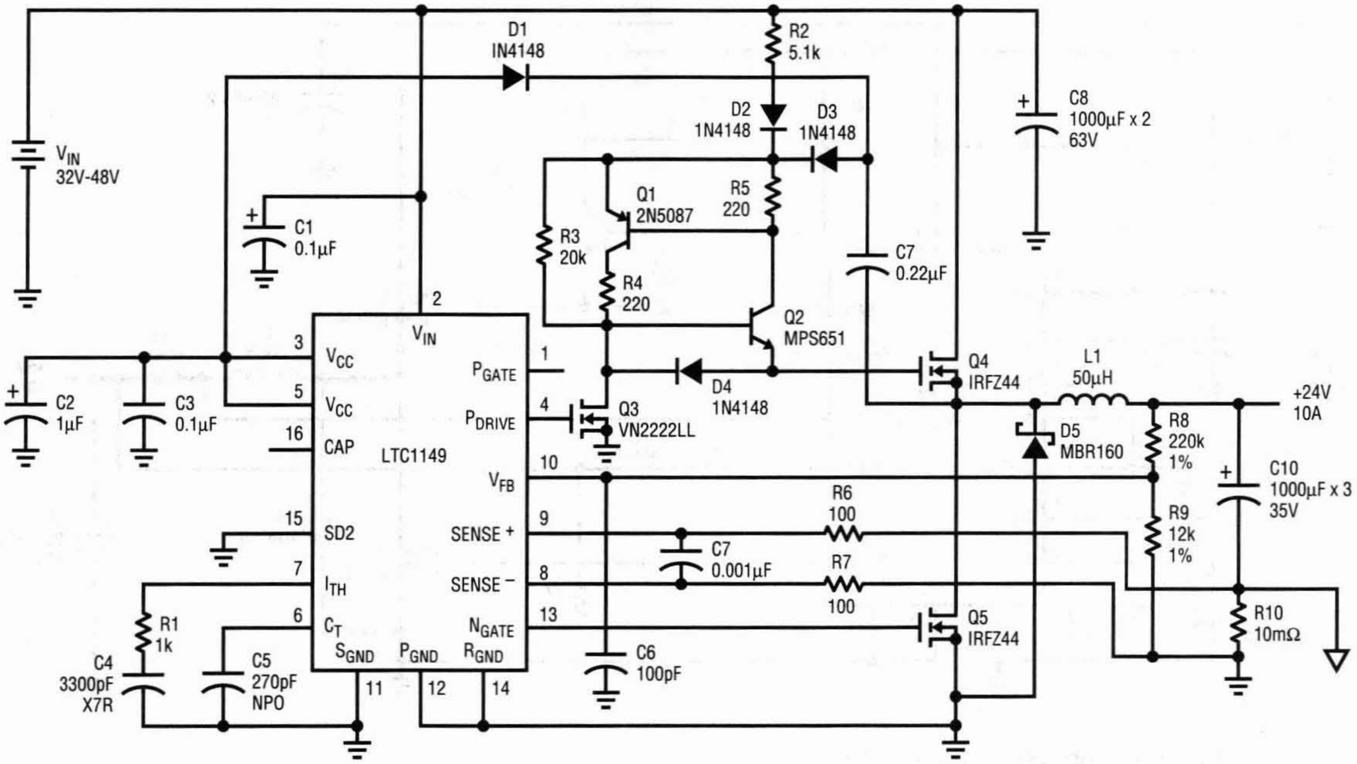
AN54 • TA25

Figure 13A. LTC1149: (12V-48V to 5V/10A) High Current, High Voltage Buck Converter



AN54 • TA26

Figure 13B. LTC1149: (12V-48V to 5V/10A) High Current, High Voltage Buck Converter Measured Efficiency


D1
1N4148
R2
5.1k
D2
1N4148
D3
1N4148
C8
1000µF x 2
63V
VIN
32V-48V
C1
0.1µF
Q1
2N5087
R5
220
R3
20k
R4
220
C7
0.22µF
Q2
MPS651
2
VIN
3
VCC
5
VCC
16
CAP
LTC1149
1
PGATE
4
PDRIVE
10
VFB
15
SD2
9
SENSE +
7
ITH
8
SENSE −
6
CT
13
NGATE
SGND
PGND
RGND
11
12
14
C2
1µF
C3
0.1µF
Q3
VN2222LL
D4
1N4148
Q4
IRFZ44
L1
50µH
+24V
10A
D5
MBR160
R8
220k
1%
C10
1000µF x 3
35V
R6
100
C7
0.001µF
R7
100
R9
12k
1%
R10
10mΩ
Q5
IRFZ44
R1
1k
C4
3300pF
X7R
C5
270pF
NPO
C6
100pF

C2	(TA)
C9	NICHICON (AL) UPL1J102MRH ESR = 0.027Ω I_{RMS} = 2.370A
C10	NICHICON (AL) UPL1V102MRH ESR = 0.029Ω I_{RMS} = 1.980A
Q4, Q5	IR NMOS BV_{DSS} = 60V RDS_{ON} = 0.028Ω C_{RSS} = 310pF Q_g = 69nC
Q1	PNP BV_{CEO} = 50V
Q2	NPN BV_{CEO} =
D1, D2, D3, D4	SILICON VBR = 75V
D5	MOTOROLA SCHOTTKY VBR = 60V
R10	KRL NP-2A-C1-0R010J Pd = 3W
L1	COILTRONICS CTX50-10-KM DCR = 0.010Ω KOOL Mµ CORE

ALL OTHER CAPACITORS ARE CERAMIC

V_{OUT} = 1.25V (1 + R8/R9)

QUIESCENT CURRENT = 2mA

TRANSITION CURRENT (BURST MODE™ OPERATION/CONTINUOUS OPERATION) = 1.5A

AN54 • TA27

Figure 14A. LTC1149: (32V-48V to 24V/10A) High Current, High Voltage Buck Converter

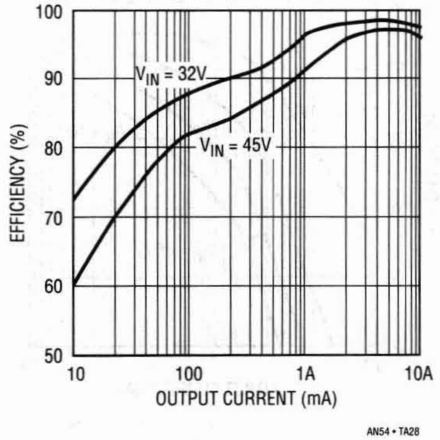
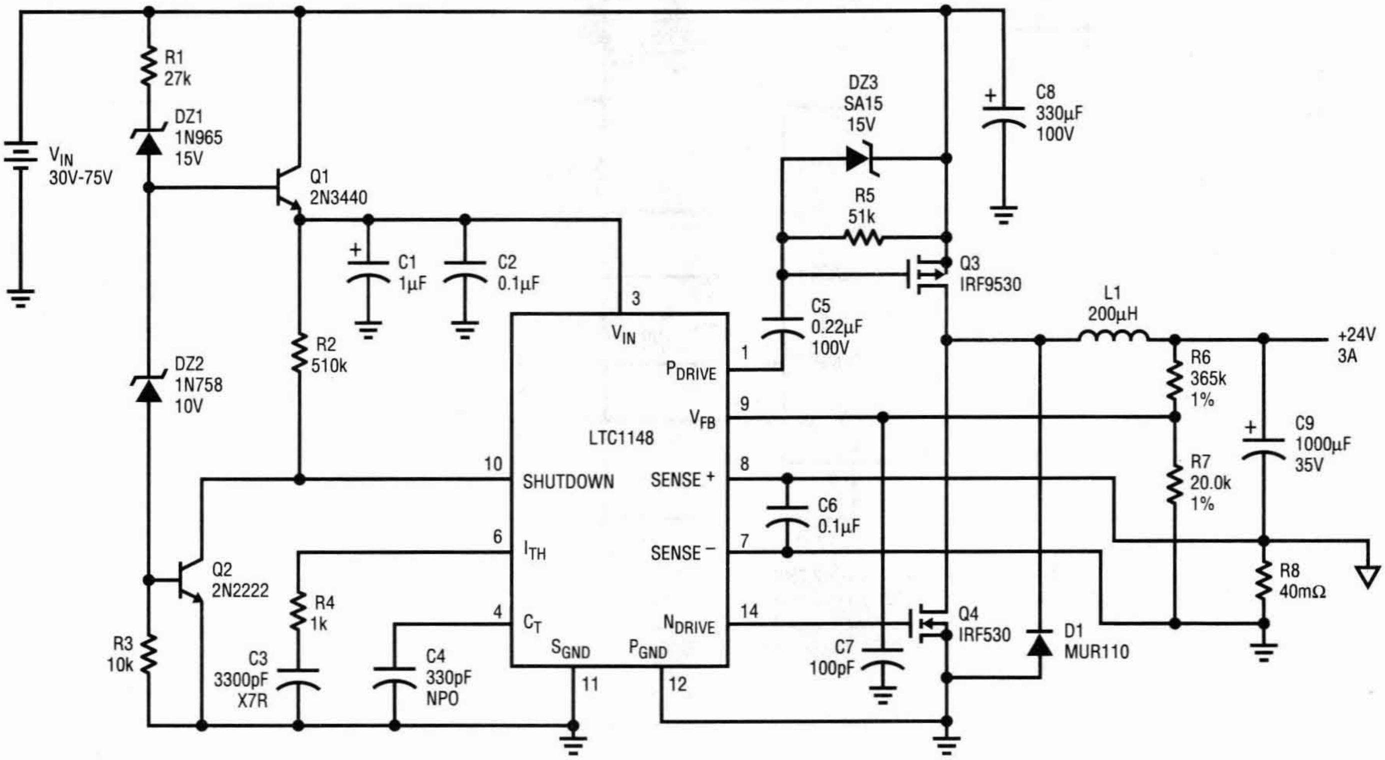


Figure 14B. LTC1149: (32V-48V to 24V/10A) High Current, High Voltage Buck Converter Measured Efficiency


R1
27k
DZ1
1N965
15V
V_{IN}
30V-75V
Q1
2N3440
DZ3
SA15
15V
C8
330μF
100V
R5
51k
Q3
IRF9530
C1
1μF
C2
0.1μF
3
L1
200μH
C5
0.22μF
100V
+24V
3A
V_{IN}
1
P_{DRIVE}
R6
365k
1%
DZ2
1N758
10V
R2
510k
9
V_{FB}
C9
1000μF
35V
LTC1148
10
SHUTDOWN
8
SENSE +
R7
20.0k
1%
C6
0.1μF
6
I_{TH}
7
SENSE −
Q2
2N2222
R8
40mΩ
R4
1k
4
C_T
14
N_{DRIVE}
Q4
IRF530
D1
MUR110
R3
10k
C3
3300pF
X7R
C4
330pF
NPO
S_{GND}
P_{GND}
C7
100pF
11
12

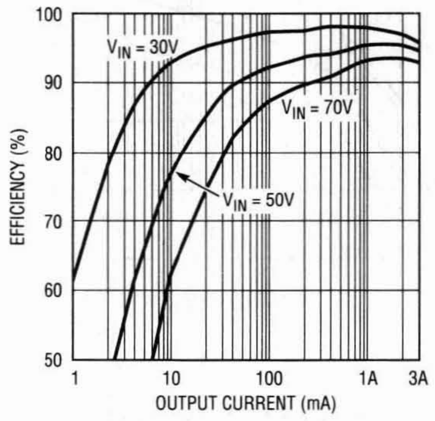
C1	(TA)
C8	UNITED CHEMI-CON (AL) KMF100VB221M16 X 25 ESR = 0.090Ω I_{RMS} = 1.440A
C9	UNITED CHEMI-CON (AL) LXF35VB10212.5 X 30 ESR = 0.030Ω I_{RMS} = 1.950A
Q1	MOTOROLA NPN $V(BR)_{CEO}$ = 200V Pd = 1W hFE = 40
Q2	MOTOROLA NPN $V(BR)_{CEO}$ = 30V hFE = 50
Q3	IR PMOS BV_{DSS} = 100V DCR_{ON} = 0.250Ω C_{RSS} = 100pF Q_g = 25nC
Q4	IR NMOS BV_{DSS} = 100V DCR_{ON} = 0.120Ω C_{RSS} = 44pF Q_g = 17nC
DZ3	MOTOROLA V_Z = 15V Pd = 3W
D1	MOTOROLA SILICON VBR = 100V
R7	KRL NP-1A-C1-0R040J Pd = 1W
L1	COILTRONICS CTX200-3-KM DCR = 0.044Ω KOOL Mμ CORE

V_{OUT} = 1.25V (1 + R6/R7)
QUIESCENT CURRENT = 1mA
TRANSITION CURRENT (BURST MODE™ OPERATION/CONTINUOUS OPERATION) = 340mA

ALL OTHER CAPACITORS ARE CERAMIC

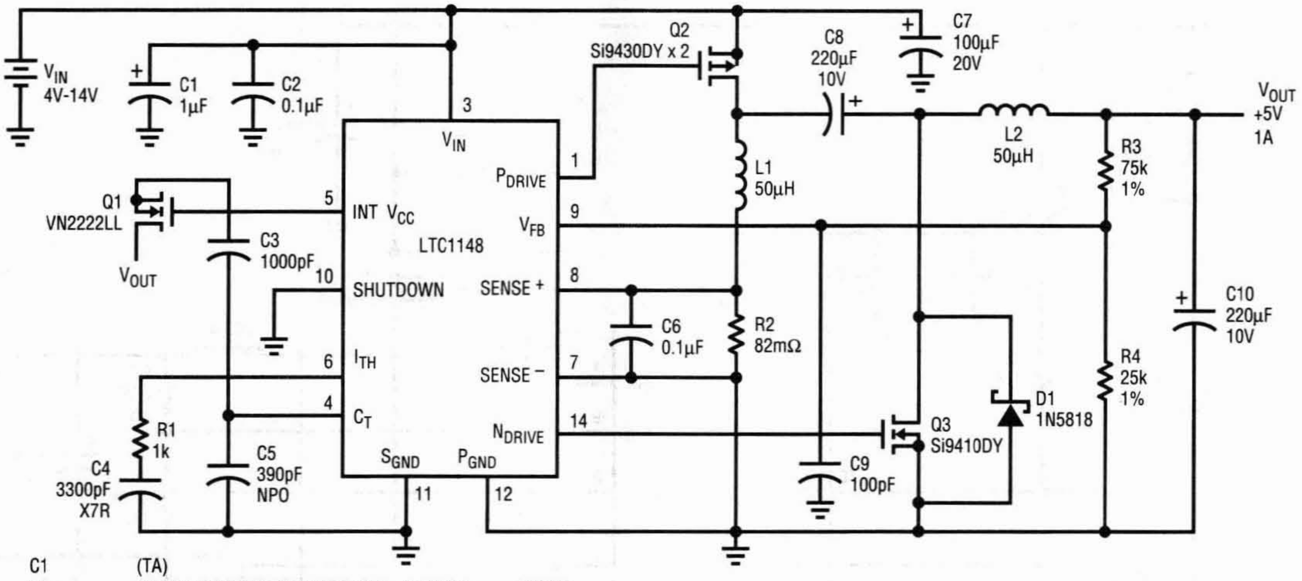
AN54 • TA29

Figure 15A. LTC1148: (30V-75V to 24V/3A) High Voltage Buck Converter



AN54 • TA30

Figure 15B. LTC1148: (30V-75V to 24V/3A) High Voltage Buck Converter Measured Efficiency


V_{IN}
4V-14V
C1
1µF
C2
0.1µF
3
V_{IN}
Q2
Si9430DY x 2
C8
220µF
10V
C7
100µF
20V
V_{OUT}
+5V
1A
1
P_{DRIVE}
L1
50µH
L2
50µH
R3
75k
1%
Q1
VN2222LL
5
INT V_{CC}
V_{FB}
9
C3
1000pF
LTC1148
V_{OUT}
10
SHUTDOWN
SENSE +
8
C10
220µF
10V
C6
0.1µF
R2
82mΩ
6
I_{TH}
SENSE –
7
R4
25k
1%
D1
1N5818
4
C_T
R1
1k
N_{DRIVE}
14
Q3
Si9410DY
C4
3300pF
X7R
C5
390pF
NPO
S_{GND}
P_{GND}
C9
100pF
11
12

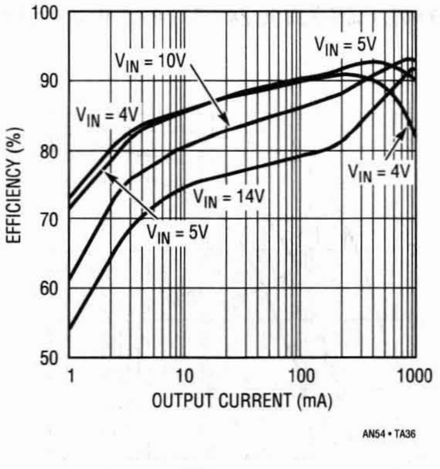
C1	(TA)
C7	SANYO (OS-CON) 20SA100M ESR = 0.037Ω I_{RMS} = 2.250A
C8, C10	SANYO (OS-CON) 10SA220M ESR = 0.035Ω I_{RMS} = 2.360A
Q2	SILICONIX PMOS BV_{DSS} = 20V RDS_{ON} = 0.100Ω C_{RSS} = 400pF Q_g = 50nC
Q3	SILICONIX NMOS BV_{DSS} = 30V RDS_{ON} = 0.050Ω C_{RSS} = 160pF Q_g = 30nC
D1	MOTOROLA SCHOTTKY VBR = 30V
R2	KRL NP-1A-C1-0R082J Pd = 1W
L1	COILTRONICS 082

ALL OTHER CAPACITORS ARE CERAMIC

V_{OUT} = 1.25V (1 + R2/R3)
QUIESCENT CURRENT = 200µA
TRANSITION CURRENT (BURST MODE™ OPERATION/
CONTINUOUS OPERATION) = 250mA/V_{IN} = 5V

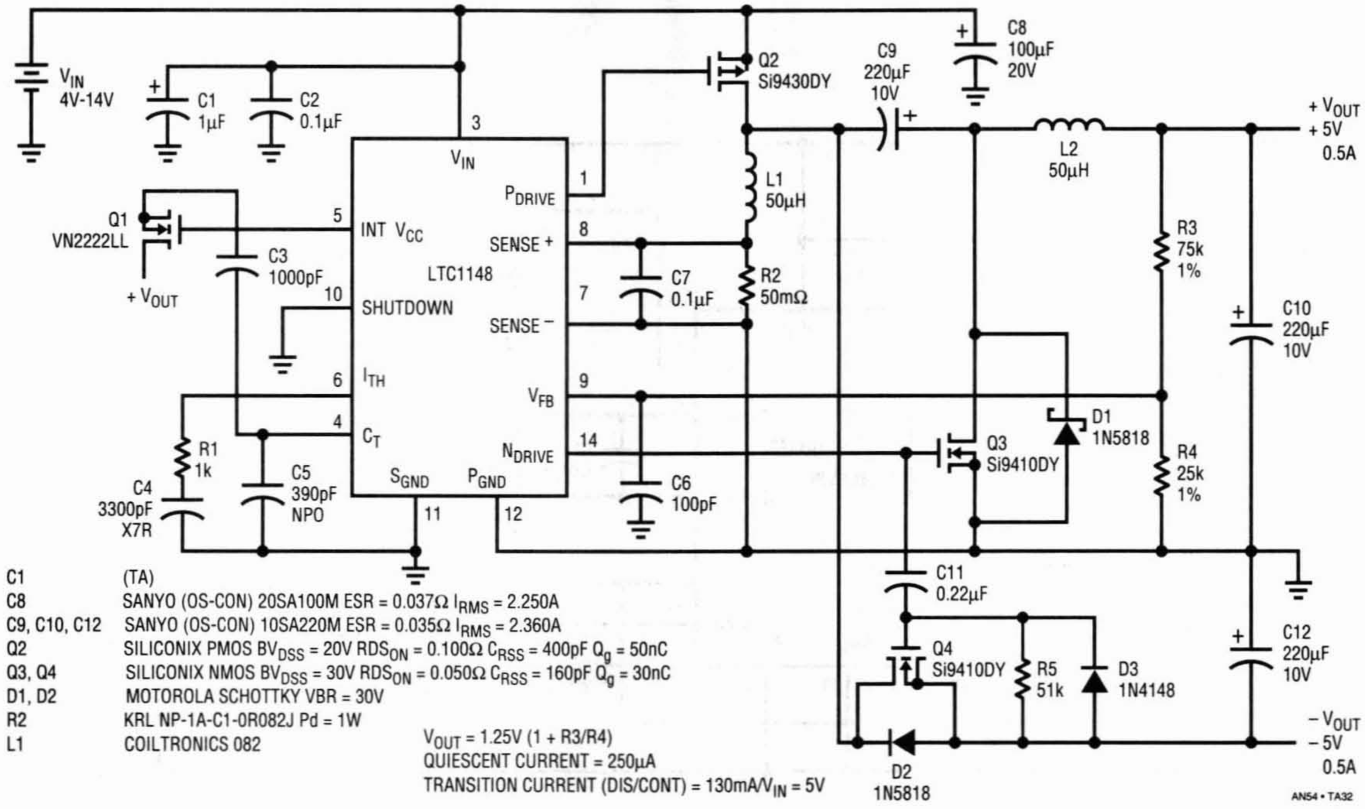
AN54 • TA31

Figure 16A. LTC1148: (4V-14V to 5V/1A) Buck-Boost Converter



AN54 • TA36

Figure 16B. LTC1148: (4V-14V to 5V/1A) Buck-Boost Converter Measured Efficiency


VIN
4V-14V
C1
1µF
C2
0.1µF
C8
100µF
20V
Q2
Si9430DY
C9
220µF
10V
+VOUT
+5V
0.5A
3
VIN
1
PDRIVE
L1
50µH
L2
50µH
Q1
VN2222LL
5
INT VCC
8
SENSE+
C3
1000pF
LTC1148
C7
0.1µF
R2
50mΩ
R3
75k
1%
+VOUT
10
SHUTDOWN
7
SENSE−
C10
220µF
10V
6
ITH
9
VFB
D1
1N5818
4
CT
NDRIVE
14
Q3
Si9410DY
R1
1k
R4
25k
1%
C4
3300pF
X7R
C5
390pF
NPO
SGND
PGND
11
12
C6
100pF
C11
0.22µF
Q4
Si9410DY
R5
51k
D3
1N4148
C12
220µF
10V
−VOUT
−5V
0.5A
D2
1N5818
AN54 • TA32

C1	(TA)
C8	SANYO (OS-CON) 20SA100M ESR = 0.037Ω I_{RMS} = 2.250A
C9, C10, C12	SANYO (OS-CON) 10SA220M ESR = 0.035Ω I_{RMS} = 2.360A
Q2	SILICONIX PMOS BV_{DSS} = 20V RDS_{ON} = 0.100Ω C_{RSS} = 400pF Q_g = 50nC
Q3, Q4	SILICONIX NMOS BV_{DSS} = 30V RDS_{ON} = 0.050Ω C_{RSS} = 160pF Q_g = 30nC
D1, D2	MOTOROLA SCHOTTKY VBR = 30V
R2	KRL NP-1A-C1-0R082J Pd = 1W
L1	COILTRONICS 082

V_{OUT} = 1.25V (1 + R3/R4)
QUIESCENT CURRENT = 250µA
TRANSITION CURRENT (DIS/CONT) = 130mA/V_{IN} = 5V

Figure 17A. LTC1148: (4V-14V to +5V/0.5A, –5V/0.5A) Split Supply Converter

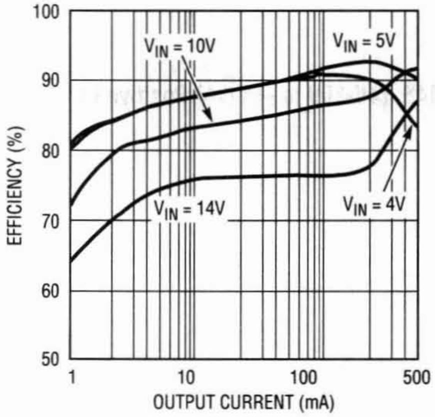
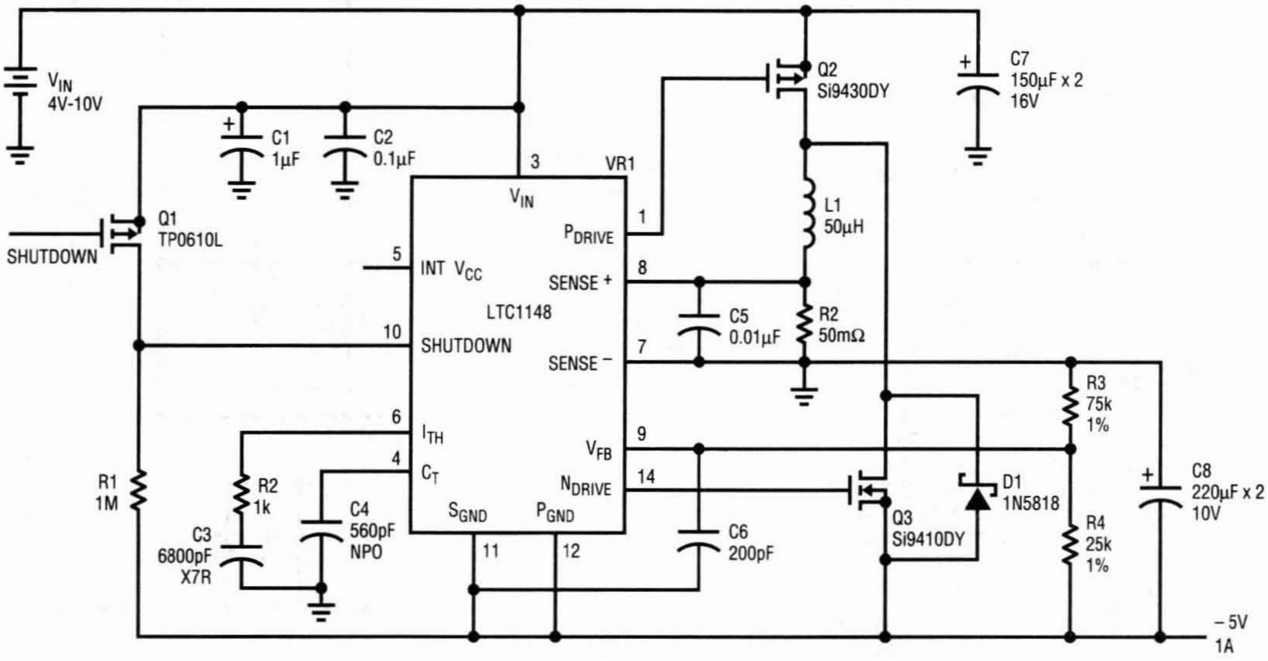


Figure 17B. LTC1148: (4V-14V to +5V/0.5A, –5V/0.5A) Split Supply Converter Measured Efficiency


VIN
4V-10V
C1
1µF
C2
0.1µF
Q1
TP0610L
SHUTDOWN
R1
1M
C3
6800pF
X7R
R2
1k
C4
560pF
NPO
3
VR1
VIN
PDRIVE
1
5
INT VCC
LTC1148
SENSE +
8
10
SHUTDOWN
SENSE –
7
6
ITH
VFB
9
4
CT
NDRIVE
14
SGND
PGND
11
12
Q2
Si9430DY
C7
150µF x 2
16V
L1
50µH
C5
0.01µF
R2
50mΩ
R3
75k
1%
D1
1N5818
Q3
Si9410DY
R4
25k
1%
C6
200pF
C8
220µF x 2
10V
– 5V
1A

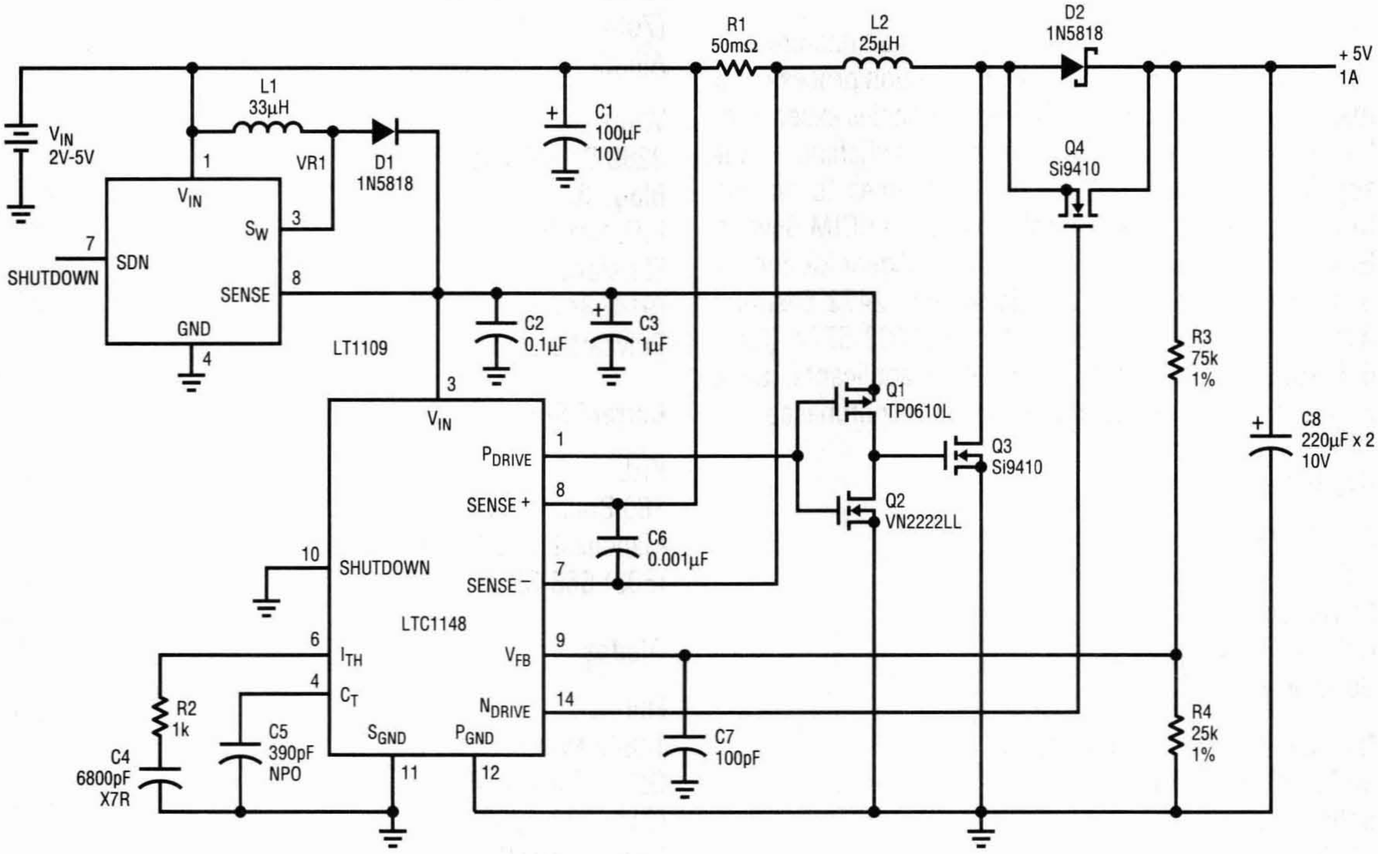
C1	(TA)
C7	SANYO (OS-CON) 16SA150M ESR = 0.035Ω I_{RMS} = 2.280A
C8	SANYO (OS-CON) 10SA220M ESR = 0.035Ω I_{RMS} = 2.360A
Q2	SILICONIX PMOS BV_{DSS} = 20V RDS_{ON} = 0.100Ω C_{RSS} = 400pF Q_g = 50nC
Q3	SILICONIX NMOS BV_{DSS} = 30V RDS_{ON} = 0.050Ω C_{RSS} = 160pF Q_g = 30nC
D1	MOTOROLA SCHOTTKY VBR = 30V
R2	KRL NP-1A-C1-0R050J
L1	COILTRONICS CTX50-2-MP DCR = 0.032Ω MMP CORE

V_{OUT} = 1.25V (1 + R3/R4)

ALL OTHER CAPACITORS ARE CERAMIC

AN54 • TA33

Figure 18. LTC1148: (4V-10V to –5V/1A) Positive to Negative Converter


R1
50mΩ
L2
25μH
D2
1N5818
+5V
1A
L1
33μH
V_{IN}
2V-5V
1
VR1
D1
1N5818
+
C1
100μF
10V
Q4
Si9410
V_{IN}
3
S_W
7
SHUTDOWN
SDN
8
SENSE
GND
4
LT1109
+
C2
0.1μF
C3
1μF
R3
75k
1%
3
V_{IN}
Q1
TP0610L
P_{DRIVE}
1
Q3
Si9410
+
C8
220μF x 2
10V
SENSE +
8
Q2
VN2222LL
C6
0.001μF
10
SHUTDOWN
SENSE −
7
LTC1148
6
I_{TH}
V_{FB}
9
4
C_T
N_{DRIVE}
14
R2
1k
R4
25k
1%
C5
390pF
NPO
S_{GND}
P_{GND}
C7
100pF
C4
6800pF
X7R
11
12

C1	SANYO (OS-CON) 10SA100M ESR = 0.045Ω I_{RMS} = 1.870A
C3	(TA)
C8	SANYO (OS-CON) 10SA220M ESR = 0.035Ω I_{RMS} = 2.360A
Q3, Q4	SILICONIX NMOS BV_{DSS} = 30V RDS_{ON} = 0.050Ω C_{RSS} = 160pF Q_g = 30nC
D1, D2	MOTOROLA SCHOTTKY VBR = 30V
R2	KRL SL-1-C1-0R050J Pd = 1W
L1	COILTRONICS CTX33-1 DCR = 0.220Ω KOOL Mμ CORE
L2	COILTRONICS

$V_{OUT} = 1.25V (1 + R3/R4)$

AN54 • TA34

Figure 19. LTC1148: (2V-5V to 5V/1A) Boost Converter

WARNING!!!
This is a preliminary circuit!
Contact Brian Huffman at the factory if you have any problems.

APPENDIX A

SUGGESTED MANUFACTURERS

Linear Technology provides this list of manufacturers to get you started in your component selection process. We make no claims about any of these companies except that they provide components necessary in switching power supplies. There are many more companies to choose from; for a more complete list refer to the PCIM Buyer's Guide. PCIM (Power Conversion & Intelligent Motion) is published by Intertec International Inc., 2472 Eastman Ave., Bldg. 33-34, Ventura, California 93003-5774, (805) 650-7070. PCIM is free to qualified applicants. Back issues, such as the Buyer's Guide can be purchased.

Capacitors

AVX Corporation
P.O. Box 867
Myrtle Beach, SC 29577
(803) 448-9411
Surface Mount Tantalum

Nichicon (America) Corporation
927 East State Parkway
Schaumburg, IL 60173
(708) 843-7500
Aluminum Electrolytic

Philips Components Disc. Prod. Div.
Division Headquarters
2001 W. Blue Heron Blvd.
Riviera Beach, FL 33404
(800) 881-3200
Low ESR filter capacitors-Solid Aluminum
Electrolytic Capacitors

Sanyo Video Components (USA) Corp.
2001 Sanyo Ave.
San Diego, CA 92073
(619) 661-6835
Low ESR filter capacitors-Solid Aluminum
Electrolytic Capacitors (OS-CON)

United Chemi-Con, Inc.
9801 West Higgins Road
Rosemount, IL 60018
(708) 696-2000
Aluminum Electrolytic

Wima
2269 Saw Mill River Rd.
Bldg. 4C
P.O. Box 217
Elmsford, NY 10523
(914) 347-2474
Polycarbonate Film

Current Sense Resistors

KRL
160 Bouchard Street
Manchester, NH 03103
(603) 668-3210

Diodes

Fuji
14368 Proton Rd.
Dallas, TX 75244
(214) 233-1589
Low Current Schottkys

General Instruments
600 W John St. CS620
Hickville, NY 11802
(516) 933-3333

Motorola Inc.
3102 North 56th St.
MS 56-126
Phoenix, AZ 85018
(800) 521-6274
Full Line

Philips Components Disc. Prod. Div.
Division Headquarters
2001 W. Blue Heron Blvd.
Riviera Beach, FL 33404
(800) 881-3200

Ferrite Beads

Fair-Rite Products Corp.
1 Commerial Row
P.O. Box J
Wallkill, NY 12589
(914) 895-2055

Toshiba America Elec. Components
9775 Toledo Way
Irvine, CA 92718
(714) 455-2000

Heat Sinks

Aavid Engineering, Inc.
One Kool Path Box 400
Laconia, NH 03247
(603) 528-3400

Thermalloy
2021 W. Valley View Lane
P.O. Box 810839
Dallas, TX 75381
(214) 243-4321

Mounting Hardware

Bergquist
5300 Edina Industrial Blvd.
Minneapolis, MN 55439
(612) 835-2322
Thermally Conductive Insulators

Stockwell Rubber
4749 Tolbut St.
Philadelphia, PA 19136
(800) 523-0123
Thermally Conductive Insulators

Thermalloy
2021 W. Valley View Lane
P.O. Box 810839
Dallas, TX 75381
(214) 243-4321
Power Sockets, Thermal Compounds, and Adhesives
Thermally Conductive Insulators, Mounting Kits

Power MOSFETs

International Rectifier Corp.
233 Kansas St.
El Segundo, CA 90245
(310) 322-3331

Motorola Inc.
3102 North 56th St.
MS 56-126
Phoenix, AZ 85018
(800) 521-6274

Siliconix
2201 Laurelwood Rd.
Santa Clara, CA 96056
(800) 554-5565

Inductors and Transformers

Caddell-Burns
285 East Second St.
Mineola, NY 11501
(516) 746-2310

Coilcraft
1102 Silver Lake Rd.
Cary, IL 60013
(800) 322-2645

Coiltronics
984 SW 13th Ct.
Pompano Beach, FL 33069
(305) 781-8900
Full Line including Surface Mount Inductors

Gowanda Electronics Corp.
1 Industrial Place
Gowanda, NY 14070
(716) 532-2234

Hurricane Electronics Lab
P.O. Box 1280
Hurricane Industrial Park
Hurricane, UT 84737
(801) 635-2003

Murata Erie North America
2200 Lake Park Drive
Smyrna, GA 30080
(404) 436-1300

Renco
60 E. Jefryn Blvd.
Deerpark, NY 11729
(516) 586-5566

Sumida Electronic
637 E. Golf Rd. Suite 209
Arlington Heights, IL 60005
(708) 956-0666

TDK Corp. of America
1600 Feehanville Dr.
Mt. Prospect, IL 60056
(708) 803-6100

Toko America Incorparated
1250 Feehanville Dr.
Mount Propsect, IL 60056
(312) 297-0700

Magnetic Materials

Fair-Rite Products Corp.
1 Commerial Row
P.O. Box J Wallkill, NY 12589
(914) 895-2055
Ferrite

Micrometals, Inc.
1190 N. Hawk Circle
Anaheim, CA 92807
(800) 356-5977
Powdered Iron

Magnetics Div. Spang & Co
P.O. Box 391
Bulter, PA 16003-0391
(412) 282-8282
Powdered Iron, Molypermalloy, Powdered High Flux,
Kool Mμ, Ferrite

Philips Components Disc. Prod. Div. Materials Group
5083 King Highway
Saugerties, NY 12477
(914) 246-2811
Ferrite

Pyroferric International, Inc.
200 Madison St.
Toledo, IL 62468
(217) 849-3300
Powdered Iron

Siemens Components, Inc.
186 Wood Ave. S
Iselin, NJ 08830
(908) 906-4300
Ferrite

TDK Corp. of America
1600 Feehanville Dr.
Mt. Prospect, IL 60056
(708) 803-6100
Ferrite

Bipolar Transistors

Motorola Inc.
3102 North 56th St.
MS 56-126
Phoenix, AZ 85018
(800) 521-6274
Full Line

Zetex
87 Modular Ave.
Commack, NY 11725
(516) 543-7100
High Gain Bipolar Switching Transistors
including Surface Mount Devices

SECTION 2: DESIGN NOTES

SECTION 2—DESIGN NOTES

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DN67 A 1mV Offset, Clock-Tunable, Monolithic 5-Pole Lowpass Filter DN67-1
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DESIGN NOTES

Number 33 in a series from Linear Technology Corporation *April, 1990*

Powering 3.3V Digital Systems

Dennis O'Neill

The new generation of high density digital devices requiring 3.3V power supplies impose some unique constraints on power supply designers. In nearly all cases the computers using these devices already have a 5V system supply. Deriving the 3.3V supply from the existing 5V rail permits system upgrades with a simple on-card solution. In many cases the 5V rail is the only supply available, mandating this approach. The first decision to be made is whether to use a switching regulator or a linear regulator? Switchers have a clear efficiency advantage when there is a large difference between the input and output voltage, but that advantage diminishes as the input voltage approaches the output voltage.

Simple calculations show that the efficiency of a switcher is marginally better in this application. Assuming a nominal input voltage of 5.0V and an output voltage of 3.3V, the efficiency of a linear regulator, (LT1083 type Figure 1A), independent of output current, is simply 3.3V/5.0V = 66%. For a switcher (Figure 1B) the efficiency is tougher to calculate. With only 5V available a PNP switch must be used, a MOSFET is not practical due to its gate drive requirements. The average inductor current will be equal to the load current. The duty cycle is determined by:

$$DC = (V_{OUT} + V_D)/(V_{IN} - V_{SAT} - V_D)$$

where $V_{OUT} = 3.3V$, $V_{IN} = 5.0V$, $V_{SAT} = V_{CE}$ sat. of Q_S, V_D = forward voltage of D1.

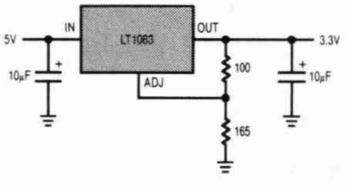


Figure 1A. Linear Regulator

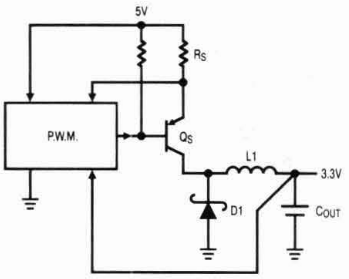


Figure 1B. Buck Switching Regulator

Assuming V_{CE} sat. of Q_S to be 0.6V at a forced Beta of 10 and the forward voltage of D1 to be 0.6V, (using a Schottky diode; a silicon diode would be closer to 1V at rated current), the formula indicates an 80% duty cycle. Significant power losses are listed below.

Switch Saturation Voltage	(0.6V) (1.0A) (80%) = 0.48W
Switch Base Current	(5.0V) (0.1A) (80%) = 0.40W
Diode Forward Voltage	(0.6V) (1.0A) (20%) = 0.12W
Inductor Voltage	(0.1V) (1.0A) (100%) = 0.10W
Switching Transients	≈ 0.10W
R_{SENSE} Voltage	(0.1V) (1.0A) (80%) = 0.08W
P.W.M. Circuit	(5.0V) (0.02A) (100%) = 0.10W
	1.38W

The efficiency is Power Out/Power In = 3.3W/(1.38W + 3.3W) ≈ 70%. This says that the switcher could be more efficient, but by a small margin (4%). Other considerations, such as noise filtering, further decrease the switchers efficiency. In addition, circuit design becomes complex. For example, short circuit sensing in the emitter lead of Q_S might require generating another supply greater than 5V to power the sense amplifier. Also, some form of adaptive base drive is needed to maintain efficiency at light loads.

When the small efficiency gain of a switcher is balanced against the advantages of a linear regulator (superior transient response, low noise, and ease of design) it becomes clear that the linear regulator is the best choice in this application.

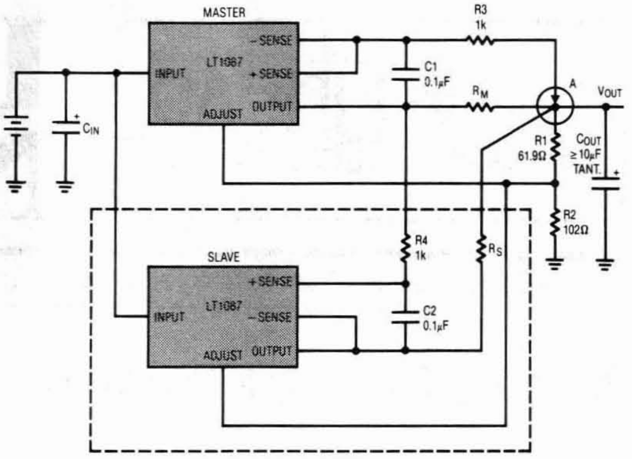
Regulator Design

Figure 1A shows a basic linear regulator circuit utilizing an LT1083 adjustable low dropout regulator. These devices, specified for dropout voltage at several points over their operating current range, are ideal for this application. Nominal tolerance on the 5V rail in most systems is ±5% (4.75V to 5.25V). If the regulator dropout voltage is at the upper extreme of its specification (1.5V at maximum current and temperature for LT1083 family) it would still be able to supply 3.25V to the memory devices when the 5V rail is at the low end of its specification (4.75V). This is well within the allowable digital supply voltage range of 3.3V ± 10% (3.0V-3.6V).

LT1083 family behavior in dropout is benign. Once the device enters dropout the output simply follows the input. There is no increase in quiescent current during dropout as is common in PNP type regulators. The basic regulator circuit shown in Figure 1A supplies currents up to 7.5A. The device has all the normal protection features associated wth high current supplies, such as thermal and short circuit protection.

At currents greater than 7.5A several LT1087's are used in parallel (Figure 2). The LT1087 is the newest member of the LT1083 family. The device is a version of the LT1084 with two additional sense pins and is available in a 5-pin TO-220 package. When tied together the sense pins are used to Kelvin sense the output voltage. When used separately they form the inputs to a differential amplifier whose output changes the devices 1.2V reference voltage.

In Figure 2 the master LT1087's sense pins are tied together and connected to point A. This device senses and controls the output voltage using the Kelvin sense feature. R3 and C1 filter the voltage fed back to the sense pins. At low frequencies the output pin voltage of the master LT1087 is forced positive by the internal loop to maintain point A at the desired 3.3V value. This voltage is set by the ratio of R2/R1 according to the formula in Figure 2. The voltage across R_M is proportional to the load current.



FOR PARALLELING MORE THAN TWO DEVICES — DUPLICATE SLAVE SECTION.

MINIMUM LOAD CURRENT = (10mA) (# OF DEVICES IN PARALLEL)
R1, R2 NETWORK CAN BE USED AS THE MINIMUM LOAD

$R_M = 8m\Omega \approx 10''$ OF #20 A.W.G. SOLID WIRE (COPPER)
$R_S = 7.3m\Omega \approx 9.1''$ OF #20 A.W.G. SOLID WIRE (COPPER)

$$V_{OUT} = 1.25\left(1 + \frac{R2}{R1}\right)$$

Figure 2. High Current 5V-3.3V Regulator

The slave unit operates differently. This device senses the voltage across R_M and adjusts the voltage across R_S to be equal, effectively forcing this device to output a current equal to the master unit. The differential gain from the sense pins to the output is low (11), so to make the devices share current equally, R_M and R_S need to be scaled $R_M/R_S = 1.0/0.9$. R4 and C2 filter the feedback to the slave unit. The minimum load current for the total circuit is 10mA per device. R1 and R2 can be scaled to guarantee that the minimum load current spec will be met, and minimizes the output voltage error due to the adjust pin currents (50µA per device). The 10µF output capacitor is the minimum value needed to ensure stability. Larger output capacitors will improve transient response. R_M and R_S are chosen so that the voltage drop across them, at full load current (5A per device) is 40mV. This value is chosen to be large enough to ensure proper current sharing without significantly degrading dropout voltage. As noted in Figure 2, R_M and R_S will be in the 7mΩ-8mΩ range. These values are small enough to be made from either short lengths of wire or from carefully laid out PC traces. The absolute value of these resistors is not critical, but the ratio of R_M:R_S should be maintained.

The circuit as shown will source 10A. This capability can be increased, in increments of 5A, by duplicating the slave unit and properly sizing R1 and R2 to sink the additional 10mA per device. $C_{OUT'S}$ value may require adjustment upwards to maintain optimum transient response.

Circuits using up to five units have been tested, but there is no limit to the number of slave units, other than limits on space. These regulators offer a simple solution to powering 3.3V digital devices with almost no efficiency compromise. Low cost, space savings, and easy design make them attractive for this application.

For literature on Regulator Products, call **(800) 637-5545**.
For applications help, call (408) 432-1900, Ext. 445.

DESIGN NOTES

Number 34 in a series from Linear Technology Corporation *May, 1990*

Active Termination for SCSI-2 Bus

Sean Gold

Overview of SCSI-2

The SCSI-2 bus[1] is an interface for computers and instrumentation that communicate over small distances — often within the same cabinet. Like GPIB (IEEE 488), SCSI's hardware and software specifications are designed to coordinate independent resources such as disk and tape drives, file servers, printers, and other computers. SCSI-2 is a bidirectional bus, which must be terminated at both ends to 2.85V (Figure 1). The terminators are needed because SCSI-2 uses simple open collector output drivers in its transceivers. Terminators link communicating devices to the supplies, and roughly match the transmission line's characteristic impedance. When the load to the bus increases, the role of the termination network becomes more important for maintaining signal integrity at high data rates. An active termination design is now a part of the SCSI-2 standard and is presented here in-depth.

The single ended SCSI-2 bus is limited to six meters in length, and supports variable speed communication up to 5M transfers/sec. The bus nominally uses 18 data lines which defines the loading requirements for the terminators, because each output driver can sink at most 48mA. Up to eight SCSI devices can access the bus at regular distances along the cable. Any two devices can terminate the cable, but bit error rates are minimized with the terminators attached only at the ends. Local capacitive loading is low under these conditions, making the transmission line more consistent with fewer discontinuities.

SCSI-2's key specifications are repeated from the ANSI standard in Table 1.

Table 1. Single Ended SCSI-2

PARAMETER	VALUE	COMMENTS
Termination Supply	4.25 < TERMPWR < 5.25	0.9A Typical 1.5A Worst Case
Logic Supply	$V_{OUT} = 2.85V@0.5A$ $2.6 < V_{OUT} < 2.9$	Per Terminator
Data Rate	5M Transfers/Sec.	Six Meters Max.
Cable Impedance	110Ω $80 < Z_0 < 140$	Nominal
Transceivers	TTL Compatible	Negative True Logic 5V = 0, 0V = 1
Signal Levels	$0 < V_{OL} < 0.5$ $2.5 < V_{OH} < 5.25$ $V_{IL} < 0.8$ $2.0 < V_{IH}$ 0.2 < Hysteresis	 $-0.4mA < I_{IL} < 0mA$ $0.0mA < I_{IH} < 0.1mA$
Short Circuit Current	48mA/Transceiver	Based on Old TTL Spec

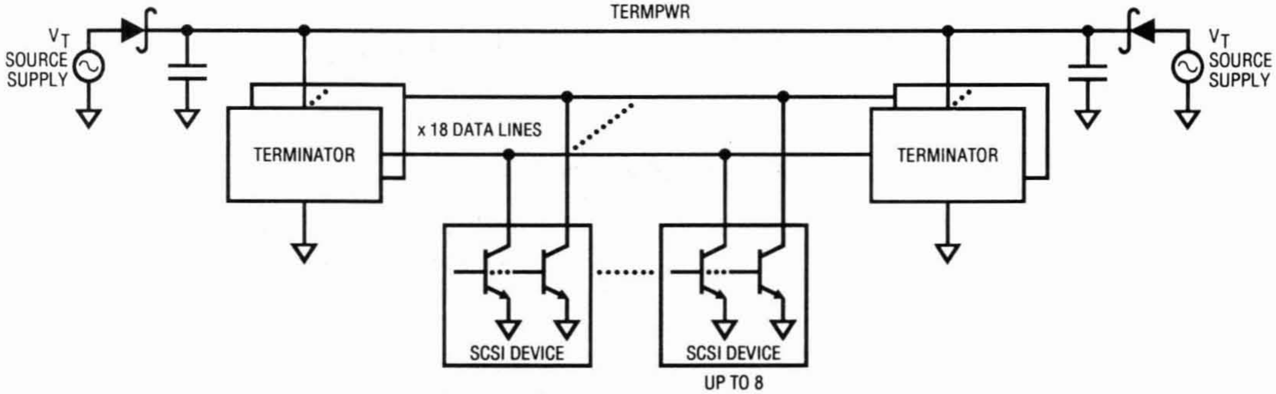


Figure 1. Global View of the SCSI-2 Bus

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[1] **Note 1:** SCSI-2 = Small Computer System Interface Version 2, pronounced "Scuzy-2." The complete specifications standard is available through ANSI #X3T9.2.

Shortcomings of Passive Terminators

The resistive voltage divider shown in Figure 2 is commonly used to terminate the SCSI bus. Multiple power sources are allowed to connect to the SCSI cable. Each source is protected with a Schottky diode to prevent damage from reverse currents. The resulting termination power signal, TERMPWR, is not well regulated — subject to variations in source supplies and protection diodes, as well as ohmic losses. Unfortunately, these changes in TERMPWR translate directly to the bus through the resistive divider, which degrades noise margins.

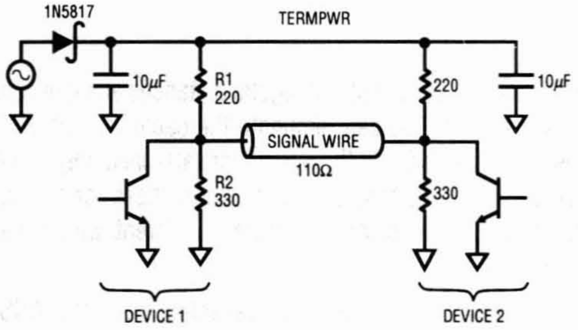


Figure 2. Passive Termination

The low values for R1 and R2 reflect a compromise between driver sink current and impedance matching the signal lines. Normally, high resistances would be desirable to minimize driver sink current. Yet, the terminator should match the signal line's 110Ω characteristic impedance, and the bus's quiescent state must be above the TTL logic threshold. It is not possible to meet all of these objectives simultaneously. The SCSI standard suggests R1 = 220Ω and R3 = 330Ω. The resulting bus voltage is 3V with 132Ω impedance, which is mismatched to the nominal 110Ω cable impedance. The Schottky diode aggravates the mismatch because it presents a poor AC ground. In addition to these problems, the small resistors draw 300mA Q-current fromTERMPWR, assuming 18 signal lines with the bus inactive.

Active Terminators

The active terminator shown in Figure 3 uses an LT1117-2.85 low dropout regulator to control the logic supply. The LT1117's line regulation makes the output immune to variations in TERMPWR. After accounting for resistor tolerances and variations in the LT1117's reference, the absolute variation in the 2.85V output is only 4 percent over temperature. When the regulator drops out at TERMPWR –2.85V = 1.25V, the output linearly tracks the input with a slope of 1V/V. Signal quality is quite good because the 110Ω series resistor closely matches the transmission line's characteristic impedance, and the regulator provides a good AC ground.

In contrast to the passive circuit, two LT1117s require only 20mA quiescent current. For the power levels in this application, the LT1117 does not need a heat sink, and is available in low cost, space saving, SOT-223 surface mount packages. Beyond solving basic signal conditioning problems, the LT1117 handles fault conditions with short circuit current limiting, thermal shutdown, and on-chip ESD protection circuitry.

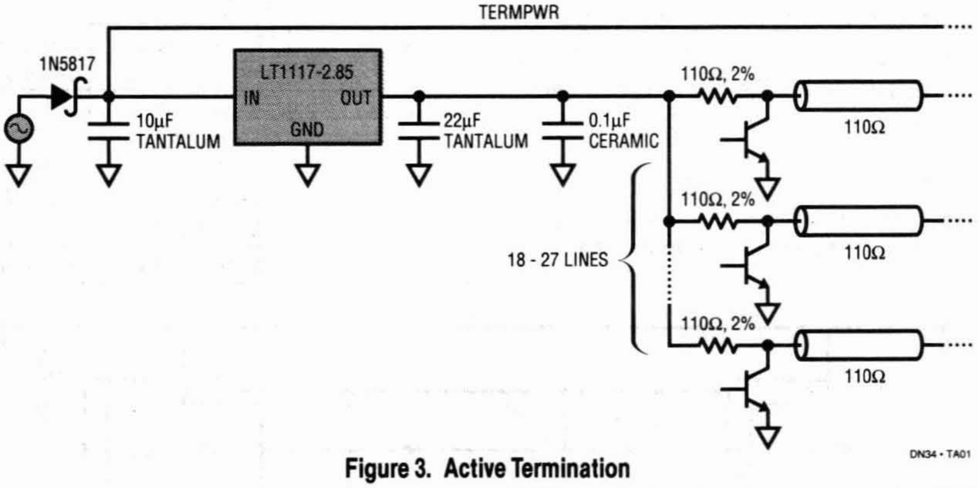


Figure 3. Active Termination

For literature on linear regulators, call **(800) 637-5545.**
For applications help, call (408) 432-1900, Ext. 209.

LINEAR TECHNOLOGY DESIGN NOTES

Number 35 in a series from Linear Technology Corporation *June, 1990*

12-Bit 8-Channel Data Acquisition System Interfaces to IBM PC Serial Port

Guy Hoover and William Rempfer

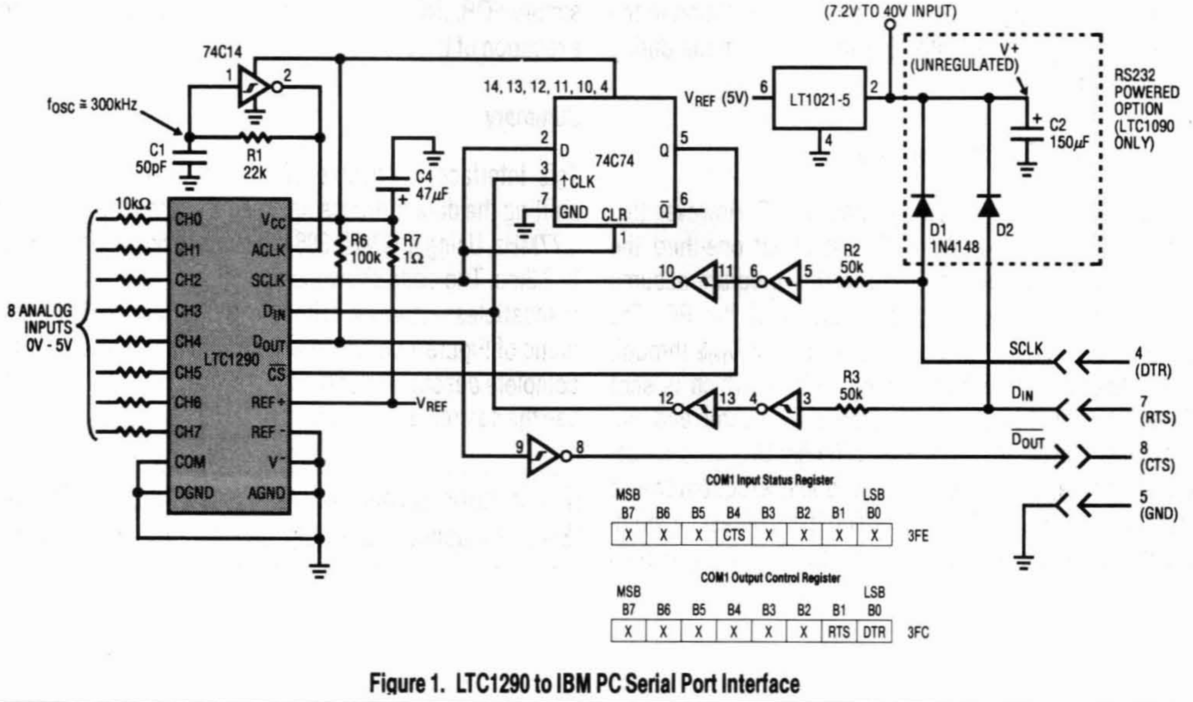
IBM PCs Collect Analog Data

IBM PC compatibles can be found just about everywhere. In those instances where a PC is not already in place, battery operated portables are readily available. This makes the PC a good choice for controlling a data acquisition system. Typically, such data acquisition systems have been expensive. Using dedicated A/D cards or IEEE-488 controllers and instruments, these systems tie up slots in the PC and are not readily transportable from one machine to another. As an alternative, the schematic of Figure 1 shows a 12-bit, 8-channel data acquisition system that connects to the serial port of the PC. This system uses an LTC1290, a reference, a handful of other low cost components and requires 12 lines of BASIC to transfer data into the PC. If only ten bits of resolution are required the LTC1290 can be replaced with an LTC1090. Additionally, if the LTC1090 is used, the system can be powered directly from the PC serial port with the option shown.

Two Glue Chips Provide the Interface

The control and status lines of the PC serial port are used to send data to and receive data from the LTC1290. Due to incompatible data formats the Rx and Tx lines are not used. The LTC1290 is a 12-bit, 8-channel data acquisition system on a chip. ACLK of the LTC1290 controls the A/D conversion rate while SCLK controls D_{IN} and D_{OUT} data rates. While $\overline{CS}$ is low D_{IN} is clocked into the LTC1290 and D_{OUT} is clocked out in a synchronous full duplex format. While $\overline{CS}$ is high the conversion requested by the last D_{IN} word is performed.

A simple RC oscillator is used to generate ACLK. The DTR pin of the PC serial port is used to form SCLK. The DTR signal is also fed into the CLR and D inputs of a 74C74 so that on the first falling SCLK the Q output of the 74C74 drives the $\overline{CS}$ of the LTC1290 low. Between data transfers DTR is held high to charge C2 which provides the unregulated V^+ if the RS232


74C14
1
2
$f_{OSC} \cong 300kHz$
C1
50pF
R1
22k
10kΩ
8 ANALOG INPUTS 0V - 5V
CH0
CH1
CH2
CH3
CH4
CH5
CH6
CH7
COM
DGND
LTC1290
V_{CC}
ACLK
SCLK
D_{IN}
D_{OUT}
$\overline{CS}$
REF+
REF–
V^-
AGND
V_{REF}
R6
100k
R7
1Ω
C4
47µF
14, 13, 12, 11, 10, 4
2
D
3
↑CLK
7
GND
CLR
74C74
Q
$\overline{Q}$
5
6
1
V_{REF} (5V)
6
LT1021-5
2
4
(7.2V TO 40V INPUT)
V+ (UNREGULATED)
C2
150µF
RS232 POWERED OPTION (LTC1090 ONLY)
D1
1N4148
D2
R2
50k
10
11
6
5
R3
50k
12
13
4
3
9
8
SCLK
D_{IN}
$\overline{D_{OUT}}$
4 (DTR)
7 (RTS)
8 (CTS)
5 (GND)

COM1 Input Status Register

MSB B7	B6	B5	B4	B3	B2	B1	LSB B0	
X	X	X	CTS	X	X	X	X	3FE

COM1 Output Control Register

MSB B7	B6	B5	B4	B3	B2	B1	LSB B0	
X	X	X	X	X	X	RTS	DTR	3FC

Figure 1. LTC1290 to IBM PC Serial Port Interface

```
10   '        LTC1290 TO RS232 IBM PC TRANSFER PROGRAM
20   '                     BY GUY HOOVER
30   '              LINEAR TECHNOLOGY CORP
40   '                        1/4/90
50   '  &H3FC IS THE ADDRESS IN HEX OF THE RS232 OUTPUT CONTROL REGISTER
60   '  &H3FE IS THE ADDRESS IN HEX OF THE RS232 INPUT STATUS REGISTER
66   '   "111101110001"  CH0 \
67   '   "111101110011"  CH1  \
68   '   "111101111001"  CH2   \
69   '   "111101111011"  CH3    \ DIN WORDS FOR CH0-CH7 SINGLE ENDED
70   '   "111101110101"  CH4    / UNIPOLAR, MSB FIRST AND 12 BITS
71   '   "111101110111"  CH5   /
72   '   "111101111101"  CH6  /
73   '   "111101111111"  CH7 /
74  DIN$="111101111111"        'DIN$ IS SENT LSB FIRST.
75                             'THE MSB MUST BE A 1 SO THAT DIN IS NORMALLY HIGH
80                             'THIS  DIN  WORD  CONFIGURES  THE LTC1290 FOR CH7
90                             'WITH RESPECT TO COM, UNIPOLAR, MSB FIRST AND
100                            '12 BITS
110  B=2048                    'B IS SCALE FACTOR FOR DOUT. B=512 FOR LTC1090
120 VOUT=0                     'VOUT IS DECIMAL REPRESENTATION OF LTC1290 DOUT
140 FOR I=1 TO 12              'LOOP TWELVE TIMES
145  OUT &H3FC,(&HFE AND INP(&H3FC))                  ' SCLK AND CS GO LOW
150                                                   ' DIN IS SHIFTED OUT
160  IF MID$(DIN$,13-I,1) ="0" THEN OUT &H3FC,(&HFD AND INP(&H3FC)) ELSE
     OUT &H3FC,(&H2 OR INP(&H3FC))
180  OUT &H3FC,(&H1 OR INP(&H3FC))                    ' SCLK GOES HIGH
210  IF (INP(&H3FE) AND 16) = 16 THEN D=0 ELSE D=1'   READ DOUT
220  VOUT=VOUT+(D*B):B=B/2                            ' SCALE EACH BIT AND SUM BITS
250 NEXT I                                            ' GO THROUGH LOOP AGAIN
260 OUT &H3FC,(&HFD AND INP(&H3FC))                   ' DIN GOES LOW
270 OUT &H3FC,(&H2 OR INP(&H3FC))                     ' DIN AND CS GO HIGH
287  'FOR J=1 TO 20: NEXT J                           ' MAKE CS HIGH FOR 52 ACLKS
```

Figure 2. Turbo BASIC Code for LTC1290 to IBM PC Serial Port Interface

powered option is used. V^+ is fed into the LT1021 reference which provides a regulated +5V for the LTC1290 and the 74C devices. The RTS pin drives the D_{IN} input of the LTC1290 and the CLK input of the 74C74. During a data transfer, RTS (D_{IN}) changes state only when DTR (SCLK) is low so the 74C74 output ($\overline{CS}$) stays low. After the transfer is completed, RTS is toggled while DTR is high causing the Q output ($\overline{CS}$ of the LTC1290) to go high. D_{OUT} of the LTC1290 goes through an inverter which drives the CTS input of the serial interface. The pull-up resistor on D_{OUT} prevents power consumption in the inverter when D_{OUT} goes into high impedance mode during the conversion.

A Few Lines of BASIC Read the Data

The code of Figure 2 is written in Turbo BASIC. However, this program will run using GW BASIC at about one-third the transfer rate. The addresses used in this program assume that the interface is connected to COM1 of the PC. The LTC1290 is configured by sending the variable D_{IN}\$ through the RTS line. D_{IN}\$ is a 12-bit string variable which is sent serially LSB first. Bits 11, 10, 9 and 8 are don't cares and bits zero through seven are the actual LTC1290 D_{IN} word as defined in the data sheet. The following loop is executed twelve times. SCLK and $\overline{CS}$ are forced low. D_{IN} is set or reset according to the desired word. SCLK is then set high. D_{OUT} is read one bit at a time and multiplied by a weighting variable B, to produce a variable that ranges from 0 to 4095 (0 to 1023 for the LTC1090). The variable B is initialized to 2048 (512 for the LTC1090) and divided by two after each bit. The last time through the loop SCLK is high and D_{IN} is cycled low then high. This causes $\overline{CS}$ to return high at which time the requested conversion is performed. $\overline{CS}$ must remain high for 52 ACLK cycles, typically 175μs with the RC oscillator shown. This is not a problem except for the fastest of PCs where a simple FOR...NEXT loop as in line 287 can be used to delay execution of the program until the conversion is complete.

Summary

This interface is capable of performing a conversion and shifting the data in 185ms using an XT compatible running at 4.77MHz. Using a 16MHz 386 the same task can be completed in 2.3ms. The code shown is specifically for the IBM PC and compatibles. However, with the proper software the schematic of Figure 1 should interface with any RS232 port. For a complete description of the LTC1290 and the LTC1090 please see the desired data sheet.

For literature on our Data Acquisition line, call **(800) 637-5545.** For applications help, call (408) 432-1900, Ext. 453.

DESIGN NOTES

Number 36 in a series from Linear Technology Corporation *July, 1990*

Ultra Low Noise Op Amp Combines Chopper and Bipolar Op Amps

Nello Sevastopoulos

Chopper op amp technology has continuously improved. Contemporary single, dual, and quad low noise chopper op amps (LTC1050/51/53), with internal sample and hold capacitors, are compatible with industry standard op amp sockets.

Chopper op amps are mainly used to amplify small DC signals and these applications require excellent V_{OS}, V_{OS} drift, low bias current and low noise. The outstanding V_{OS} performance of chopper op amps is well known. However, their low frequency noise compared to precision bipolar op amps is at least an order of magnitude higher. For applications which require both ultra low V_{OS} drift and ultra low noise, neither bipolar nor chopper op amps are optimum. A circuit combining the superior DC performance of the dual chopper LTC1051 with the ultra low noise voltage of the LT1007 precision bipolar op amp appears in Figure 1. This composite op amp can, for instance, be used as a strain gauge amplifier. One half of the LTC1051 dual chopper op amp, LTC1051, integrates the small LT1007 input offset voltage and applies a DC correction voltage at its pin-8 via divider (R2, R3). The other half of the LTC1051, buffers the V_{OS} nulling circuitry eliminating loading at input A. Resistors R1, R2, R3 allow the integrator full output swing assuring V_{OS} correction of the LT1007. The ratio of R3 to R2 is made as high as possible to limit noise injection of the chopper into pin-8 of the bipolar op amp. The total measured input V_{OS} was 2µV, with a 10nV/°C drift.

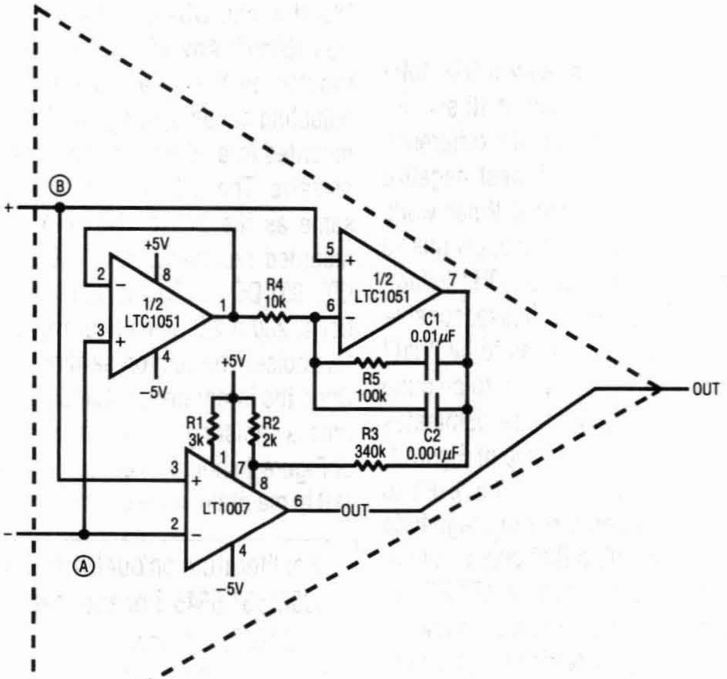


Figure 1. Combining the Low V_{OS} and V_{OS} Drift of the Dual Chopper LTC1051 with the Low Noise of a Precision LT1007 Bipolar Op Amp

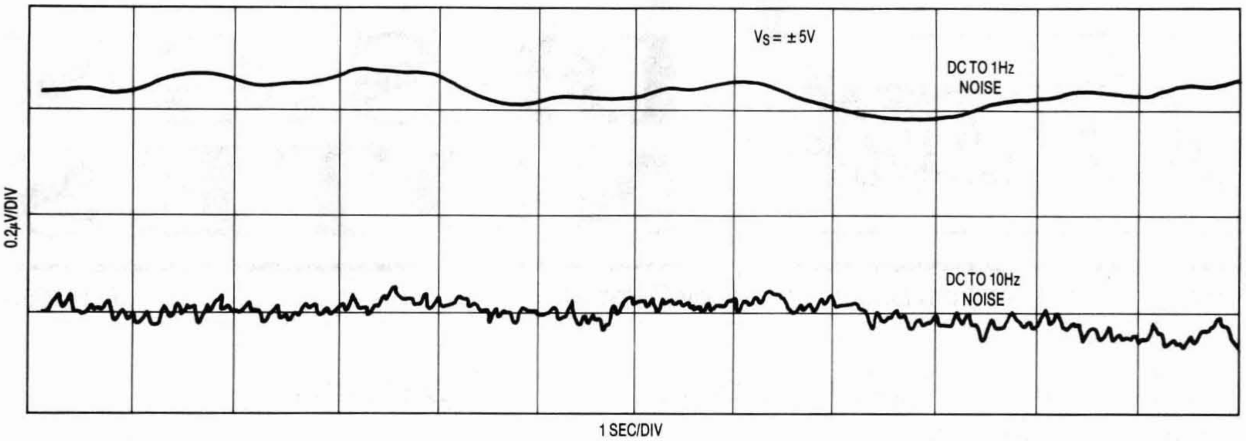


Figure 2. Recorded Peak-to-Peak Noise of the Composite Op Amp, Figure 1, During a 10 Sec. Window

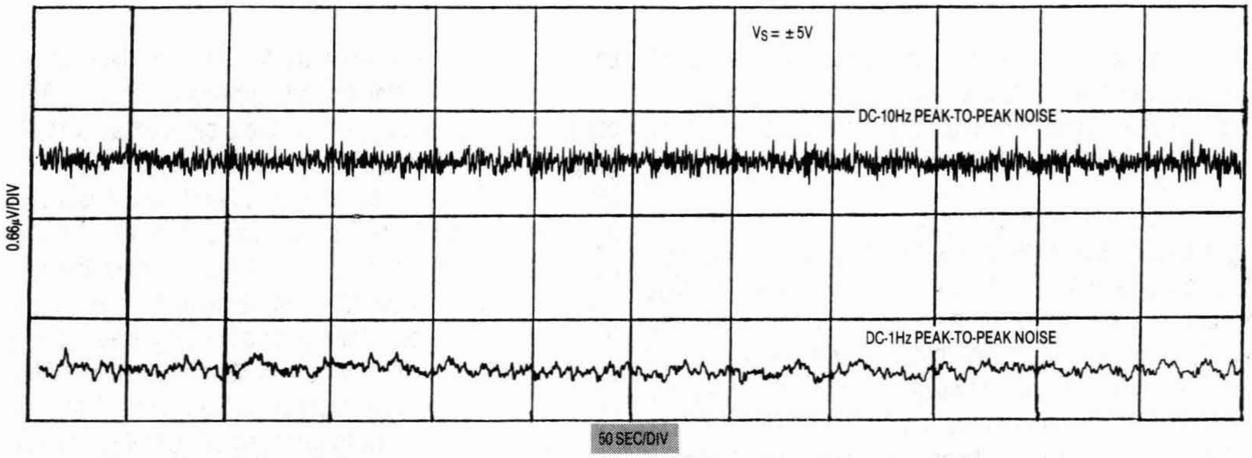


Figure 3. Recorded Peak-to-Peak Noise of the Composite Op Amp, Figure 1, During a 10 Minute Window

Noise Measurements

Bipolar op amp datasheets commonly specify 0.1Hz–10Hz peak-to-peak noise measured during a period of 10 sec. (or "10 sec. window"). The peak-to-peak noise is the difference of the highest positive noise spike to the lowest negative noise spike occurring during the 10 sec. interval. When working with chopper op amps, it is very tempting to apply this 10 sec. window test for noise measured from DC to 10Hz. In fact, the LTC1051 zeros its V_{OS} at a 2.5kHz rate, so it is reasonable to assume its noise spectral density continues to be "flat" below 0.1Hz. Experiments prove this assumption to be quite valid since the 0.1Hz to 10Hz peak-to-peak noise dominates the DC to 0.1Hz noise. For the composite op amp of Figure 1, however, the assumption may not be correct. The 0.1Hz to 10Hz noise of the LT1007 is at least an order of magnitude lower than the LTC1051 noise. Assuming that only a minute portion of the LTC1051 noise is injected into the LT1007 offset pin, then most 10 sec. windows should show outstanding noise results. Figure 2 shows this is so. Notice that for both DC-1Hz, and DC–10Hz bandwidths the peak-to-peak noise was 100nV!! Any additional noise, therefore, should be contributed by the ultra low frequency "hunting" of the V_{OS} adjusting circuit's, integrator loop. Figure 3 shows the noise recorded in a 10 minute period. Again, results are quite impressive. The DC to 10Hz peak-to-peak noise is about the same as the DC to 1Hz peak-to-peak noise. The 0.2μVp-p recorded represents a 7 to 9 times improvement over the LTC1051 DC to 10Hz noise measured under the same conditions, and a 2.5 times improvement of the equivalent DC to 1Hz noise. The turn-on settling time of the circuit is 16 sec. Once the integrator captures the V_{OS}, the circuit's response time is undistinguishable from a normal amplifier. The circuit of Figure 1 should be used with source resistances less than 1kΩ to maintain noise performance.

For literature on our Ultra Low Noise Op Amps, call **(800) 637-5545**. For applications help, call (408) 432-1900, Ext. 456.

DESIGN NOTES

Number 37 in a series from Linear Technology Corporation *Summer, 1990*

High Dynamic Range Bandpass Filters for Communications

Richard Markell

Introduction

Octave or decade wide bandpass filters are non-trivial to design. Wide bandpass filtering requires the designer use a highpass filter at the input in series with a lowpass filter to achieve the desired specifications. This becomes evident if one examines the transfer functions of the state-variable-filter configuration, be it switched capacitor or active RC. Either option limits severely the achievable dynamic range if a wideband bandpass filter is designed using the bandpass output.

Wideband bandpass filters occupy a niche in the communications arena of signal processing. The wideband bandpass function is required in receiver IF applications which traditionally use the crystal filter and/or active RC's. Sonar applications also demand steep, wide, low noise bandpass filters to allow analysis of "chunks" of the frequency spectrum, one at a time or in parallel.

Recent improvements in switched capacitor filter technology allow designers the luxury of using switched capacitor filters in these applications. True clock tuning allows variable bandwidth filters to be implemented with only a few parts.

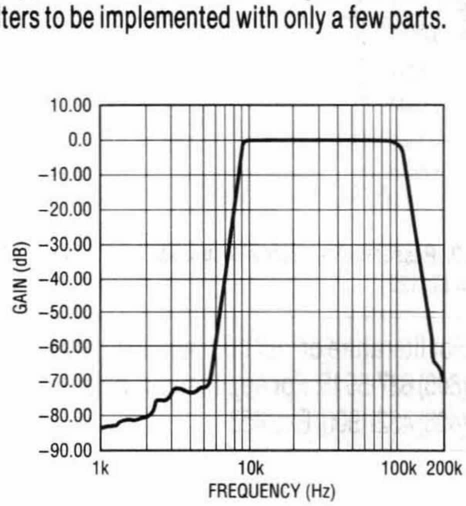


Figure 1. Frequency Response. $V_{IN} = 2.2V_{RMS}$, Output Buffer = LT1122.

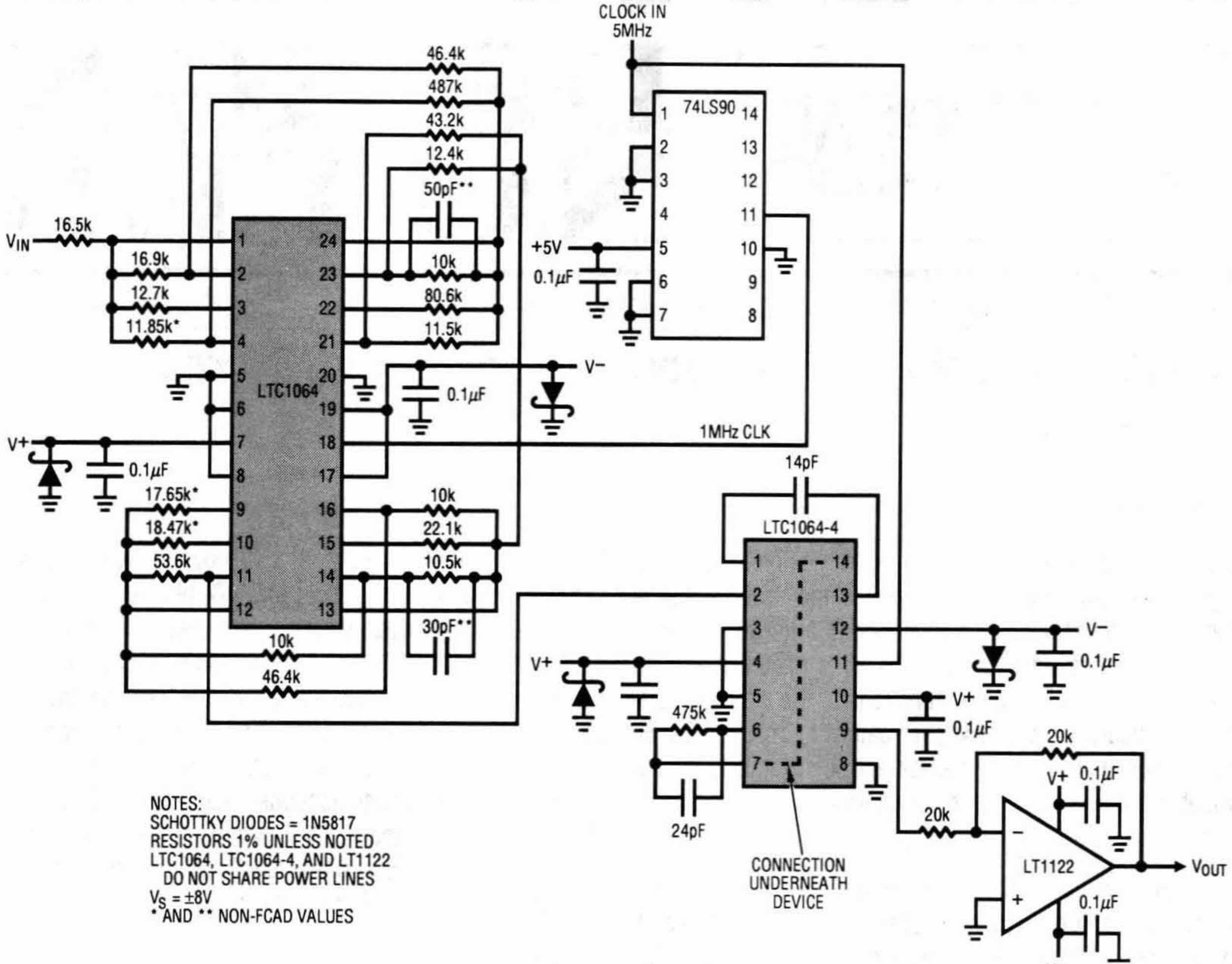
This note details the design of a wideband (10kHz–100kHz) bandpass filter using a single LTC1064 plus an LTC1064-4. The LTC1064 is a quad universal switched capacitor filter while the LTC1064-4 is the same silicon with integrated resistors configured to implement an 8th order elliptic lowpass filter. Both filters have low noise and can operate to frequencies beyond 100kHz. The combination bandpass filter has a set of tough design specifications: total integrated noise in the passband less than 350μV, passband ripple less than 0.4dB or ±0.2dB, and steep rolloffs at the band edges (−70dB at 5kHz, and −70dB at 200kHz).

Design

The design ideology combined an LTC1064-4 elliptic lowpass filter with a highpass LTC1064 designed using Linear Technology's FilterCAD filter design software. The LTC1064-4 provides an attenuation of greater than 70dB at 2 times cutoff, while the highpass filter was designed to be almost the mirror image of the lowpass filter. Figure 2 shows the schematic of the composite bandpass filter. Note the 74LS90 is used as a divide by 5 whose output clocks the LTC1064 used as the 10kHz highpass filter. In addition to providing both 5MHz and 1MHz clocks, this circuit allows the clocks to be synchronous. This is essential for well behaved operation of the sampled data filters.

Test Results

Figure 1 shows the overall frequency response of the bandpass filter. Note the steep slopes at the transition regions of the filter. The measured noise in the passband of the filter was 320μV_{RMS}. Passband ripple is shown in Figure 3. Figure 3 shows excellent ripple specifications of less than ±0.2dB. It should be noted that the values of the resistors marked with an asterisk were modified slightly from the values given by FilterCAD. Otherwise the passband ripple measured better than ±0.4dB. Additional note should be made of the 50pF


CLOCK IN
5MHz
46.4k
487k
43.2k
12.4k
50pF**
V_IN
16.5k
16.9k
12.7k
11.85k*
LTC1064
10k
80.6k
11.5k
0.1µF
V−
+5V
0.1µF
74LS90
1MHz CLK
V+
0.1µF
17.65k*
18.47k*
53.6k
10k
22.1k
10.5k
30pF**
10k
46.4k
14pF
LTC1064-4
V+
475k
24pF
V−
0.1µF
V+
0.1µF
20k
V+ 0.1µF
20k
LT1122
V_OUT
0.1µF
V−
CONNECTION
UNDERNEATH
DEVICE

NOTES:
SCHOTTKY DIODES = 1N5817
RESISTORS 1% UNLESS NOTED
LTC1064, LTC1064-4, AND LT1122
DO NOT SHARE POWER LINES
$V_S = \pm 8V$
* AND ** NON-FCAD VALUES

Figure 2. Schematic Diagram 10kHz-100kHz Bandpass Filter

and 30pF capacitors shown with double asterisks. These capacitors serve as RC filters on two of the highpass outputs of the LTC1064 to rolloff the response of the HPF (well past the passband of the overall filter) to limit noise aliasing back to the filter's passband. Note that these capacitors may limit the overall tunability of the filter or they may need a range changing switch.

Conclusions

A 16th order low noise high quality bandpass filter can be designed with only four active components and a handful of resistors. The filter meets specifications that can only be approached with the most sophisticated hybrid filter solutions. Further, the filter was primarily designed with the FilterCAD program, so that the designer may change parameters with the push of the "Enter" key. The filter is another in the amazing set of achievements available to the system designer by using the new switched capacitor filters from Linear Technology.

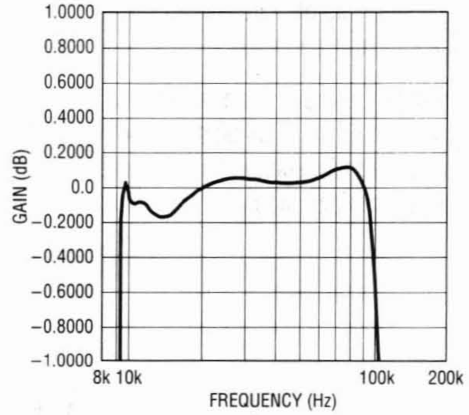


Figure 3. Passband Frequency Response. $V_{IN} = 2.2V_{RMS}$, Output Buffer = LT1122.

For literature on our complete filter line, call **(800) 637-5545**. For applications help, call (408) 432-1900, Ext. 453.

DESIGN NOTES

Number 38 in a series from Linear Technology Corporation *August, 1990*

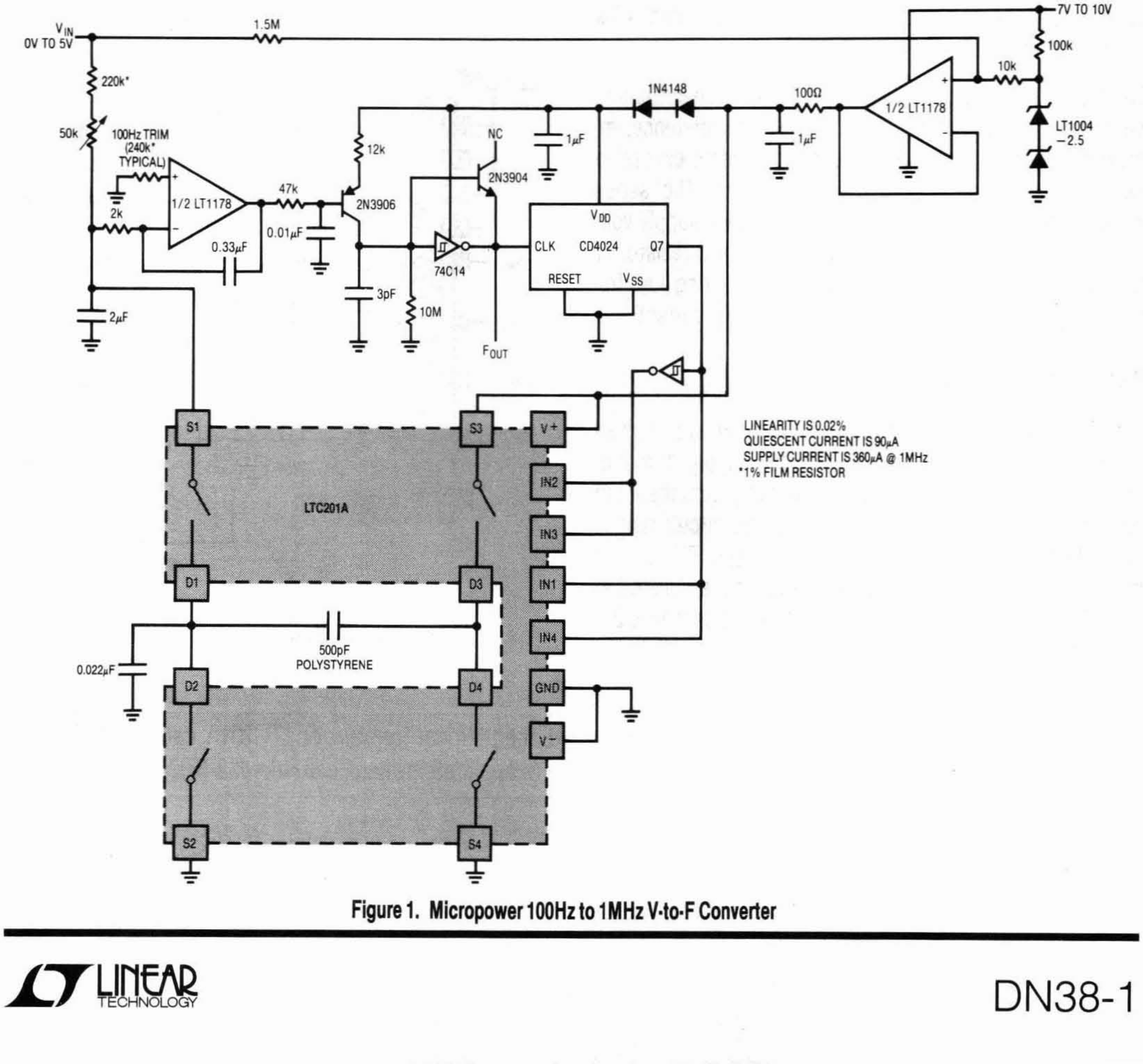
Applications for a New Micropower, Low Charge Injection Analog Switch

Guy Hoover, William Rempfer, Jim Williams

With greater accuracy for both charge and voltage switching, the LTC201A is a superior replacement for the industry standard DG201A. In addition, the micropower LTC201A operates from a single 5V supply, and has lower on-resistance and faster switching speed. These improvements are critical to the operation of the following three circuits.

Micropower V-F Converter

Figure 1 shows a 100Hz to 1MHz voltage-to-frequency converter. This V-to-F operates from a single supply and draws only 90μA quiescent current, rising to 360μA at 1MHz. Linearity is 0.02% over a 100Hz to 1MHz range.


V_IN
0V TO 5V
1.5M
220k*
50k
100Hz TRIM (240k* TYPICAL)
2k
1/2 LT1178
0.33µF
2µF
47k
0.01µF
12k
2N3906
3pF
10M
NC
2N3904
74C14
F_OUT
1µF
1N4148
V_DD
CLK
CD4024
Q7
RESET
V_SS
100Ω
1µF
1/2 LT1178
10k
100k
7V TO 10V
LT1004
−2.5
S1
S3
V+
IN2
IN3
IN1
IN4
GND
V−
LTC201A
D1
D3
D2
D4
S2
S4
500pF POLYSTYRENE
0.022µF

LINEARITY IS 0.02%
QUIESCENT CURRENT IS 90µA
SUPPLY CURRENT IS 360µA @ 1MHz
*1% FILM RESISTOR

Figure 1. Micropower 100Hz to 1MHz V-to-F Converter

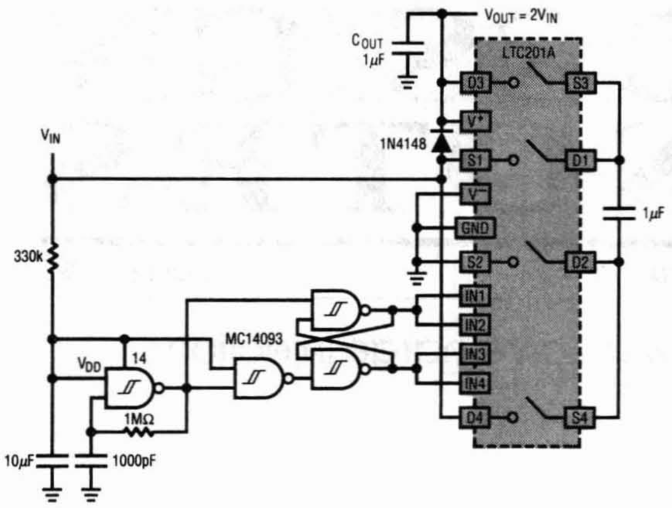


Figure 2. Micropower, 4.5V-15V Input, Voltage Doubler

The circuit consists of an oscillator, a servo amplifier and a charge pump. The oscillator's divided down output is expressed as current (charge per time) by the LTC201A-500pF combination. The input voltage is converted to current by the 220k trimmer pair. The amplifier controls the oscillator frequency to force the net value of the current into A1's summing point to zero.

The 1.5MΩ resistor between V_{IN} and the reference buffer amplifier sums a small input related voltage to the reference, improving linearity. The 0.022µF capacitor prevents excessive negative transitions at LTC201A D1-D2 pins. The series diodes in the oscillator divider supply line lower supply voltage, decreasing current consumption. The 10MΩ resistor at Q8's collector dominates node leakages ensuring low frequency operation by forcing Q8 to always source current.

Precision Voltage Doubler

The precision micropower voltage doubler of Figure 2 has an input voltage range of 4.5V to 15V. The low supply current of the LTC201A allows it to be powered directly from the input voltage. Total no load supply current of the circuit ranges from 20µA at $V_{IN} = 4.5V$ to 130µA at $V_{IN} = 15V$. Output impedance is only 1.2kΩ at $V_{IN} = 4.5V$ and reduced to 600Ω at $V_{IN} = 15V$. The accuracy of this circuit is better than 0.2% over the 4.5V to 15V input range.

The MC14093 is used to form an oscillator with complementary non-overlapping outputs. R1 and C1 determine the frequency of oscillation (roughly 1.2kHz at $V_{IN} = 4.5V$). The oscillator outputs drive two sets of switches in the LTC201A and ensure that one pair of switches shuts off before the other set turns on. C_{IN} is alternately charged to V_{IN} and then stacked on top of V_{IN} to charge C_{OUT}. R2 reduces the supply voltage to the MC14093 which keeps current drain low. The diode ensures latch-free power-up for any input rise time condition.

Quad 12-Bit Sample and Hold

Figure 3's sample and hold uses the low charge injection of the LTC201A combined with the low offset voltage of the LT1014 to produce a sample to hold offset of only 0.6mV. This makes it accurate enough for 12-bit applications. Acquisition time to 0.6mV is 20µs. Aperture time is 300ns (the off time of the LTC201A). Droop rate is 2mV/ms and is limited by the I_B of the LT1014. The input range is 3.5V to −5V with ±5V supplies.

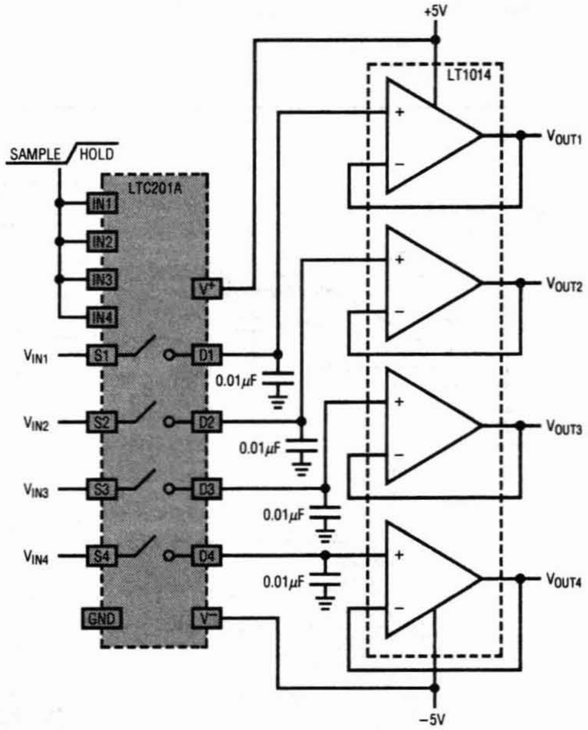


Figure 3. Quad 12-Bit Sample and Hold

For additional literature on LTC201A, call **(800) 637-5545.**
For applications help, call (408) 432-1900, Ext. 445.

DESIGN NOTES

Number 39 in a series from Linear Technology Corporation *September, 1990*

Low Power CMOS RS485 Transceiver

Robert Reay

Introduction

The EIA RS485 data transmission standard has become popular because it allows for balanced data transmission in a party line configuration. Users are able to configure inexpensive local area networks and multi-drop communication links using twisted pair wire and the protocol of their choice.

Previous RS485 transceivers have been designed using bipolar technology because the common mode range of the device must extend beyond the supplies and be immune to ESD damage and latchup. Unfortunately, the bipolar devices draw a large amount of supply current and are unacceptable for low power applications. The LTC485 is the first CMOS RS485 transceiver featuring ultra low power consumption ($I_{CC} = 500\mu A$ max.) without sacrificing ESD and latchup immunity.

Proprietary Output Stage

The LTC485 driver output stage of Figure 1 features a common mode range that extends beyond the supplies while virtually eliminating latchup and providing excellent ESD protection. Two Schottky diodes SD3 and SD4 are added to a conventional CMOS inverter output stage. The Schottky diodes are fabricated by a proprietary modification to a standard N-well CMOS process. When the output stage is operating normally, the Schottky diodes are forward biased and have a small voltage drop across them. When the output is in the high impedance state and is driven above V_{CC} or below ground by another driver on the party line, the parasitic diode D1 or D2 will forward bias, but SD3 or SD4 will reverse bias and prevent current from flowing into the N-well or substrate. Thus, the high impedance state is maintained even with the output voltage beyond the supplies. With no current flow into the N-well or substrate, latchup is virtually eliminated.

Propagation Delay

Using the test circuit of Figure 4 with only one foot of twisted pair wire, Figures 2 and 3 show the typical propagation delays.

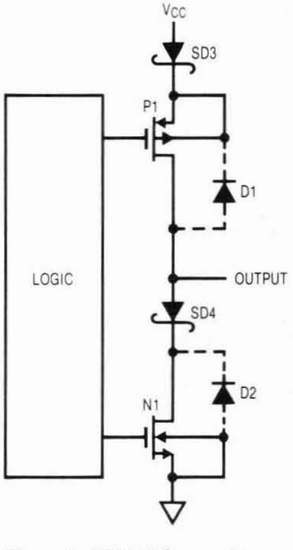


Figure 1. LTC485 Output Stage

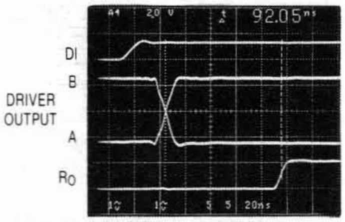


Figure 2. LTC485 System Waveforms

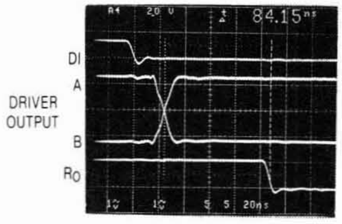


Figure 3. LTC485 System Waveforms

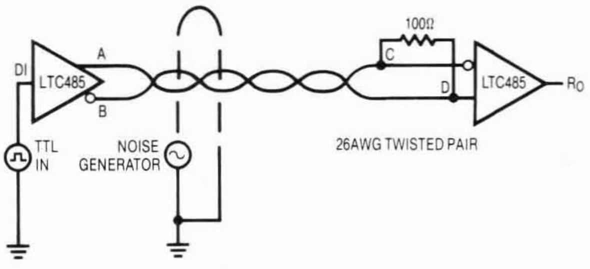


Figure 4. LTC485 System Test Circuit

LTC485 Line Length vs Data Rate

The maximum line length allowable for the RS422/RS485 standard is 4000 feet. Using the test circuit of Figure 4 with 4000 feet of twisted pair wire, Figure 5 and 6 show that with ≈20Vp-p common mode noise injected on the line, the LTC485 is able to reconstruct the data stream at the end of the wire.

Figures 7 and 8 show that the LTC485 is able to comfortably drive 4000 feet of wire at 110kHz.

When specifying line length vs maximum data rate the curve in Figure 9 should be used:

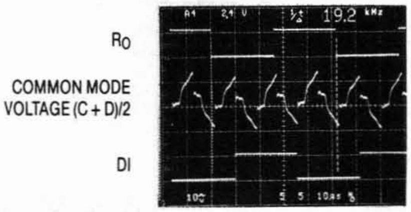

19.2 kHz
RO
COMMON MODE
VOLTAGE (C + D)/2
DI

Figure 5. System Common Mode Voltage @ 19.2kHz

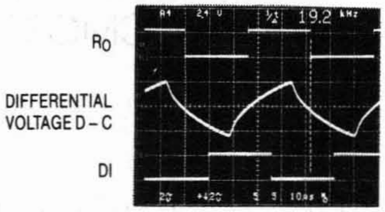

19.2 kHz
RO
DIFFERENTIAL
VOLTAGE D – C
DI

Figure 6. System Differential Voltage @ 19.2kHz

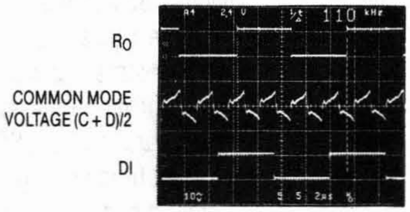

110 kHz
RO
COMMON MODE
VOLTAGE (C + D)/2
DI

Figure 7. System Common Mode Voltage @ 110kHz

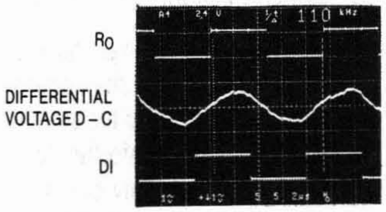

110 kHz
RO
DIFFERENTIAL
VOLTAGE D – C
DI

Figure 8. System Differential Voltage @ 110kHz

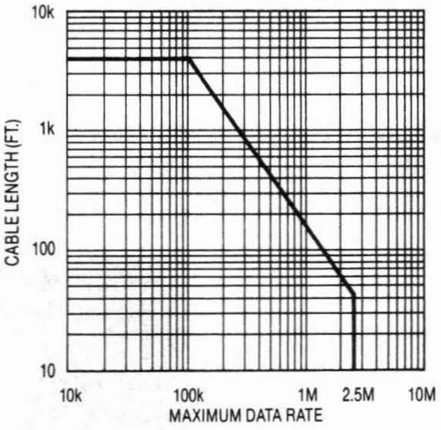


Figure 9. Cable Length vs Maximum Data Rate

For literature of our Low Power Transceivers call **(800) 637-5545.** For applications help, call (408) 432-1900, Ext. 456.

DESIGN NOTES

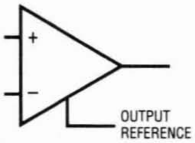
Number 40 in a series from Linear Technology Corporation *October, 1990*

Designing with a New Family of Instrumentation Amplifiers

Jim Williams

A new family of IC instrumentation amplifiers achieves performance and cost advantages over other alternatives. Conceptually, an instrumentation amplifier is simple. Figure 1 shows that the device has passive, fully differential inputs, a single ended output and internally set gain. Additionally, the output is delivered with respect to the reference pin, which is usually grounded. Maintaining high performance with these features is difficult, accounting for the cost-performance disadvantages previously associated with instrumentation amplifiers.

Figure 2 summarizes specifications for the amplifier family. The LTC1100 has the extremely low offset, drift, and bias current associated with chopper stabilization techniques. The LT1101 requires only 105μA of supply current while retaining excellent DC characteristics. The FET input LT1102 features high speed while maintaining precision. Gain error and drift are extremely low for all units, and the single supply capability of the LTC1100 and LT1101 is noteworthy.



→ NO FEEDBACK RESISTORS USED
→ GAIN FIXED INTERNALLY (TYP 10 OR 100) OR SOMETIMES RESISTOR PROGRAMMABLE
→ BALANCED, PASSIVE INPUTS
→ OUTPUT DELIVERED WITH RESPECT TO OUTPUT REFERENCE PIN

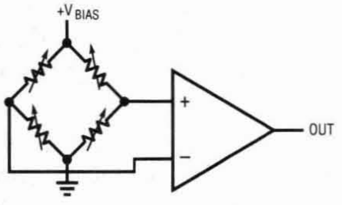
Figure 1. Conceptual Instrumentation Amplifier

PARAMETER	CHOPPER STABILIZED LTC1100	MICROPOWER LT1101	HIGH SPEED LT1102
Offset	10μV	160μV	500μV
Offset Drift	100nV/°C	2μV/°C	2.5μV/°C
Bias Current	50pA	8nA	50pA
Noise (0.1Hz-10Hz)	2μVp-p	0.9μV	2.8μV
Gain	100	10,100	10,100
Gain Error	0.03%	0.03%	0.05%
Gain Drift	4ppm/°C	4ppm/°C	5ppm/°C
Gain Non-Linearity	8ppm	8ppm	10ppm
CMRR	104dB	100dB	100dB
Power Supply	Single or Dual, 16V Max	Single or Dual, 44V Max	Dual, 44V Max
Supply Current	2.2mA	105μA	5mA
Slew Rate	1.5V/μs	0.07V/μs	25V/μs
Bandwidth	8kHz	33kHz	220kHz

Figure 2. Comparison of The New IC Instrumentation Amplifiers

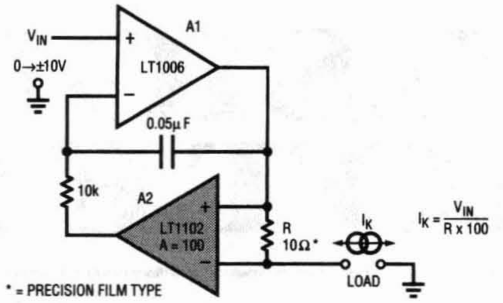
The classic application for these devices is bridge measurement. Accuracy requires low drift, high common mode rejection and gain stability. Figure 3 shows a typical arrangement with the table listing performance features for different bridge transducers and amplifiers.

Bridge measurement is not the only use for these devices. They are also useful as general purpose circuit components, in similar fashion to the ubiquitous op amp. Figure 4 shows a voltage controlled current source with load and control voltage referred to ground. This simple, powerful circuit produces output current in strict accordance with the sign and magnitude of the control voltage. The circuit's accuracy and stability are almost entirely dependent upon resistor R. A1, biased by V_{IN}, drives current through R (in this case 10Ω) and the load. A2, sensing differentially across R, closes a loop back to A1. The load current is constant because A1's loop forces a fixed voltage across R. The 10k-0.5μF combination sets rolloff, and the configuration is stable. Figure 5 shows dynamic response. Trace A is



BRIDGE TRANSDUCER	AMPLIFIER	V_{BIAS}	COMMENTS
350Ω Strain Gage (BLH #DHF – 350)	LTC1100	10V	Highest Accuracy, 30mA Supply Current
1800Ω Semiconductor (Motorola MPX2200AP)	LT1101	1.2V	Lower Accuracy & Cost. < 800μA Supply Current

Figure 3. Characteristics of Some Bridge Transducer - Amplifier Combinations


VIN
0→±10V
A1
LT1006
0.05μF
10k
A2
LT1102
A = 100
R
10Ω*
IK
IK = VIN / (R x 100)
LOAD

* = PRECISION FILM TYPE

Figure 4. Voltage Programmable Current Source is Simple and Precise

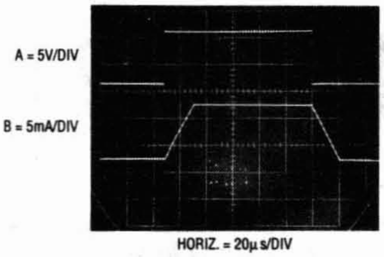
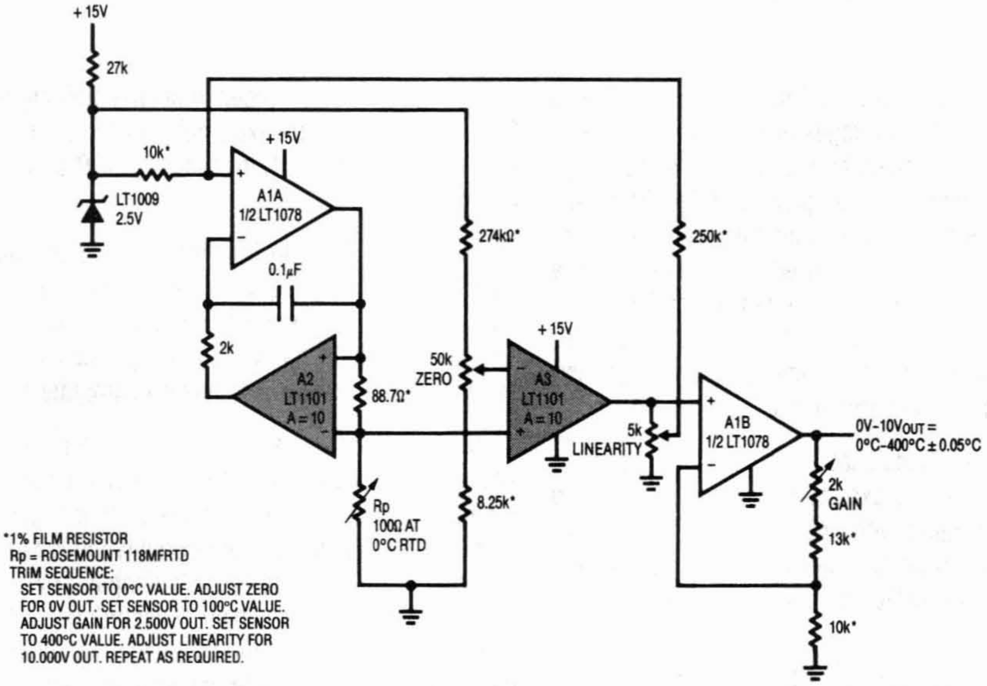


Figure 5. Dynamic Response of the Current Source


+15V
27k
10k*
LT1009
2.5V
+15V
A1A
1/2 LT1078
0.1μF
2k
A2
LT1101
A = 10
88.7Ω*
274kΩ*
50k
ZERO
+15V
A3
LT1101
A = 10
250k*
5k
LINEARITY
A1B
1/2 LT1078
0V-10VOUT = 0°C-400°C ± 0.05°C
2k
GAIN
13k*
10k*
Rp
100Ω AT
0°C RTD
8.25k*

*1% FILM RESISTOR
Rp = ROSEMOUNT 118MFRTD
TRIM SEQUENCE:
SET SENSOR TO 0°C VALUE. ADJUST ZERO FOR 0V OUT. SET SENSOR TO 100°C VALUE. ADJUST GAIN FOR 2.500V OUT. SET SENSOR TO 400°C VALUE. ADJUST LINEARITY FOR 10.000V OUT. REPEAT AS REQUIRED.

Figure 6. Linearized Platinum RTD Bridge. Feedback to Bridge from A3 Linearizes the Circuit

the voltage control input while trace B is the output current. Response is clean, with no slew residue or aberrations.

A final circuit, Figure 6, combines the current source and a platinum RTD bridge to form a complete high accuracy thermometer. A1A and A2 will be recognized as a form of Figure 4's current source. The ground referred RTD sits in a bridge composed of the current drive and the LT1009 biased resistor string. The current drive allows the voltage across the RTD to vary directly with its temperature induced resistance shift. The difference between this potential and that of the opposing bridge leg forms the bridge output. The RTD's constant current drive forces the voltage across it to vary with its resistance, which has a nearly linear positive temperature coefficient. The non-linearity could cause several degrees of error over the circuit's 0°C-400°C operating range. The bridges output is fed to instrumentation amplifier A3, which provides differential gain while simultaneously supplying non-linearity correction. The correction is implemented by feeding a portion of A3's output back to A1's input via the 10k-250k divider. This causes the current supplied to Rp to slightly shift with its operating point, compensating sensor non-linearity to within ±0.05°C. A1B, providing additional scaled gain, furnishes the circuit output. To calibrate this circuit, follow the procedure given in Figure 6.

Details of these and other instrumentation amplifier circuits may be found in LTC Application Note 43, "Bridge Circuits — Marrying Gain and Balance."

For literature on our Instrumentation Amplifiers, call **(800) 637-5545**. For applications help, call (408) 432-1900, Ext. 456

DESIGN NOTES

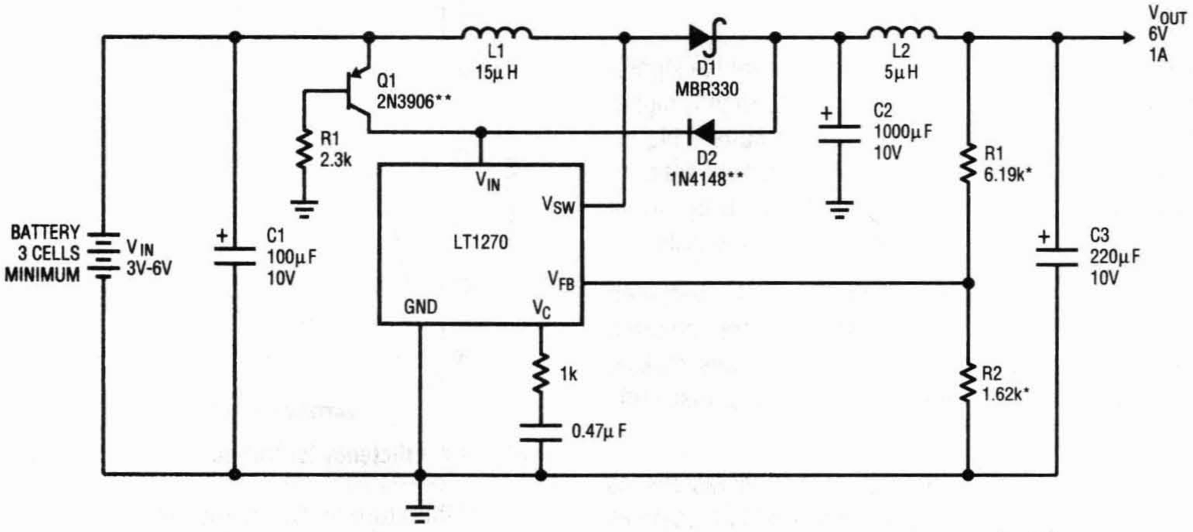
Number 41 in a series from Linear Technology Corporation *November, 1990*

Switching Regulator Allows Alkalines to Replace NiCads

Brian Huffman

In many applications it is desirable to substitute nonrechargeable batteries for chargeable types. This capability is necessary when the NiCads can't be recharged or long charge times are unacceptable. Alkaline batteries are an excellent choice in this situation. They are readily available and have reasonable energy density. Compared to Alkalines, NiCads provide a more stable terminal voltage as they discharge. NiCads decay from 1.3V to 1.0V, while Alkalines drop from 1.5V to 0.8V. Replacing NiCads with Alkalines can cause unacceptable low supply voltage, although available energy is adequate. A boost type switching regulator obviates this problem, allowing Alkaline cells to replace NiCads. The circuit shown in Figure 1 accommodates the Alkaline cells widely varying terminal voltage while providing a constant output voltage.

This circuit is a step-up boost type switching regulator. It maintains a constant 6V output as battery voltage falls. The inductor accumulates energy from the battery when the LT1270 switch pin (V_{SW}) switches to ground and dumps its stored energy to the output when the switch pin (V_{SW}) goes off. The feedback pin (V_{FB}) samples the output from the 6.19k-1.62k divider. The LT1270's error amplifier compares the feedback pin voltage to its internal 1.24V reference and controls the V_{SW} pin switching current, completing a control loop. The output voltage can be varied by changing the resistor divider ratio. The RC damper on the V_C pin provides loop frequency compensation. The minimum start up voltage for this circuit is 3V. If a 3.3V start up voltage is permissible R1 and Q1 can be removed with D2 replaced by a short.



* = 1% FILM RESISTORS
** = OPTIONAL – FOR 0.3V LOWER START UP VOLTAGE
D1 = MOTOROLA – MBR330
C1 = NICHICON – UPL1A101MRH
C2 = NICHICON – UPL1A102MRH6
C3 = NICHICON – UPL1A221MRH
L1 = COILTRONICS – CTX15-8-52
L2 = COILTRONICS – CTX5-1-FR

$$V_{OUT} = 1.24V\left(1 + \frac{R1}{R2}\right)$$

Figure 1. Low Voltage Circuit Provides Constant Output Voltage as Battery Discharges

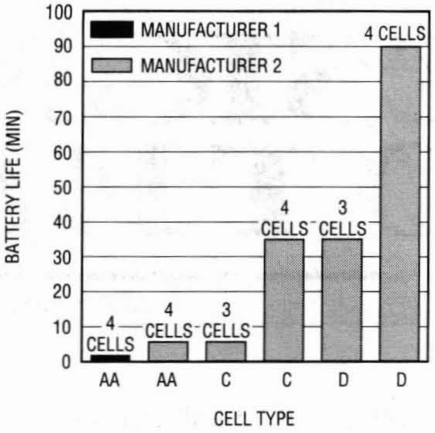


Figure 2. Battery Life Characteristics for Different Batteries for a 6W Load

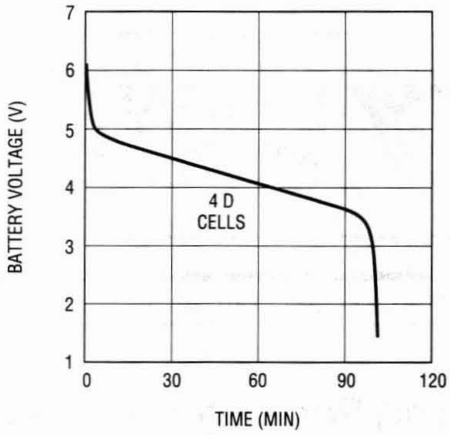


Figure 3. Alkaline Battery Discharge Characteristic with 6W Load

Bootstrapping the V_{IN} pin off the output voltage allows the battery voltage to drop below the minimum start up voltage, while maintaining circuit operation. For example, with three C cells the battery voltage is initially 4.5V and operates down to 2.4V. With this bootstrapped technique the circuit provides a constant output voltage over the battery's complete operating range, maximizing battery life.

Battery life characteristics are different for various cell types. Figure 2 compares battery life between AA, C, and D cells with a 6W load. In this application the power drain from the battery remains relatively constant. As the battery voltage decreases the battery current increases. The AA types discharge quicker than the C or D cells. They are physically smaller than the other cells, and therefore store less energy. The AA cells are 3 times smaller than the C cells and 6 times smaller than the D cells.

Current drain also influences cell life. Battery life significantly decreases at high current discharge. Slightly higher battery stack voltages permit surprising battery life increases. The higher voltage means lower current drain for a constant power load. Operating at just 33% less current the four C cells last 5 times longer than three C cells.

Battery life characteristics vary widely between manufacturers. Some manufacturers' cells are optimized to operate more efficiently at lower current levels, making it wise to consult the battery manufacturer's discharge characteristics.

Figure 3 shows Alkaline battery discharge characteristics for four D cells. A fresh cell measures 1.5V and operates down to 0.8V before the cell dies. The battery stack voltage drops quickly and then stabilizes until it reaches 3.2V; 0.8V per cell. There is no usable battery life beyond this point.

Figure 4 shows efficiency exceeding 85%. The diode and LT1270 switch are the two main loss elements. The Schottky diode introduces a relatively constant 7% loss, while the LT1270 switch loss varies with battery voltage. As battery voltage decreases, switch current and duty cycle increase. This has a dramatic effect on switch loss, because switch loss is proportional to the square of switch current multiplied by duty cycle. Therefore, at low input voltages efficiency is degraded because this loss is a higher percentage of the battery power drain.

If lower output current is desired, an LT1170, LT1171, or LT1172 can be used.

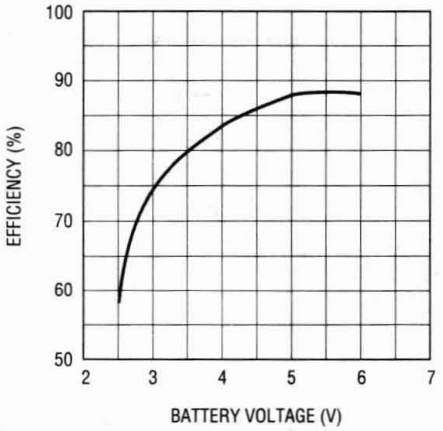


Figure 4. Efficiency for Various Battery Voltages

For literature on Switching Regulators, Call **(800) 637-5545**. For applications help, call (408) 432-1900, Ext. 456

LINEAR TECHNOLOGY
DESIGN NOTES

Number 42 in a series from Linear Technology Corporation *December, 1990*

Chopper vs Bipolar Op Amps — An Unbiased Comparison

George Erdi

Over the last few years dozens of new CMOS chopper stabilized and precision bipolar op amps have been introduced. Despite the fact that these two groups compete for the same market, a valid scientific comparison of the merits of choppers and precision bipolars is unavailable. The probable explanation is that most analog IC companies have introduced products in one group or the other, but not both. Therefore, articles and news releases have extolled the benefits of one, while knocking the other. Linear Technology is the only company with offerings in both groups with no vested interest in promoting one versus the other. Hence, an attempt will be made for an unbiased comparison.

Table 1 lists the parameters of importance. In all input parameters (except noise) the advantage unquestionably goes to the choppers. 5μV maximum offset voltage, 0.05μV/°C maximum drift are commonly found guaranteed parameters on all Linear Technology choppers. Changes with time and temperature cycling are near zero. These parameters cannot be measured accurately, but can be guaranteed by design; assuming that the auto-zeroing chopper loop, which can be tested independently, is working properly. The best, tightly specified bipolar op amps can only approach this performance, at the cost of great testing and yield expense.

Table 1. Chopper Stabilized vs Precision Bipolar Op Amps

PARAMETER	ADVANTAGE		COMMENTS
	CHOPPER	BIPOLAR	
Offset Voltage	✓		No Contest
Offset Drift	✓		
All Other DC Specs	✓		
Wideband, 20Hz to 1MHz		✓	See Details in Text
Noise		✓	See Details in Text
Output: Light Load	✓		Rail to Rail Swing
Heavy Load		✓	2mA Limit on Choppers
Single Supply Application	✓		Inherent to Choppers Needs Special Design Bipolars
±15V Supply Voltage		✓	Except LTC1150
Prejudice/Tradition		✓	Still a Chopper Problem
Cost		✓	Unless DC Performance Needed

In wideband applications bipolars get the nod. This may seem inconsistent, since typical chopper slew rate is 4V/μs, bandwidth is 2.5MHz — faster than most precision op amps. But choppers have clock frequency spikes, chopping frequency spikes, aliasing errors, millisecond overload recovery, and high wideband noise. All these factors limit the choppers' usefulness as wideband amplifiers.

The noise performance of bipolars is acknowledged to be superior. As shown in Figure 1 from 10Hz to 1kHz bipolar noise is nine times better. This comparison is for the industry standard LT1001 and OP-07. Bipolar designs optimized for low noise, such as the LT1007,

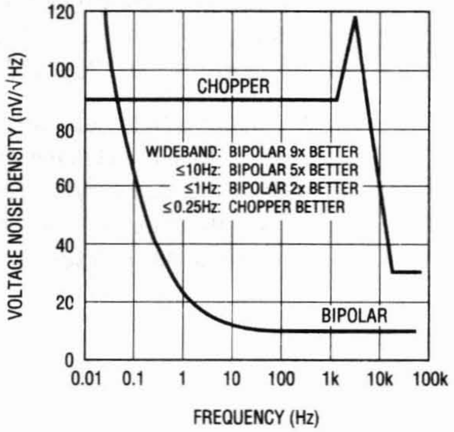


Figure 1. Bipolar vs Chopper Noise Comparison

Table 2. Chopper Stabilized Op Amps

PART NUMBER	DESCRIPTION	MAX V_{OS} (25°C)	MAX TCV_{OS}	TYPICAL 0.1Hz TO 10Hz NOISE	EXTERNAL CAPS REQUIRED	MAXIMUM SUPPLY VOLTAGE
LTC1049	Single, Micropower	10μV	0.10μV/°C	3.0μVp-p	No	± 9V
LTC1050	Single, Low Power	5μV	0.05μV/°C	1.6μVp-p	No	± 9V
LTC1051	Dual, Low Power	5μV	0.05μV/°C	1.5μVp-p	No	± 9V
LTC1052	Single, 7652 Upgrade	5μV	0.05μV/°C	1.5μVp-p	Yes	± 9V
LTC1053	Quad, Low Power	5μV	0.05μV/°C	1.5μVp-p	No	± 9V
LTC1150	Single, ± 15V Operation	5μV	0.05μV/°C	1.8μVp-p	No	± 18V

Table 3. Precision Bipolar Op Amps

DESCRIPTION	SINGLE	DUAL	QUAD
Low Cost, Optimum Performance	LT1001 LT1012 LT1097	LT1013 LT1078	LT1014 LT1079
Low Noise, Wideband	LT1007 LT1028 LT1037		
Low Noise, Audio	LT1115		
Single Supply, Low Power	LT1006	LT1013	LT1014
Single Supply, Micropower	LT1077	LT1078 LT1178	LT1079 LT1179

LT1028, LT1037, or LT1115, have 36 to 100 times lower noise than choppers. But choppers do not have 1/f noise, i.e. as frequency decreases bipolar noise increases, while chopper noise stays flat. If the bandwidth is limited chopper noise gets comparatively better. If signal bandwidth is cut-off at 0.25Hz — a rather restrictive requirement — chopper noise is actually lower.

Chopper stabilized amplifiers are also limited to ± 9V maximum supplies, excluding them from the mainstream ± 15V analog applications. The new LTC 1150 is the exception. The LTC1150 represents a major breakthrough; it plugs into standard ± 15V sockets, yet guarantees the expected 5μV offset and 0.05μV/°C drift.

A non-scientific, yet real, parameter of comparison is prejudice/tradition. Early CMOS circuits have established a reputation of being damaged easily by electrostatic discharge, and latching up under normal operating conditions. Most of the problems were solved years ago, yet the negative impression lingers. Many system designers will not try, and therefore will not use, CMOS choppers.

The cost of precision bipolar op amps is lower than choppers. For example, the 1000 piece price of the LT1097CN8 (50μV max offset voltage, 1μV/°C max drift) is $0.97 versus the LTC1050CN8's $2.10. This, however, is somewhat of an apples to oranges comparison, because the LTC1050CN8's offset and drift performance cannot be obtained at any price on a bipolar op amp.

Table 2 summarizes Linear Technology's chopper-stabilized op amp offerings. Table 3 lists the currently available precision bipolar operational amplifiers.

For literature on our Chopper Stabilized
and Precision Bipolar Operational Amplifiers
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DESIGN NOTES

Number 43 in a series from Linear Technology Corporation *January, 1991*

LT1056 Improved JFET Op Amp Macromodel Slews Asymmetrically

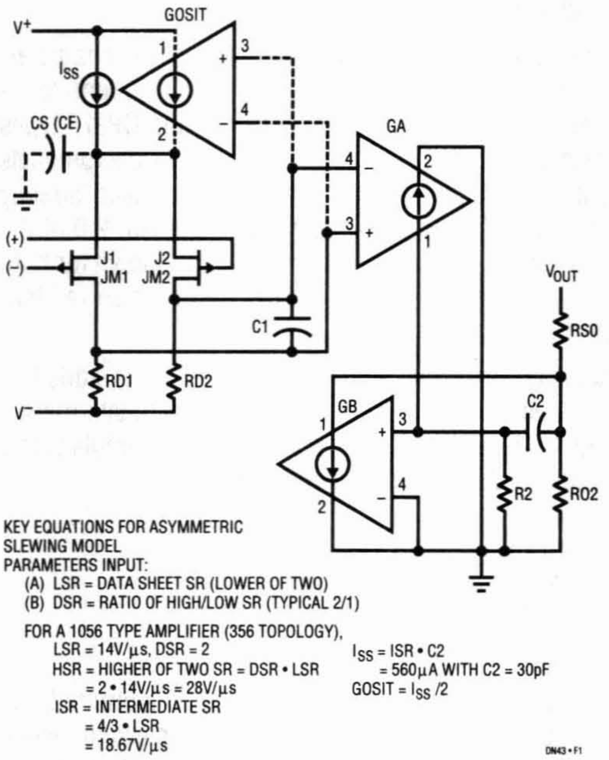
Walt Jung

SPICE macromodels for op amps have been available for some time, for both bipolar[1,2] and JFET[3] input stage device types. Interestingly however, not much attention has been given in the models available to controlled slewing asymmetry. Dependent upon a given amplifier design topology, the large signal characteristics can have various degrees of slew rate (SR) asymmetry. It therefore makes sense to have models which emulate real IC parts in this regard.

A case in point is that of the available P-channel JFET input op amps, many which have a characteristic SR response which is asymmetrical. In fact, popular op amps with topologies like the original 355/356 types are intrinsically faster for negative going output swings than they are for positive. Similar comments apply to such related devices as the OP15, OP16, etc. Since this type of JFET device topology was introduced, the SR specified on the data sheet has typically been the **lower** of two dissimilar rates, i.e., the slower, **positive edge** SR. Thus, given an op amp with a typical SR spec of 14V/µs for positive going edges, the same amp will have a corresponding negative SR of about 28V/µs.

Ironically, this quite common JFET amplifier slewing characteristic has not been well modeled thus far. Most macromodels currently available simply do not address the asymmetric SR issue at all. Others have means of modeling it, but it is seldom found used.

A means of SR control was built into the original Boyle[1] model, and it addresses SR asymmetry for common mode (CM) signals by means of a common emitter (source) capacitor, CE (CS, for JFET amps). However, using this capacitor alone for a general SR symmetry control mechanism leaves something to be desired, as the resulting slopes are not consistent. LTC has implemented a new means of modeling SR asymmetry, shown in Figure 1.



KEY EQUATIONS FOR ASYMMETRIC
SLEWING MODEL
PARAMETERS INPUT:
(A) LSR = DATA SHEET SR (LOWER OF TWO)
(B) DSR = RATIO OF HIGH/LOW SR (TYPICAL 2/1)

FOR A 1056 TYPE AMPLIFIER (356 TOPOLOGY),
LSR = 14V/µs, DSR = 2
HSR = HIGHER OF TWO SR = DSR • LSR
= 2 • 14V/µs = 28V/µs
ISR = INTERMEDIATE SR
= 4/3 • LSR
= 18.67V/µs

I_{SS} = ISR • C2
= 560µA WITH C2 = 30pF
GOSIT = I_{SS} /2

Figure 1. The LTC Asymmetric Slewing JFET Macromodel Has Little Additional Complexity, But Offers Controlled Slewing Response.

The circuit as shown here is a simplified Boyle type model with P-channel JFET input devices, J1 and J2. As this type (or similar input structure) of model is typically used, the SR is simply I_{SS}/C2, which is symmetrical when CS is zero. When the common source capacitor CS is added, the SR for CM signals can be adapted (corresponds to CE in the Boyle paper). Unfortunately, this strategy works best for CM amplifier inputs, and not as well for inverting inputs.

The LTC method of modeling asymmetrical SR employs an added VCCS (shown dotted), which dynamically modifies the total tail current available to J1/J2. This controlled source, "GOSIT," is driven by the differential output of J1/J2 and produces a current which adds to or subtracts from the fixed current, I_{SS}. The resulting current available to charge/discharge compensation cap C2 is thus higher for one slewing slope than it is for the opposite. This is true regardless of whether the amplifier is operating in an inverting or non-inverting input mode. As an option, CS can still be used for further control of slewing for CM inputs (shown dotted).

In generating a new macromodel with asymmetrical SR, the **lower** of the two slew rates is input from the data sheet. Also input is the **ratio** of the high-to-low SR. Algorithms in the program used by LTC then calculate an appropriate static value for I_{SS} and the gain of VCCS GOSIT, so that the proper slewing characteristic will be produced by the model.

A representative example op amp with these characteristics is the LT1056, a high performance op amp topologically much like the LF156-LF356 and OP-16 types (also produced by LTC, with corresponding macromodels available). Some sample lines of code taken directly from the LT1056 model released in version 2.0 of the LTC library are shown below. These are shown for both the asymmetric form as released, and for an (edited) symmetric case.

Actually, only one SPICE model element is added to produce the asymmetric SR as opposed to symmetric, and that is the VCCS GOSIT. The LT1056 example below produces SR of +14V/μs and −28V/μs.

```
**
C1  80  90  1.5000E-11
ISS  7  12  5.6000E-04
GOSIT  7  12  90  80  2.8000E-04
* intermediate
```

When the controlled source GOSIT is omitted, the model reverts to simple symmetric slewing, where the SR will be ±(I_{SS})/C2. This is shown below, with I_{SS} adjusted for a (symmetric) SR of 14V/μs. Those lines of code edited are shown in **bold**.

```
**
C1  80  90  1.5000E-11
* for a (symmetric) SR of 14V/μs,
* iss = (1.4e7)*(3e-11) = 420μA
ISS  7  12  4.2000E-04
* comment out gosit with first column "*"
* GOSIT  7  12  90  80  2.8000E-04
* intermediate
```

The non-inverting mode waveforms of a typical SPICE run using the LT1056 macromodel and parallel lab results with an actual LT1056 device are shown in Figures 2A and 2B, respectively. As noted, there is quite reasonable correspondence between the two. A complete LT1056 model is contained on the LTC SPICE diskette.

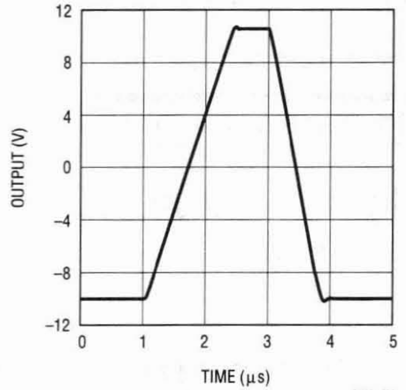


Figure 2A. LT1056 SR (+) Mode, Macromodel

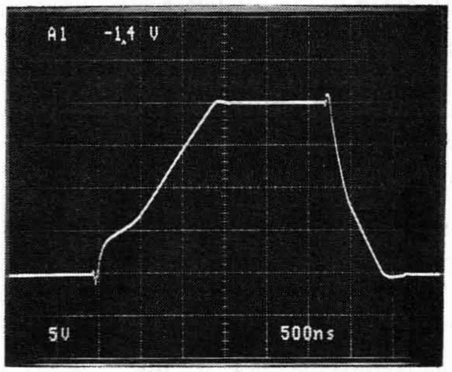


Figure 2B. LT1056 SR (+) Mode, Lab Photo

References

Available from LTC literature service, at (800) 637-5545 are copies of the latest LTC SPICE macromodel library on either a 5.25" or a 3.5" high density floppy diskette.

1. Boyle, G.R., Cohn, B.M., Pederson, D.O., Solomon, J.E., "Macromodeling of Integrated Circuit Operational Amplifiers," *IEEE Journal of Solid-State Circuits*, Vol. SC-9, #6, December 1974.
2. Solomon, J.E., "The Monolithic Op Amp: A Tutorial Study," *IEEE Journal of Solid-State Circuits*, Vol. SC-9, #6, December 1974.
3. Krajewska, G., Holmes, F.E., "Macromodeling of FET/Bipolar Operational Amplifiers," *IEEE Journal of Solid-State Circuits*, Vol. SC-14, # 6, December 1979.

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LINEAR TECHNOLOGY

DESIGN NOTES

Number 44 in a series from Linear Technology Corporation *February, 1991*

A Simple Ultra-Low Dropout Regulator

Jim Williams

Switching regulator post regulators, battery powered apparatus, and other applications frequently require low drop-out linear regulators. Often, battery life is significantly affected by the regulator's dropout performance. Figure 1's simple circuit offers lower dropout voltage than any monolithic regulator. Dropout is below 50mV at 1A, increasing to only 450mV at 5A. Line and load regulation are within 5mV, and initial output accuracy is inside 1%. Additionally, the regulator is fully short circuit protected, and has a no load quiescent current of 600μA.

Circuit operation is straightforward. The 3-pin LT1123 regulator (TO-92 package) servo controls Q1's base to maintain its feedback pin (FB) at 5V. The 10μF output capacitor provides frequency compensation. If the circuit is located more than six inches from the input source the optional 10μF capacitor should bypass the input. The optional 20Ω resistor limits LT1123 power dissipation and is selected based upon the maximum expected input voltage (see Figure 2).

Normally, configurations of this type offer unpredictable short circuit protection. Here, the MJE1123 transistor shown has been specially designed for use with the LT1123. Because of this, beta based current limiting is practical. Excessive output current causes the LT1123 to pull down harder on Q1 until beta limiting occurs. Under these conditions the controlled pull down current combines with Q1's beta and safe operating area characteristics to provide reliable short circuit limiting. Figure 3 details current limit characteristics for 30 randomly selected transistors.

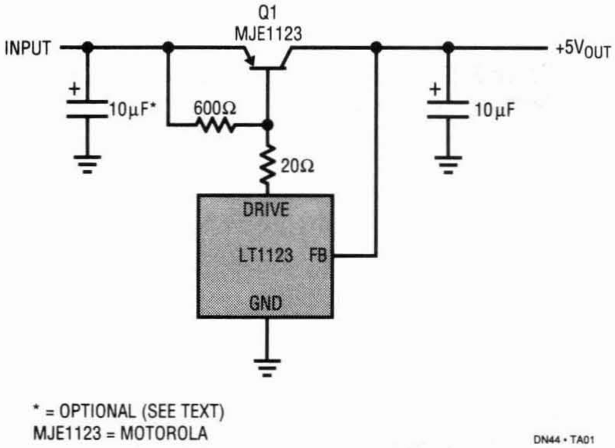


Figure 1. The Ultra-Low Dropout Regulator. LT1123 Combines with Specially Designed Transistor for Lowest Dropout and Short Circuit Protection.

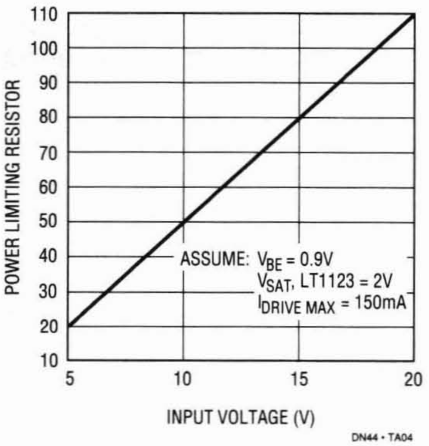


Figure 2. LT1123 Power Dissipation Limiting Resistor Value vs Input Voltage

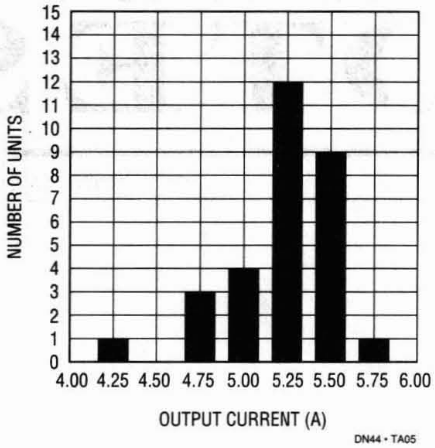


Figure 3. Short Circuit Current for 30 Randomly Selected MJE1123 Transistors at V_{IN} = 7V

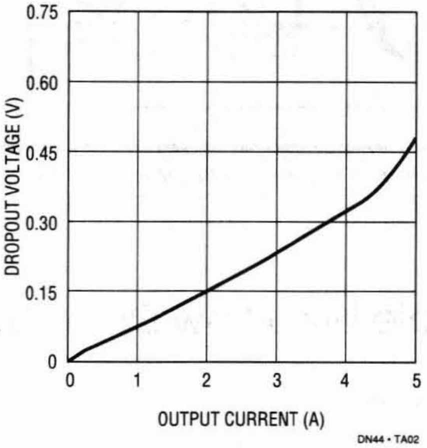


Figure 4. Dropout Voltage vs Output Current

Figure 4 shows dropout characteristics. Even at 5A, dropout is about 450mV, decreasing to only 50mV at 1A. Monolithic regulators cannot approach these figures, primarily because monolithic power transistors do not offer Q1's combination of high beta and excellent saturation. For comparison, Figure 5 compares the circuits performance against some popular monolithic regulators. Dropout is ten times better than 138 types, and significantly better than the other types shown. Because of Q1's high beta, base drive loss is only 1%-2% of output current, even at full 5A output. This maintains high efficiency under the low $V_{IN} - V_{OUT}$ conditions the circuit will typically operate at. As an exercise, the MJE1123 was replaced with a 2N4276, a Germanium device. This combination provided even lower dropout performance, although current limit characteristics cannot be guaranteed.

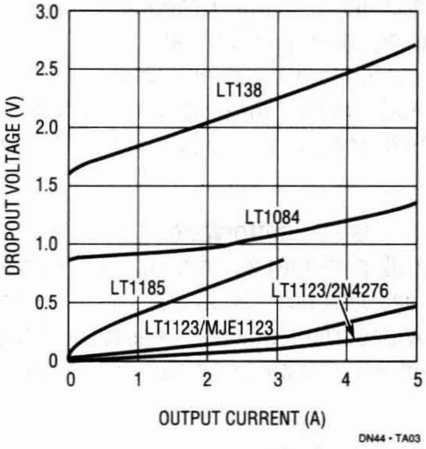


Figure 5. Dropout Voltage vs Output Current for Various Regulators

For literature on our Low Dropout Regulators, call **(800) 637-5545**. For applications help, call (408) 432-1900, Ext. 456

DESIGN NOTES

Number 45 in a series from Linear Technology Corporation *March, 1991*

Signal Conditioning for Platinum Temperature Transducers

Jim Williams

High accuracy, stability, and wide operating range make platinum RTDs (resistance temperature detectors) popular temperature transducers. Signal conditioning these devices requires care to utilize their desirable characteristics. Figure 1's bridge based circuit is highly accurate and features a ground referred RTD. The ground connection is often desirable for noise rejection. The bridges RTD leg is driven by a current source while the opposing bridge branch is voltage biased. The current drive allows the voltage across the RTD to vary directly with its temperature induced resistance shift. The difference between this potential and that of the opposing bridge leg forms the bridges output.

A1A and instrumentation amplifier A2 form a voltage controlled current source. A1A, biased by the LT1009 reference, drives current through the 88.7Ω resistor and the RTD. A2, sensing differentially across the 88.7Ω resistor, closes a loop back to A1A. The 2k-0.1µF combination sets amplifier rolloff, and the configuration is stable. Because A1A's loop forces a fixed voltage across the 88.7Ω resistor, the current through Rp is constant. A1's operating point is primarily fixed by the 2.5V LT1009 voltage reference.

The RTD's constant current forces the voltage across it to vary with its resistance, which has a nearly linear positive temperature coefficient. The non-linearity could cause several degrees of error over the circuit's 0°C-400°C operating range. The bridges output is fed to instrumentation amplifier A3, which provides differential gain while simultaneously supplying non-linearity

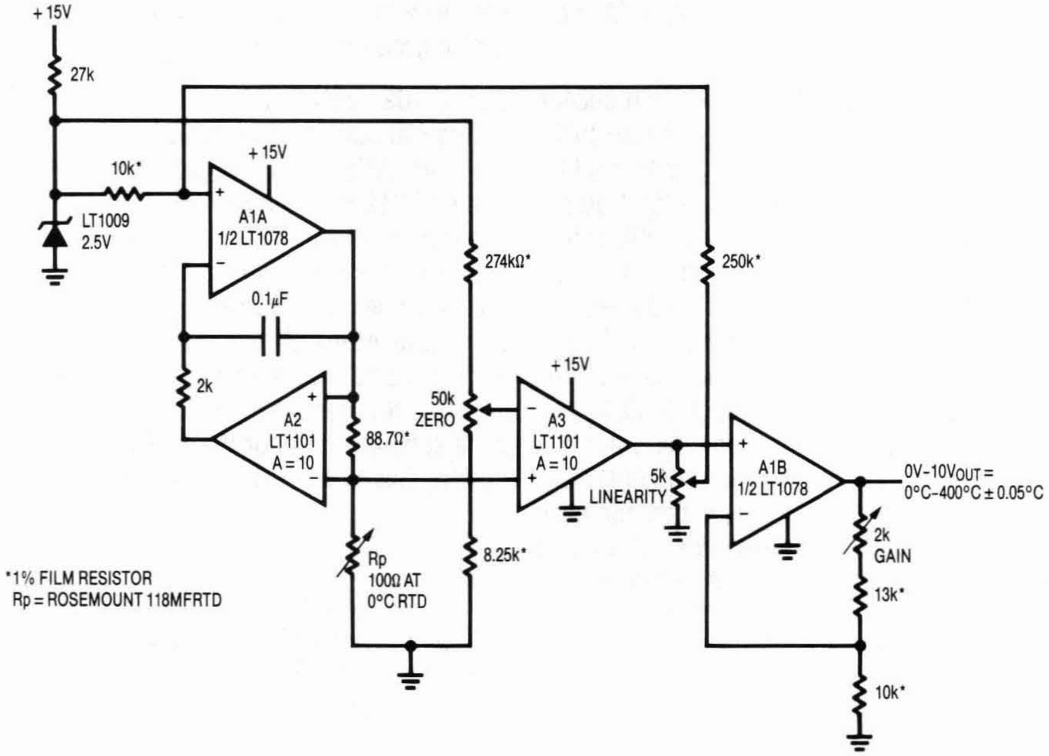

+15V
27k
10k*
LT1009
2.5V
+15V
A1A
1/2 LT1078
0.1µF
274kΩ*
250k*
2k
A2
LT1101
A = 10
88.7Ω*
50k
ZERO
+15V
A3
LT1101
A = 10
5k
LINEARITY
A1B
1/2 LT1078
0V-10V$_{OUT}$ =
0°C-400°C ± 0.05°C
2k
GAIN
13k*
10k*
Rp
100Ω AT
0°C RTD
8.25k*
*1% FILM RESISTOR
Rp = ROSEMOUNT 118MFRTD

Figure 1. Linearized Platinum RTD Bridge. Feedback to Bridge from A3 Linearizes the Circuit.

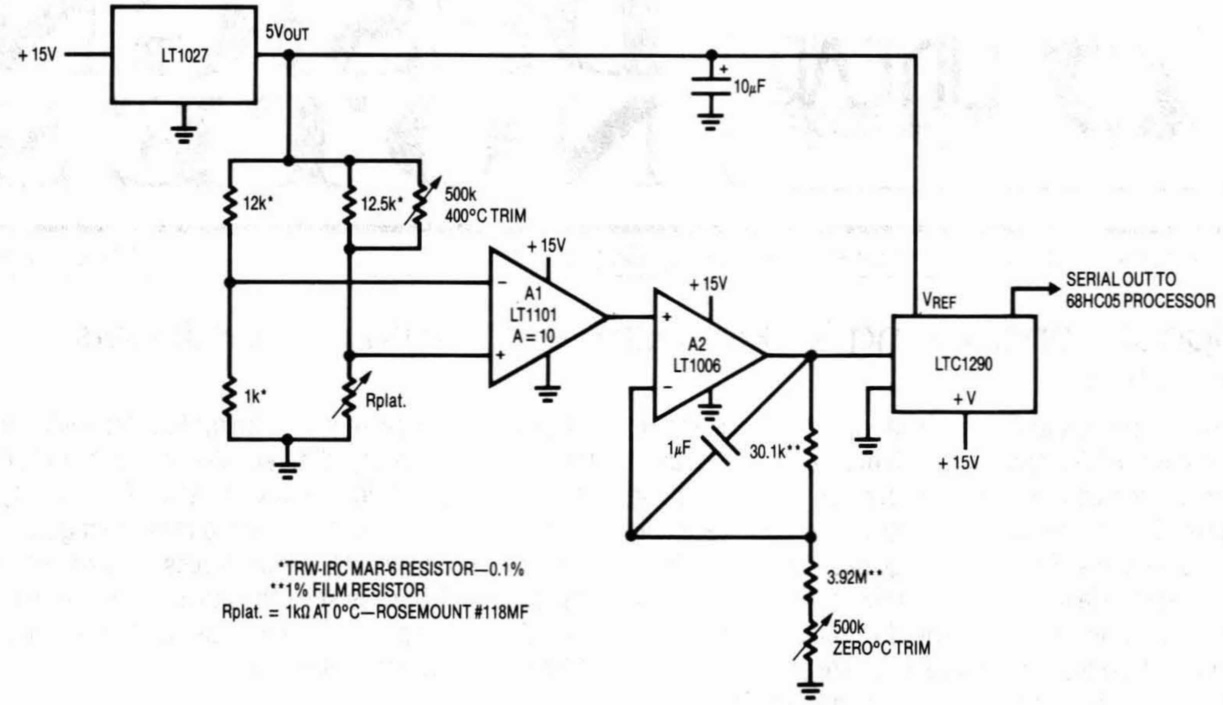


Figure 2. Digitally Linearized Platinum RTD Signal Conditioner

correction. The correction is implemented by feeding a portion of A3's output back to A1's input via the 10k-250k divider. This causes the current supplied to Rp to slightly shift with its operating point, compensating sensor non-linearity to within ±0.05°C. A1B, providing additional scaled gain, furnishes the circuit output.

To calibrate this circuit, substitute a precision decade box (e.g., General Radio 1432k) for Rp. Set the box to the 0°C value (100.00Ω) and adjust the zero trim for a 0.00V output. Next, set the decade box for a 140°C output (154.26Ω) and adjust the gain trim for a 3.500V output reading. Finally, set the box to 249.0Ω (400.00°C) and trim the linearity adjustment for a 10.000V output. Repeat this sequence until all three points are fixed. Total error over the entire range will be within ±0.05°C. The resistance values given are for a nominal 100.00Ω (0°C) sensor. Sensors deviating from this nominal value can be used by factoring in the deviation from 100.00Ω. This deviation, which is manufacturer specified for each individual sensor, is an offset term due to winding tolerances during fabrication of the RTD. The gain slope of the platinum is primarily fixed by the purity of the material and has a very small error term.

The previous example relies on analog techniques to achieve a precise, linear output from the platinum RTD bridge. Figure 2 uses digital corrections to obtain similar results. A processor is used to correct residual RTD non-linearities. The bridges inherent non-linear output is also accommodated by the processor.

The LT1027 drives the bridge with 5V. The bridge differential output is extracted by instrumentation amplifier A1. A1's output, via gain scaling stage A2, is fed to the LTC1290 12-bit A-D. The LTC1290's raw output codes reflect the bridges non-linear output versus temperature. The processor corrects the A-D output and presents linearized, calibrated data out. RTD and resistor tolerances mandate zero and full scale trims, but no linearity correction is necessary. A2's analog output is available for feedback control applications. The complete software code for the 68HC05 processor, developed by Guy M. Hoover, appears in Application Note 43.

For literature on our Amplifiers and Data Converters, call **(800) 637-5545**. For applications help, call (408) 432-1900, Ext. 456

DESIGN NOTES

Current Feedback Amplifier "Do's and Don'ts" – 46

William H. Gross

Introduction

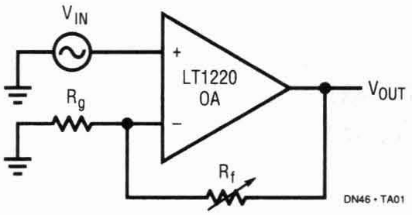
The introduction of current feedback amplifiers, such as the LT1223, has significantly increased the designer's ability to solve difficult high speed amplifier problems. The current feedback architecture has very high slew rate and the small signal bandwidth is fairly constant for all gains. Current feedback amplifiers are used in broadcast video systems, radar systems, IF and RF stages, RGB distribution systems and many other high speed circuits.

As with any new circuit, there are several new rules that must be kept in mind to prevent problems. Because current feedback amplifiers act very much the same as regular op amps, it is important to note the differences and show how some standard op amp circuits should be implemented.

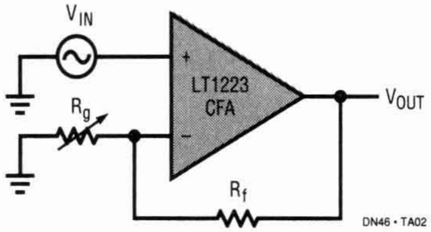
The most important thing to remember about current feedback amplifiers is that the impedance at the inverting (negative) input sets the bandwidth and therefore the stability of the amplifier. It should be resistive, not capacitive. To slow the amplifier down, increase the resistance driving the inverting input. If the amplifier peaks too much due to capacitive loading, or anything else, increase the value of the feedback resistors.

The best way to demonstrate how to use current feedback amplifiers is to show some example circuits. To make it as painless as possible, I will show the traditional op amp implementation next to the current feedback amplifier version.

Op Amp Adjustable Gain Amp

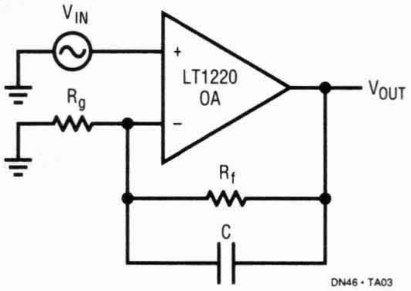


Current Feedback Amp Adjustable Gain Amp

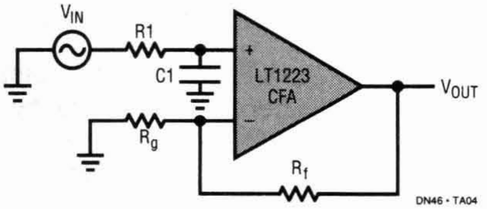


With a standard op amp you can vary the gain of the amplifier with either R_f or R_g. The only real restriction on the values is the loading affect the resistors have on the amplifier output. With a current feedback amplifier the value of R_f should not be varied. If R_f is a pot, then the bandwidth will be reduced at minimum gain and the circuit will oscillate when R_f is very small.

Op Amp Bandwidth Limiting

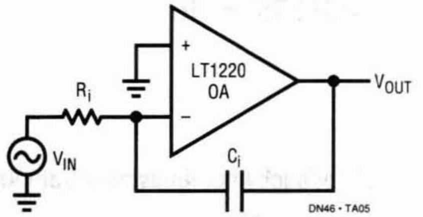


Current Feedback Amp Bandwidth Limiting

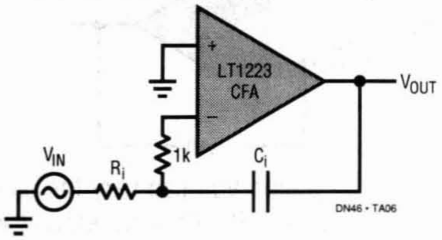


It is very common to limit the bandwidth of an op amp by putting a small capacitor in parallel with R_f. This works with all unity gain stable op amps; DO NOT PUT A SMALL CAPACITOR FROM THE INVERTING INPUT OF A CURRENT FEEDBACK AMPLIFIER TO ANYWHERE, ESPECIALLY NOT TO THE OUTPUT. The capacitor on the inverting input will cause peaking or oscillations. If you need to limit the bandwidth of a current feedback amplifier, use a resistor and capacitor at the non-inverting input (R1 and C1). This technique will also cancel (to a degree) the peaking caused by stray capacitance at the inverting input. Unfortunately, this will not limit the output noise the way it does for the op amp.

Op Amp Integrator

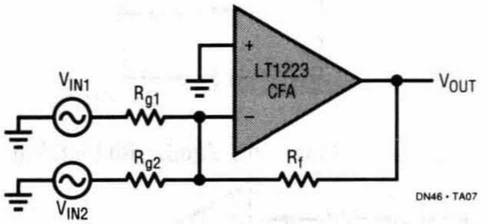


Current Feedback Amplifier Integrator



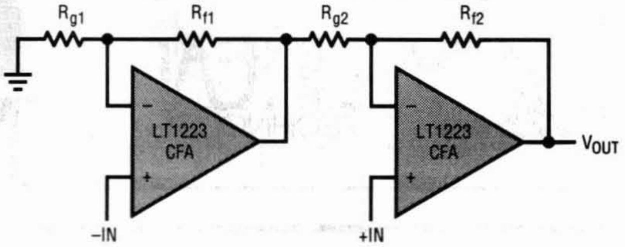
The integrator is one of the easiest circuits to make with an op amp. However, the circuit must be modified before a current feedback amplifier can be used. Since we remember that the inverting input wants to see a resistor, we can add one to the standard circuit. This generates a new summing node where we can apply capacitive feedback. The new current feedback amplifier compatible integrator works just like you would expect; it has excellent large signal capability and accurate phase shift at high frequencies.

Current Feedback Amplifier Summer (DC Accurate)



There is no I_{OS} spec on current feedback amplifiers because there is no correlation between the two input bias currents. Therefore we will not improve the DC accuracy of the inverting amplifier by putting an extra resistor in the non-inverting input. This is also true of input bias current canceled op amps where the I_{OS} spec is the same as the I_B spec, such as the LT1220.

Two Amplifier Instrumentation Amp



TRIM R_{g2} FOR GAIN, THEN TRIM R_{g1} FOR CMRR. VOLTAGE GAIN, G, IS V_{OUT} DIVIDED BY DIFFERENCE BETWEEN +IN AND –IN.

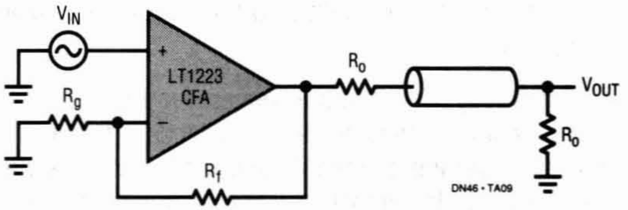
OP AMP DESIGN EQUATIONS:
$R_{f1} = R_{g2}$; $R_{f2} = (G–1)\ R_{g2}$; $R_{g1} = R_{f2}$

CURRENT FEEDBACK AMP DESIGN EQUATIONS:
$R_{f1} = R_{f2}$; $R_{g1} = (G–1)\ R_{f2}$; $R_{g2} = \frac{R_{f2}}{G–1}$

DN46 • TA08

The two amplifier instrumentation amp is easily modified for current feedback amplifiers. The only necessary change is to make the feedback resistor of each amplifier the same and therefore make the gain setting resistors different. This way the bandwidth of both amps is the same and the common mode rejection at high frequencies is better than that of the op amp circuit. In the op amp circuit one amplifier has maximum bandwidth, since it runs at about unity gain, while the other is limited to its gain bandwidth product divided by the gain.

Cable Driver



The cable driver circuit is the same for both types of amplifiers. But because most op amps do not have enough output drive current, they are not often used for heavy loads like cables. When driving a cable it is important to properly terminate both ends if even modest high frequency performance is required. The additional advantage of this is that it isolates the capacitive load of the cable from the amplifier so it can operate at maximum bandwidth.

For literature on our Current Feedback Amplifiers, call **(800) 637-5545**. For applications help, call (408) 432-1900, Ext. 456

DESIGN NOTES

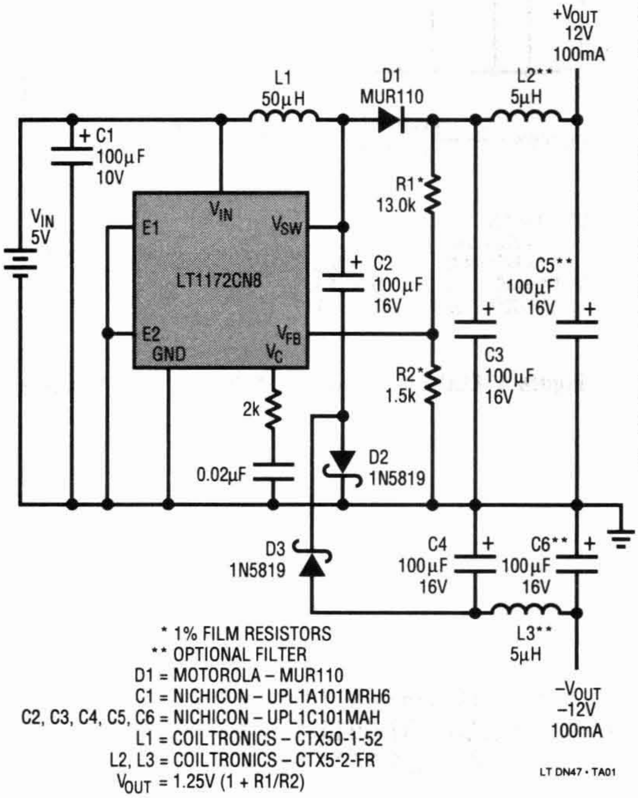
Switching Regulator Generates Both Positive and Negative Supply with a Single Inductor – Design Note 47

Brian Huffman

Many systems require ±12V from a 5V input. Analog or RS-232 driver power supplies are obvious candidates. This requirement is usually solved by using a switcher with a multiple-secondary transformer or multiple switchers. These solutions can be complicated, requiring either transformer design or two inductors. An alternative approach, shown in Figure 1, uses a single inductor and charge pump to obtain the dual outputs. This solution is particularly noteworthy because is uses off-the-shelf components.

Figure 1 uses an LT1172 to generate both the positive and negative supply. The LT1172 is configured as a step-up converter to obtain the positive output. To generate the negative output a charge pump is used. The pump capacitor, C2, is charged up by the inductor when D2 is forward biased and discharges into C4 when the LT1172's power switch pulls the positive side of C2 to ground. The output capacitor provides current to the load during the charging cycle.

Figure 2 shows the regulator's operating waveforms. Since the LT1172 has a ground referred power switch, the inductor has the input voltage applied across it when the switch is on. Trace A is the V_{SW} pin voltage and trace B is its current. The inductor current, trace C, rises slowly as the magnetic field builds up. The current rate of change is determined by the voltage applied across the inductor and its inductance. During this interval, energy is being stored in the inductor and no power is transferred to the +12V output. When the switch is turned off, energy is no longer transferred to the inductor, which causes the magnetic field to collapse. The collapsing magnetic field induces a change in voltage across the inductor causing the V_{SW} pin to rise until output diode D1 forward biases.



* 1% FILM RESISTORS
** OPTIONAL FILTER
D1 = MOTOROLA – MUR110
C1 = NICHICON – UPL1A101MRH6
C2, C3, C4, C5, C6 = NICHICON – UPL1C101MAH
L1 = COILTRONICS – CTX50-1-52
L2, L3 = COILTRONICS – CTX5-2-FR
V_{OUT} = 1.25V (1 + R1/R2)

Figure 1. Inductor and Switch Capacitor Techniques Provide Bipolar Output

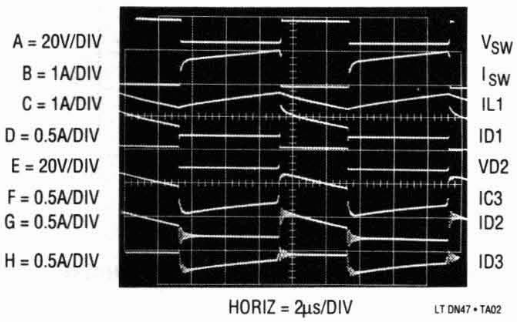


Figure 2. Switching Waveforms for ±12V Output Converter

Trace D is the diode's current waveform. The diode provides a current path for the energy stored in the inductor to be transferred between the load and the output capacitor. When the diode is reverse biased, the output capacitor provides the load current. The LT1172's error amplifier compares the feedback pin voltage, from the 13kΩ–1.5kΩ divider, to its internal 1.24V reference and controls duty cycle. The output voltage can be varied by changing the R1–R2 divider ratio (see Equation 1). An RC network at the V_C pin provides loop compensation.

A charge pump is used to invert the +12V output to a –12V output. When the LT1172's power switch turns off, the voltage on C2's positive side rises until D1 is forward biased. The inductor charges C2 when the voltage on C2's negative side rises enough to forward bias D2. Trace F shows C2's current waveform, trace E is D2's voltage waveform and trace G is its current. The voltage across C2 will be equal to a diode drop above $+V_{OUT}$ minus a Schottky diode drop. When the LT1172's power transistor turns on, the positive side of C2 is pulled to ground. During this period diode D3 is forward biased (trace H is its current waveform), and C4 is charged by C2. An optional LC filter is added to each output to attenuated output voltage ripple. Efficiency for this circuit generally exceeds 70%.

Diode junction losses (D2 and D3) preclude ideal results, but performance is quite good. This circuit will convert $+V_{OUT}$ to $-V_{OUT}$ with losses as shown in Figure 3. Negative output load current should not exceed the positive output load by more than a factor of 5, otherwise the imbalance will cause the –12V transient response to suffer.

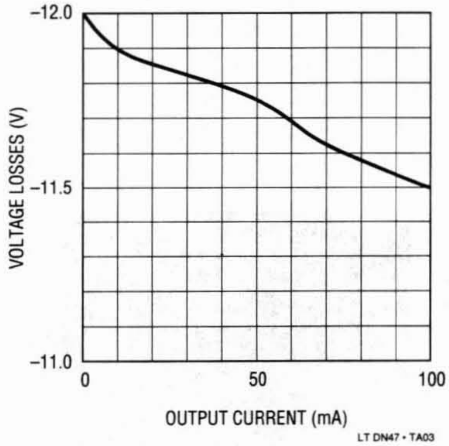
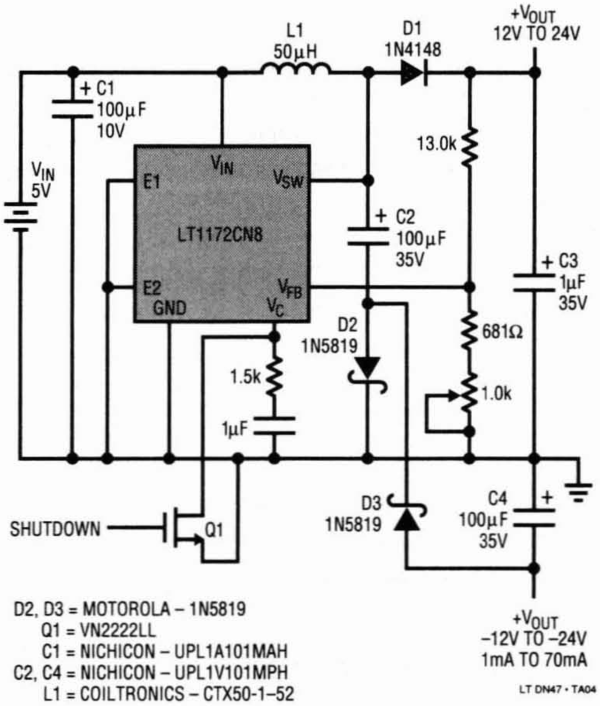


Figure 3. Losses for Charge Pump Converter

Figure 4 can be used for a LCD display contrast control. It is similar to the previous circuit except that all the load current is drawn from the negative output. This requires C3 to be small so negative output load fluctuations are quickly reflected to the positive output. Resistor R3 adjusts output voltage between –12V to –21V.

The LT1172 provides an elegant solution to power shutdown problems by integrating a shutdown feature; eliminating the need to place a power MOSFET in series with the input voltage. When the voltage of the V_C pin is pulled below 150mV, the IC shuts down pulling only 150µA. This is implemented by turning on Q1, reducing the circuit's quiescent current from 6mA to 150µA.



L1
50µH
D1
1N4148
$+V_{OUT}$
12V TO 24V
+ C1
100µF
10V
13.0k
V_{IN}
5V
V_{IN}
E1
V_{SW}
LT1172CN8
+ C2
100µF
35V
+ C3
1µF
35V
E2
GND
V_{FB}
V_C
D2
1N5819
681Ω
1.5k
1.0k
1µF
SHUTDOWN
Q1
D3
1N5819
C4
100µF
35V
D2, D3 = MOTOROLA – 1N5819
Q1 = VN2222LL
C1 = NICHICON – UPL1A101MAH
C2, C4 = NICHICON – UPL1V101MPH
L1 = COILTRONICS – CTX50-1-52
$+V_{OUT}$
–12V TO –24V
1mA TO 70mA
LT DN47 • TA04

Figure 4. LCD Display Contrast Control Power Supply

For literature on our Regulators, call **(800) 637-5545**. For applications help, call (408) 432-1900, Ext. 361.

DESIGN NOTES

No Design Switching Regulator
5V, 5A Buck (Step Down) Regulator – Design Note 48

Ron Vinsant

Introduction

This simple, no design regulator, is a step down DC to DC converter designed to convert an 8V to 40V input to a regulated 5V output. The 5V output is capable of sourcing up to 5A of output current.

This converter is based on the Linear Technology LT1074 switching regulator IC. This device needs only a few external parts to make up a complete regulator including thermal protection and current limit. This design uses off-the-shelf parts for low cost and easy availability of components. Specifications for the circuit are in Table 1.

Circuit Description

Figure 1 shows the schematic of the circuit. For the purpose of this explanation assume that the output is at a constant +5V DC and that the input voltage is greater than +8V DC.

At intervals of ≈10μs (100kHz) the control portion of the LT1074 turns on the switch transistor between the V_{IN} and V_{SW} pins impressing a voltage across the inductor, L1. This causes current to build up in the inductor while also supplying current to the load and capacitor C1.

The control circuit determines when to turn off the switch during the 10μs interval to keep the output voltage at +5V DC. When the switch transistor turns off, the magnetic field in the inductor collapses and the polarity of the voltage across the inductor changes to try and maintain the current in the inductor. This current in the inductor is now directed (due to the change in voltage polarity across the inductor) by the diode, D1, to the load. The current will flow from the inductor until the switch turns on again, (continuous operation) or until the inductor runs out of energy (discontinuous operation).

Referring back to Figure 1, the divider circuit of R1 and R2 is used to set the output voltage of the supply against an internal voltage reference of 2.21V DC.

R3 and C2 make up the frequency compensation network used to stabilize the feedback loop.

Conclusion

This Design Note demonstrates a fully characterized step down converter circuit that is both simple and low cost. This design can be taken and reliably used in a production environment without the need for any custom components. A P.C. board layout and FAB drawing are available from Linear Technology.

Table 1. Performance Summary (Operating Temperature Range 0°C to 50°C)

Input Voltage Range			+8.0V to +40.0V DC
Output	Output Voltage (±0.15V DC)		+5.00V DC
	Max Output Current V_{IN} = 8.0V to 40.0V		5.0A DC
	Typical Output Ripple at I_{OUT} = 4.0A DC @ Switching Frequency	With Optional Filter (L2 & C4) Without Optional Filter (L2 & C4)	5mVp-p 50mVp-p
	Load Regulation V_{IN} = 8V	At I_{OUT} = 0.5A DC to I_{OUT} = 5.0A DC	0.5%
	Line Regulation I_{OUT} = 5A	At V_{IN} = +8.0V DC to V_{IN} = +40.0V DC	0.5%

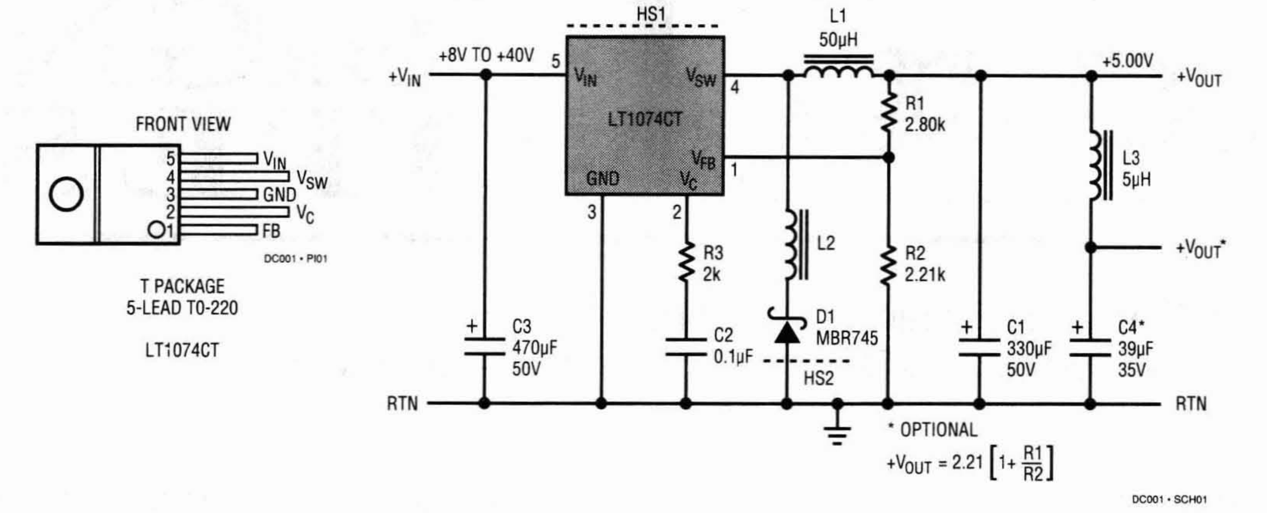

FRONT VIEW
5 VIN
4 VSW
3 GND
2 VC
1 FB
DC001 • PI01
T PACKAGE
5-LEAD TO-220
LT1074CT
HS1
+VIN
+8V TO +40V
5
VIN
VSW
4
LT1074CT
VFB
1
GND
VC
3
2
L1
50µH
+5.00V
+VOUT
R1
2.80k
L3
5µH
+VOUT*
R3
2k
L2
R2
2.21k
D1
MBR745
HS2
C3
470µF
50V
C2
0.1µF
C1
330µF
50V
C4*
39µF
35V
RTN
RTN
* OPTIONAL
+VOUT = 2.21 [1+ R1/R2]
DC001 • SCH01

Figure 1. Package and Schematic Diagrams

Table 2. Parts List

REFERENCE DESIGNATOR	QUANTITY	PART NUMBER	DESCRIPTION	VENDOR
PCB	1	001A	PCB FAB, Buck Switching Regulator	LTC
D1	1	MBR745	Diode, Schottky, 7A, 45V	Motorola
HS2	1	6038B-TT	Heatsink	Thermalloy
L2	1	2664000101	Shield Bead	Fair-Rite
VR1	1	LT1074CT	Switching Regulator, 100kHz	LTC
HS1	1	7020B-MT	Heatsink	Thermalloy
C1	1	SXE50VB331M12X20LL	Cap, Alum Elect, 330µF, 50V	United Chemicon
C2	1	CK06BX104K	Cap, Ceramic, 0.1µF, 50V	AVX
C3	1	UPL1H471MRH	Cap, Alum Elect, 470µF, 50V	Nichicon
C4	1	UPL1V390MAH	Cap, Alum Elect, 39µF, 35V	Nichicon
L1	1	CTX50-5-MP	Inductor, 50µH, 5A	Coiltronics
L3	1	CTX5-5-FR	Inductor, 5µH, 5A	Coiltronics
R1	1	MF 1/8W 2.80kΩ	RES, MF, 1/8W, 1%, 2.80kΩ	
R2	1	MF 1/8W 2.21kΩ	RES, MF, 1/8W, 1%, 2.21kΩ	
R3	1	CF 1/4W 2kΩ	RES, CF, 1/4W, 5%, 2kΩ	

For literature on our Switching Regulators, call **(800) 637-5545**. For applications help, call (408) 432-1900, Ext. 456

DESIGN NOTES

No Design Switiching Regulator
5V Buck-Boost (Positive to Negative) Regulator – Design Note 49

Ron Vinsant

Introduction

This simple, no design regulator, operates with an input between 4.5V DC and 40V DC. It provides a –5V output at a maximum output current of 1A to 3A depending on input voltage.

This converter is based on the Linear Technology LT1074 switching regulator IC. This device needs only a few external parts to make up a complete regulator including thermal protection and current limit. This design uses off-the-shelf parts for low cost and easy availability of components. Specifications for the circuit are in Table 1.

Circuit Description

Figure 1 shows the schematic of the circuit. For the purpose of this explanation assume that the output is at a constant –5V DC and that the input voltage is greater than +4.5V DC.

At intervals of ≈10μs (100kHz) the control portion of the LT1074 turns on the switch transistor between the V_{IN} and V_{SW} pins impressing a voltage across the inductor, L1. This causes current to build up in the inductor.

The control circuit determines when to turn off the switch during the 10μs interval to keep the output voltage at –5V DC. When the switch transistor turns off, the magnetic field in the inductor collapses and the polarity of the voltage across the inductor changes to try and maintain the current in the inductor. This current in the inductor is now directed (due to the change in voltage polarity across the inductor) by the diode, D1, to the load. The current will flow from the inductor until the switch turns on again, (continuous operation) or until the inductor runs out of energy (discontinuous operation).

C2 is a low ESR type electrolytic capacitor that is used in conjunction with L1 as the output filter. C5 and L2 form a post filter that reduces output ripple further.

Referring back to Figure 1, the divider circuit of R1, R2, R3 and R4 is used to set the output voltage of the supply against an internal voltage reference of 2.21V DC.

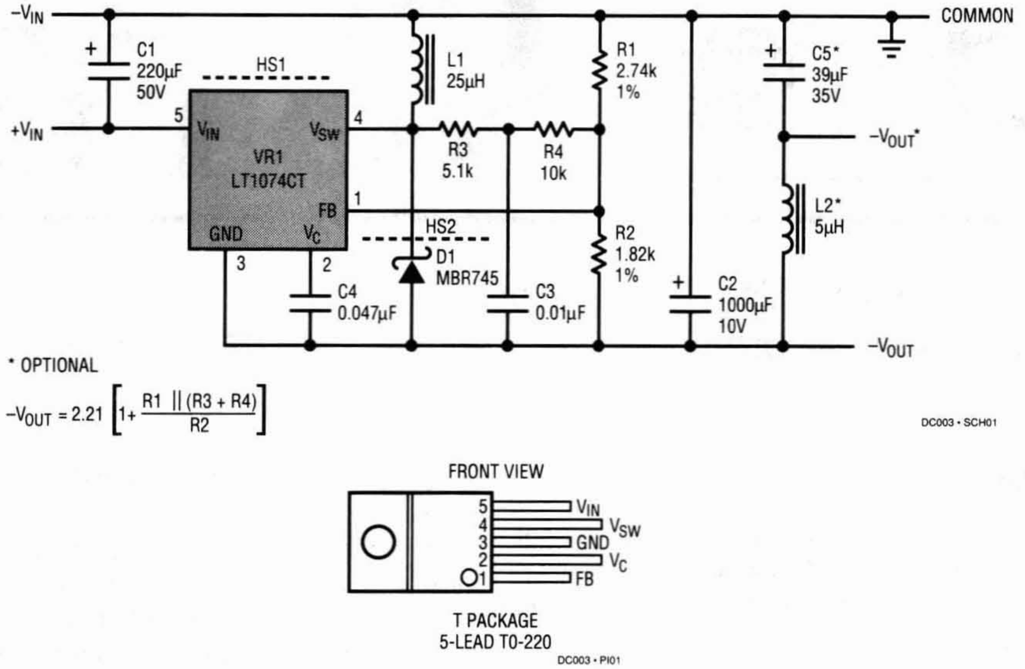
R3, R4, C3 and C4 make up the frequency compensation network used to stabilize the feedback loop.

Conclusion

This Design Note demonstrates a fully characterized positive to negative converter circuit that is both simple and low cost. This design can be taken and reliably used in a production environment without the need for any custom magnetics. A P.C. board layout and FAB drawing are available from Linear Technology.

Table 1. Performance Summary (Operating Temperature Range 0°C to 50°C)

Input Voltage Range			+4.5V to +40.0V DC
Output	Output Voltage (±0.15V DC)		– 5.00V DC
	Max Output Current At V_{IN} = 4.5V DC		1.0A DC
	Max Output Current At V_{IN} = 40.0V DC		3.5A DC
	Typical Output Ripple at I_{OUT} = 2.5A DC @ Switching Frequency	With Optional Filter (L2 & C5) Without Optional Filter (L2 & C5)	50mVp-p 300mVp-p
	Load Regulation V_{IN} = 4.5V DC	At I_{OUT} = 0.1A DC to 1.0A DC	0.6%
	Line Regulation I_{LOAD} = 1A	At V_{IN} = 4.5V DC to 40.0V DC	0.2%



$-V_{IN}$
$+V_{IN}$
C1
220µF
50V
HS1
5
V_{IN}
V_{SW}
4
VR1
LT1074CT
FB
1
GND
V_C
3
2
C4
0.047µF
L1
25µH
R3
5.1k
R4
10k
HS2
D1
MBR745
C3
0.01µF
R1
2.74k
1%
R2
1.82k
1%
C2
1000µF
10V
C5*
39µF
35V
COMMON
$-V_{OUT}$*
L2*
5µH
$-V_{OUT}$
DC003 • SCH01
FRONT VIEW
5
4
3
2
1
V_{IN}
V_{SW}
GND
V_C
FB
DC003 • PI01

* OPTIONAL

$$-V_{OUT} = 2.21\left[1 + \frac{R1\ \|\ (R3 + R4)}{R2}\right]$$

T PACKAGE
5-LEAD TO-220

Figure 1. Package and Schematic Diagrams

Table 2. Parts List

REFERENCE DESIGNATOR	QUANTITY	PART NUMBER	DESCRIPTION	VENDOR
PCB	1	003A	PCB FAB, Buck-Boost Converter	LTC
D1	1	MBR745	Diode, Schottky, 7A, 45V	Motorola
HS2	1	6038B-TT	Heatsink	Thermalloy
VR1	1	LT1074CT	Switching Regulator, 100kHz	LTC
HS1	1	7020B-MT	Heatsink	Thermalloy
C1	1	UPL1H221MPH	Cap, Alum Elect, Low ESR, 220µF, 50V	Nichicon
C2	1	LXF10VB272M12X30LL	Cap, Alum Elect, Low ESR, 1000µF, 10V	United Chemicon
C3	1	CK06BX103K	Cap, Ceramic, 0.01µF, 100V	AVX
C4	1	CK05BX473K	Cap, Ceramic, 0.047µF, 100V	AVX
C5	1	UPL1V390MAH	Cap, Alum Elect, Low ESR, 39µF, 35V	Nichicon
L1	1	CTX 25-5-52	Inductor, 25µH, 5A	Coiltronics
L2	1	CTX5-5-FR	Inductor, 5µH, 5A	Coiltronics
R1	1	MF 1/8W 2.74kΩ	RES, MF, 1/8W, 1%, 2.74kΩ	
R2	1	MF 1/8W 1.82kΩ	RES, MF, 1/8W, 1%, 1.82kΩ	
R3	1	CF 1/4W 5.1kΩ	RES, CF, 1/4W, 5%, 5.1kΩ	
R4	1	CF 1/4W 10kΩ	RES, CF, 1/4W, 5%, 10kΩ	

For literature on our Switching Regulators, call **(800) 637-5545**. For applications help, call (408) 432-1900, Ext. 456

DESIGN NOTES

High Frequency Amplifier Evaluation Board – Design Note 50

Mitchell Lee

Introduction

Demo board DC009 is designed to simplify the evaluation of high speed operational amplifiers. It includes both an inverting and non-inverting circuit, and pads are provided to allow the use of board-mounted BNC or SMA connectors. The two circuits are independent, with the exception of shared power supply and ground connections.

High Speed Layout Techniques

Layout is a primary contributor to the performance of any high speed amplifier. Poor layout techniques adversely affect the behavior of a finished circuit. Several important layout techniques, all used in demo board DC009, are described below:

Top Side Ground Plane: The primary task of a ground plane is to lower the impedance of ground connections. The inductance between any two points on a uniform sheet of copper is less than the inductance of a narrow, straight trace of copper connecting the same two points. The ground plane approximates the characteristics of a copper sheet and lowers the impedance at key points in the circuit, such as at the grounds of connectors and supply bypass capacitors.

Ground Plane Voids: Certain components and circuit nodes are very sensitive to stray capacitance. Two good examples are the summing node of the op amp and the feedback resistor. Voids are put in the ground plane in these areas to reduce stray ground capacitance.

Input/Output Matching: The width of the input and output traces is adjusted to a stripline impedance of 50Ω. Note that the terminating resistors (R3 and R7) are connected to the end of the input lines — not at the connector. While stripline techniques aren't absolutely necessary for the demo board, they are important on larger layouts where line lengths are longer. The short lines on the demo board can be terminated in 50Ω, 75Ω, or 93Ω without adversely affecting performance.

Separation of Input and Output Grounds: Even though the ground plane exhibits a low impedance, input and output grounds are still separated. For example, the termination resistors (R3 and R7) and the gain-setting resistor (R1) are grounded in the vicinity of the input connector. Supply bypass capacitors (C1, C2, C4, C5, C7, C8, C9, and C10) are returned to ground in the vicinity of the output connectors.

Optional Components

The circuit board is designed to accommodate standard 8-pin miniDIP, single operational amplifiers, such as the LT1190 and LT1220 families. Both voltage and current feedback types can be used. Pins 1, 5, and 8 are outfitted with pads for use in adjusting DC offsets, compensation or, in the case of the LT1223 and LT1190/1/2, for shutting down the amplifier.

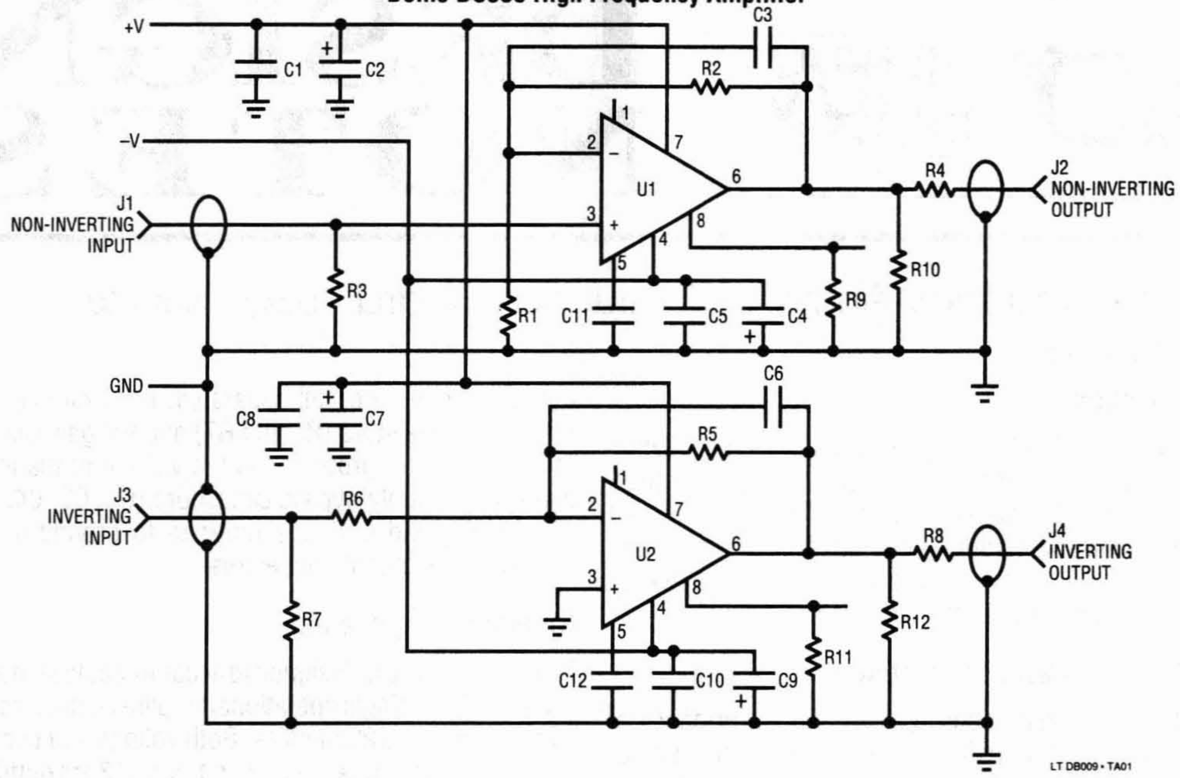
If a current feedback amplifier such as the LT1223 is being evaluated, omit C3/C6. R4 and R8 are included for impedance matching when driving low impedance lines. If the amplifier is supposed to drive the line directly, or if the load impedance is high, R4 and R8 can be replaced by jumpers. Similarly R10 and R12 can be used to establish a load at the output of the amplifier.

Low profile sockets may be used for the op amps to facilitate changing parts, but performance may be affected above 100MHz.

Supply Bypass Capacitors

High speed operational amplifiers work best when their supply pins are bypassed with RF-quality capacitors. C1, C5, C8, and C10 should be 10nF disc ceramics with a self-resonant frequency greater than 10MHz. The polarized capacitors (C2, C4, C7, and C9) should be 1μF to 10μF tantalums. Most 10nF ceramics are self-resonant well above 10MHz, and 4.7μF solid tantalums (axial leaded) are self-resonant at 1MHz or below. Lead lengths are critical: the self-resonant frequency of a 4.7μF tantalum drops by a factor of 2 when measured through 2 inch leads. Although a capacitor may become inductive at high frequencies, it is still an effective bypass component above resonance because the impedance is low.

Demo DC009 High Frequency Amplifier



+V
C1
C2
C3
R2
–V
J1
NON-INVERTING
INPUT
R3
R1
C11
C5
C4
R9
R10
U1
R4
J2
NON-INVERTING
OUTPUT
GND
C8
C7
C6
R5
J3
INVERTING
INPUT
R6
R7
U2
C12
C10
C9
R11
R12
R8
J4
INVERTING
OUTPUT
LT DB009 • TA01

Demo Board DC009 Parts List

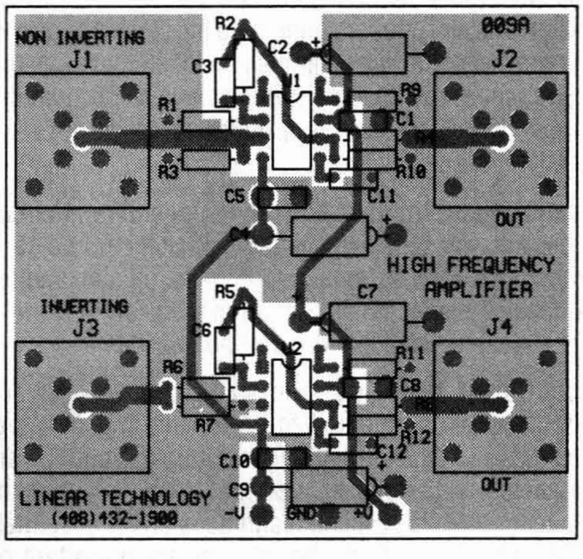
Non-inverting Amplifier:

R1	Gain Setting Resistor
R2	Feedback Resistor
R3	Input Line Termination (51Ω)
R4	Output Line Termination (51Ω)
R9	Shutdown Pin Pull Down
R10	Output Load Resistor
C1	Positive Supply High Frequency Bypass (10nF)
C2	Positive Supply Low Frequency Bypass (4.7µF)
C3	Feedback Capacitor
C4	Negative Supply Low Frequency Bypass (4.7µF)
C5	Negative Supply High Frequency Bypass (10nF)
C11	Compensation Capacitor
J1	Input Connector (AMP 227699-3)
J2	Output Connector (AMP 227699-3)

Inverting Amplifier:

R5	Feedback Resistor
R6	Gain Setting Resistor
R7	Input Line Termination (51Ω)
R8	Output Line Termination (51Ω)
R11	Shutdown Pin Pull Down
R12	Output Load Resistor
C6	Feedback Capacitor
C7	Positive Supply Low Frequency Bypass (4.7µF)
C8	Positive Supply High Frequency Bypass (10nF)
C9	Negative Supply Low Frequency Bypass (4.7µF)
C10	Negative Supply High Frequency Bypass (10nF)
C12	Compensation Capacitor
J3	Input Connector (AMP 227699-3)
J4	Output Connector (AMP 227699-3)

High Frequency Amplifier, Demo 009A Component Side



NON INVERTING
J1
R2
C2
009A
J2
C3
R1
R9
C1
R3
R10
C5
C11
C4
OUT
HIGH FREQUENCY
AMPLIFIER
R5
C7
INVERTING
J3
C6
J4
R11
R6
C8
R7
R12
C12
C10
LINEAR TECHNOLOGY
(408)432-1900
C9
–V
GND
+V
OUT

For literature on our High Speed Amplifiers, call **(800) 637-5545**. For applications help, call (408) 432-1900, Ext. 456.

LINEAR TECHNOLOGY
DESIGN NOTES

Gain Trimming In Instrumentation Amplifier Based Systems – Design Note 51

Jim Williams

Gain trimming is almost always required in instrumentation amplifier based systems. Gain uncertainties, most notable in transducers, necessitate such a trim.

Figure 1, a conceptual system, shows several points as candidates for the trim. In practice, only one of these must actually be used. The appropriate trim location varies with the individual application.

Figure 2 approaches gain trimming by altering transducer excitation. The gain trim adjustment results in changes in the LT1010's output. The LT1027 reference and LT1097 ensure output stability. Transducer output varies with excitation, making this a viable approach. It is important to consider that gain "lost" by reducing transducer drive translates into reduced signal-to-noise ratio. As such, gain reduction by this method is usually limited to small trims, e.g. 5-10%. Similarly, too much gain introduced by this method can cause excessive transducer drive, degrading accuracy. The transducer manufacturer's data sheet should list the maximum permissible drive for rated accuracy.

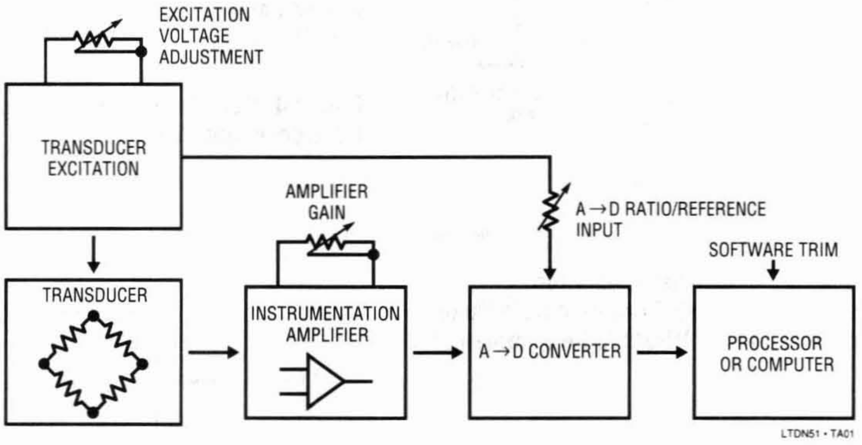

EXCITATION VOLTAGE ADJUSTMENT
TRANSDUCER EXCITATION
AMPLIFIER GAIN
A→D RATIO/REFERENCE INPUT
SOFTWARE TRIM
TRANSDUCER
INSTRUMENTATION AMPLIFIER
A→D CONVERTER
PROCESSOR OR COMPUTER
LTDN51 • TA01

Figure 1. Conceptual Transducer Signal Conditioning Path Showing Gain Trimming Possibilities. In Practice, Only One Adjustment Is Required.

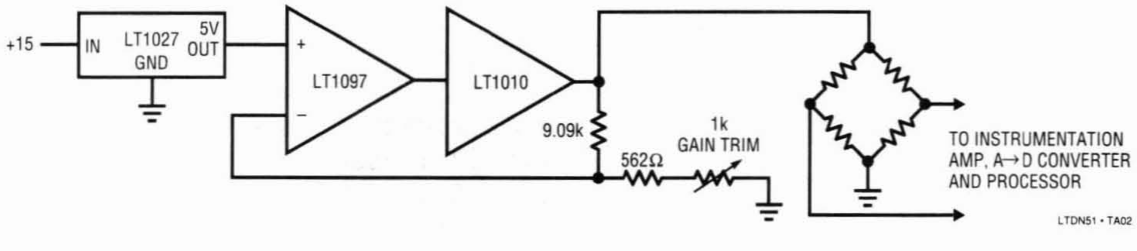

+15
IN
LT1027
GND
5V OUT
+
–
LT1097
LT1010
9.09k
562Ω
1k GAIN TRIM
TO INSTRUMENTATION AMP, A→D CONVERTER AND PROCESSOR
LTDN51 • TA02

Figure 2. Gain Trimming by Adjustment of Transducer Excitation. This Method is Useable for Small (5-10%) Trims. Large Trims Will Cause Excessive Transducer Power Dissipation or "Starved" Outputs.

Figure 3 adjusts gain in the instrumentation amplifier stage. The fixed gain LT1101 instrumentation amplifier feeds a second amplifier where the trim occurs. As both cases show, the gain trim may be up or down. A secondary benefit of this trim scheme is that it permits optional offset summing and filtering. Note that either the inverter or follower may be set up for gain addition or reduction. The sole limitation is the signal polarity reversal imposed by the inverter case. This may be corrected by reversing the instrumentation amplifiers' inputs.

A final hardware based gain trim is shown in Figure 4. Here, the A→D reference input is scaled to the appropriate voltage by the op amp and associated components. The op amp input is usually the transducer excitation voltage or, in cases where this is not possible, a reference.

One final way to trim gain is in software. If a processor is involved in the system this is a viable alternative. The software trim does a simple code conversion on the A→D output. When using this approach utilize as much of the analog components' dynamic range as possible to avoid signal-to-noise degradation.

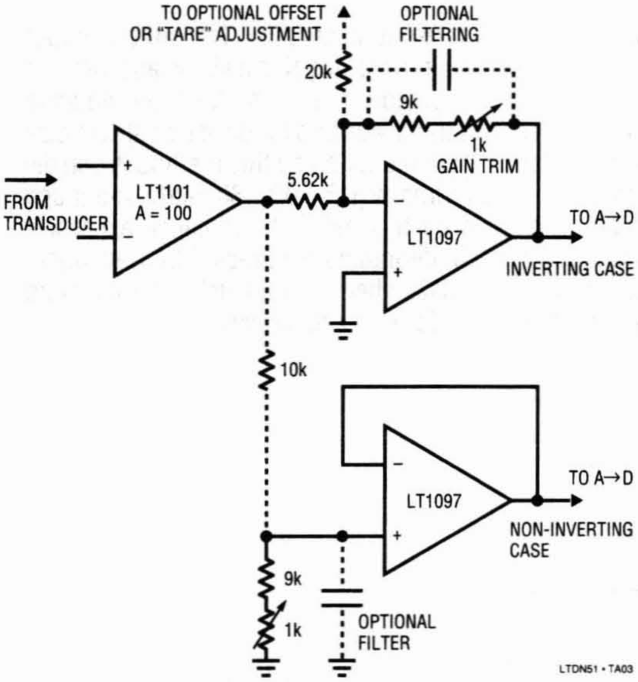

TO OPTIONAL OFFSET OR "TARE" ADJUSTMENT
OPTIONAL FILTERING
20k
9k
1k GAIN TRIM
FROM TRANSDUCER
LT1101 A = 100
5.62k
LT1097
TO A→D
INVERTING CASE
10k
LT1097
TO A→D
NON-INVERTING CASE
9k
1k
OPTIONAL FILTER
LTDN51 • TA03

Figure 3. Gain Trimming at the Instrumentation Amplifier. A Second Stage Permits Trimming Gain Up or Down, and Allows Filtering and Offsets to Be Summed In.

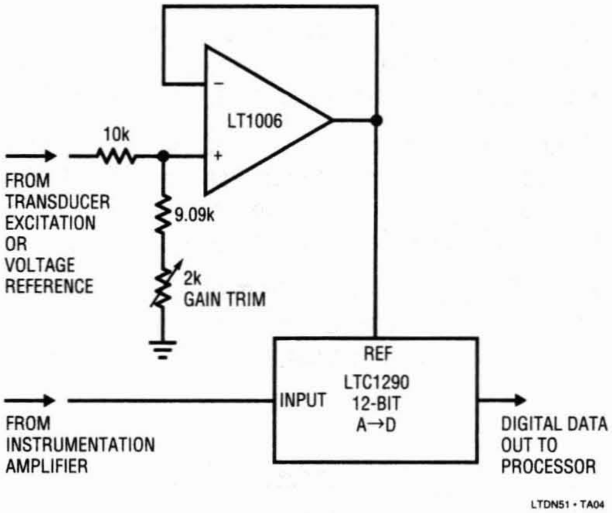

LT1006
10k
FROM TRANSDUCER EXCITATION OR VOLTAGE REFERENCE
9.09k
2k GAIN TRIM
REF
LTC1290 12-BIT A→D
INPUT
FROM INSTRUMENTATION AMPLIFIER
DIGITAL DATA OUT TO PROCESSOR
LTDN51 • TA04

Figure 4. Gain Trimming By Adjustment of the A→D Reference Input Voltage

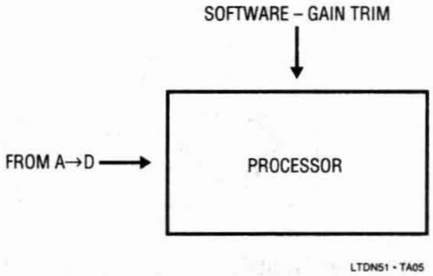

SOFTWARE – GAIN TRIM
FROM A→D
PROCESSOR
LTDN51 • TA05

Figure 5. Software Based Trimming

For literature on our Instrumentation Amplifiers, call **(800) 637-5545**. For applications help, call (408) 432-1900, Ext. 456.

DESIGN NOTES

DC-DC Converters for Portable Computers – Design Note 52

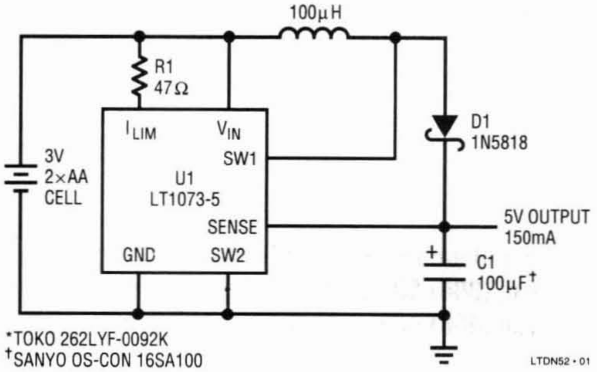
Steve Pietkiewicz
Jim Williams

Portable computers require simple and efficient converters for +5V power and display driving. A regulated 5V supply can be generated from two "AA" cells using the circuit shown in Figure 1. U1, an LT1073-5 micropower DC-DC converter, is arranged as a step-up, or "boost" converter. The 5V output, monitored by U1's SENSE pin, is internally divided down and compared to a 212mV reference voltage inside the device. U1's oscillator turns on when the output drops below 5V, cycling the switch on and off at a 19kHz rate. This action alternately causes current to build up in L1, then dump into C1 through D1, increasing the output voltage. When the output reaches 5V, the oscillator turns off. The gated oscillator provides the mechanism to keep the output at a constant 5V. R1 invokes the current limit feature of the LT1073, limiting peak switch current to 1A. U1 limits switch current by turning off the switch when the current reaches the programmed limit set by R1. Switch "on" time, therefore, decreases as V_{IN} is increased. Switch "off" time is not affected. This scheme keeps peak switch current constant over the entire input voltage range, allowing maximum energy transfer to occur at low battery voltage without exceeding L1's maximum current rating at high battery voltage.

The circuit delivers 5V at 150mA from an input range of 3.5V to 2.0V. Efficiency measures 80% at 3.0V, decreasing to 70% at 2.0V for load currents in the 15mA to 150mA range. Output ripple measures 170mVp-p and no-load quiescent current is just 135µA.

A −24V LCD bias generator is shown in Figure 2. In this circuit U1 is an LT1173 micropower DC-DC converter. The 3V input is converted to +24V by U1's switch, L1, D1, and C1. The switch pin (SW1) then drives a charge pump composed of C2, C3, D2, and D3 to generate −24V. Line regulation is less than 0.2% from 3.3V to 2.0V inputs. Load regulation, although it suffers somewhat since the −24V output is not directly regulated, measures 2% from a 1mA to 7mA load. The circuit will deliver 7mA from a 2.0V input at 73% efficiency.

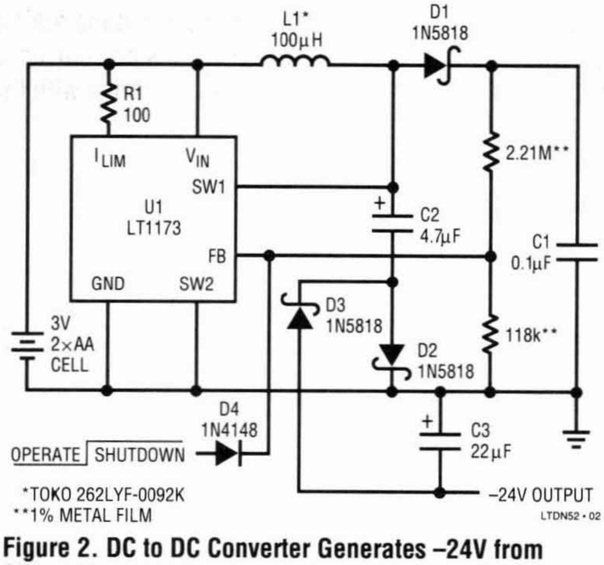
If greater output power is required, Figure 2's circuit can be driven from a +5V source. R1 should be changed to



L1*
100µH
R1
47Ω
I_LIM
V_IN
SW1
U1
LT1073-5
SENSE
GND
SW2
3V
2×AA
CELL
D1
1N5818
5V OUTPUT
150mA
C1
100µF†
LTDN52 • 01

*TOKO 262LYF-0092K
†SANYO OS-CON 16SA100

Figure 1. Two "AA" Cell to 5V Step-Up Converter Delivers 150mA



L1*
100µH
D1
1N5818
R1
100
I_LIM
V_IN
SW1
U1
LT1173
FB
GND
SW2
2.21M**
C2
4.7µF
C1
0.1µF
D3
1N5818
118k**
D2
1N5818
3V
2×AA
CELL
D4
1N4148
OPERATE | SHUTDOWN
C3
22µF
−24V OUTPUT
LTDN52 • 02

*TOKO 262LYF-0092K
**1% METAL FILM

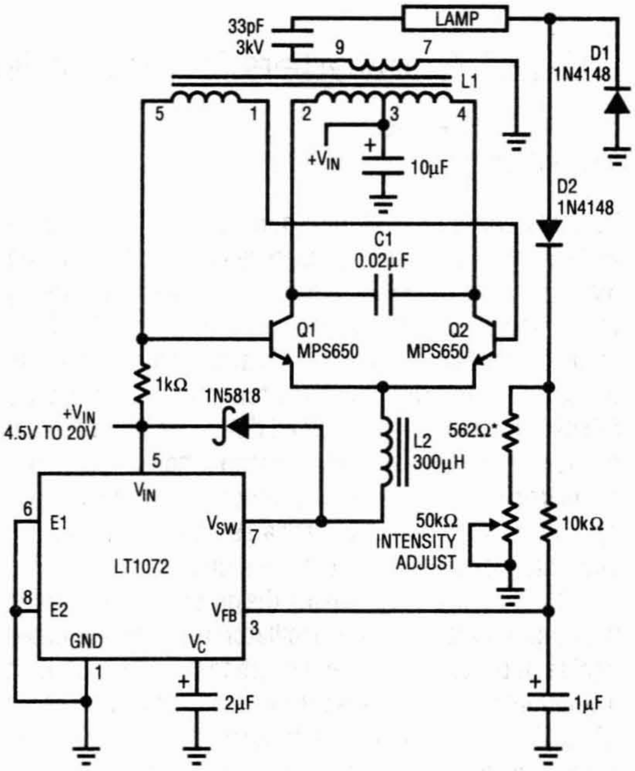
Figure 2. DC to DC Converter Generates −24V from 3V or 5V

47Ω and C3 to 47μF. With a 5V input, 40mA is available at 75% efficiency. Shutdown is accomplished by bringing the anode of D4 to a logic high, forcing the feedback pin of U1 to go above the internal reference voltage of 1.25V. Shutdown current is 110μA from the input source and 36μA from the shutdown signal.

Current generation portables require back lit LCD displays using cold cathode fluorescent lamps (CCFLs). Figure 3 provides 78% efficiency with full control over lamp brightness. 82% efficiency is possible if the LT1072 is driven from a low voltage (e.g. 3V-5V) source. Additional benefits include a 4.5V to 20V supply range and low radiated power due to sine wave based operation.

L1 and the transistors comprise a current driven Royer class converter which oscillates at a frequency primarily set by L1's characteristics and the 0.02μF capacitor. LT1072 driven L2 sets the magnitude of the Q1-Q2 tail current, and hence L1's drive level. The 1N5818 diode maintains current flow when the LT1072 is off.

The 0.02μF capacitor combines wth L1's characteristics to produce sine wave voltage drive at the Q1 and Q2 collectors. L1 furnishes voltage step-up, and about 1400Vp-p appears at its secondary. Current flows through the 33pF capacitor into the lamp. On negative waveform cycles the lamp's current is steered to ground via D1. Positive waveform cycles are directed, via D2, to the ground referred 562Ω-50k potentiometer chain. The positive half-sine appearing across these resistors represents 1/2 the lamp current. This signal is filtered by the 10k-1μF pair and presented to the LT1072's feedback pin. This connection closes a control loop which regulates lamp current. The 2μF capacitor at the LT1072's V_C pin provides stable loop compensation. The loop forces the LT1072 to switch-mode modulate L2's average current to whatever value is required to maintain a constant current in the lamp. The constant current's value, and hence lamp intensity, may be varied with the potentiometer. The constant current drive allows full 0-100% intensity control with no lamp dead zones or "pop-on" at low intensities. Additionally, lamp life is enhanced because current cannot increase as the lamp ages. Detailed information on this circuit appears in LTC Application Note 45, "Measurement and Control Circuit Collection."



C1 = MUST BE A LOW LOSS CAPACITOR.
METALIZED POLYCARB
WIMA FPK 2 (GERMAN) RECOMMENDED.
L1 = SUMIDA 6345-020 OR COILTRONIX CTX110092-1.
PIN NUMBERS SHOWN FOR COILTRONIX UNIT
L2 = COILTRONIX CTX300-4
* = 1% FILM RESISTOR
DO NOT SUBSTITUTE COMPONENTS

LTDN52 • 03

Figure 3. Cold Cathode Fluorescent Lamp Power Supply

For literature on our DC-DC Converters, call **(800) 637-5545**. For applications help, call (408) 432-1900, Ext. 456

High Performance Frequency Compensation Gives DC-to-DC Converter 75µs Response With High Stability — Design Note 53

Ron Vinsant

This Design Note describes four high performance, low cost, 1.75A step-down converter circuits based on the LT1076 five terminal switching regulator. All four circuits have exceptional transient response; indeed, it is superior to most three terminal linear regulators. Transient response is important to loads that are switched on and off or that require high peak currents. Examples are digital circuits that are turned on and off, disk drive motors, stepper motors and linear amplifiers. The frequency compensation schemes shown in this Design Note, when compared to the usual R and C technique, allow greater variation in output capacitor ESR without causing stability problems. This is important in applications where wide temperature variations occur (which changes capacitor ESR) such as industrial control, automotive and military, and when the use of multiple capacitor vendors with different capacitor specifications is required.

Phase margin is always more than 50° and gain margin is a minimum of 18dB. Bode plots are available from the factory upon request.

The efficiency of these circuits is typically 80% with output ripple less than 50mV. Input voltages can be as high as 45V. Input ripple rejection is an exceptional 60dB due to the feedforward architecture of the LT1076. These circuits use a small number of external parts that are available off-the-shelf.

Many of the problems associated with five terminal switching regulators have been addressed by these circuits. Start-up overshoot is less than 5% with the optional soft start circuit. On recovery from a short circuit, a 10% overshoot is realized.

For a 15V output, line regulation is typically 0.06% (10mV) for a 20V to 40V input voltage change. Load regulation is difficult to measure; in fact, it is only 1mV to 2mV at the point of regulation. This applies to all output voltages.

Each circuit has been built in our lab and evaluated for stability, temperature, component life and tolerance. Two circuit options are shown: a simple soft start circuit and an output voltage adjustment (see Figure 1).

Inductors

The inductors shown in Table 3 are designed around two different core materials. The first is powered iron based for low cost. The second is tape wound steel for smaller size and higher efficiency but greater cost. For rapid evaluation of these circuits, powered iron cores are available in sample quantities from Micrometals at 1-800-356-5977. Completed inductors are available from Coiltronics at 305-781-8900.

Capacitors

Ripple current in the output capacitor is 150mA maximum with the input voltage at 40V and maximum load. At 35°C ambient estimated life-time with the specified capacitor and full load is 28 years.

The input capacitor, which undergoes higher stress, has a ripple current of 830mA maximum at 14V input and maximum load. The life-time of this capacitor is 14 years at 35°C. If the ambient temperature is higher, the life of the capacitor will be cut in half for every 10°C increase. The ESR specification affects the output ripple as well as frequency compensation. Its value of capacitance is not critical.

The capacitors in the frequency compensation network should be at least X7R ceramic, never Z5U, and, if broad temperature operation is expected, polyester or polycarbonate film caps should be used.

Manufacturing technologies must also be taken into account. If an IR furnace is used for soldering, use only ceramic capacitors. A wave or hand soldering operation is suggested for both film and electrolytic capacitors.

This is an area of continuing development so be sure to contact the capacitor manufacturers for temperature profiles.

Layout

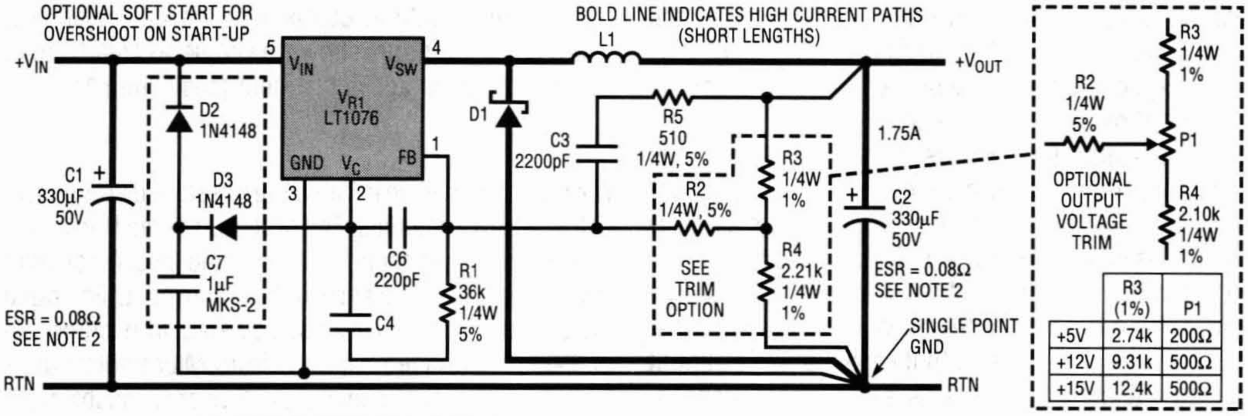
In order to achieve proper performance it is important to lay out the circuit as the schematic indicates. Use a single point ground at the output of the converter as shown. The term "short" indicates that the trace should be as short as possible between the two points shown. These traces should have a minimum width of 0.2 inches in 2oz. copper for a length of less than 1.5 inches. Traces longer than this should be avoided on the heavily shaded portions of the schematic.

Output Adjustment

A potentiometer can be added to the output divider string, provided the string does not change its overall resistance value. A table showing resistance values is shown with the schematic.

Heatsinking

Any heatsink of 30°C/W (~2 square inches) or lower will keep the LT1076 at an acceptable temperature up to a 70°C ambient. See LT1076 data sheet for further information.



OPTIONAL SOFT START FOR OVERSHOOT ON START-UP
+V_IN
5
V_IN
V_SW
4
V_R1
LT1076
GND
V_C
FB
1
3
2
D2
1N4148
D3
1N4148
C1 +
330µF
50V
C7
1µF
MKS-2
ESR = 0.08Ω
SEE NOTE 2
C6
220pF
C4
R1
36k
1/4W
5%
D1
C3
2200pF
BOLD LINE INDICATES HIGH CURRENT PATHS (SHORT LENGTHS)
L1
R5
510
1/4W, 5%
R2
1/4W, 5%
SEE TRIM OPTION
R3
1/4W
1%
R4
2.21k
1/4W
1%
1.75A
+V_OUT
C2
330µF
50V
ESR = 0.08Ω
SEE NOTE 2
SINGLE POINT GND
RTN
RTN
R3
1/4W
1%
R2
1/4W
5%
P1
OPTIONAL OUTPUT VOLTAGE TRIM
R4
2.10k
1/4W
1%
DN53 • TA01

	R3 (1%)	P1
+5V	2.74k	200Ω
+12V	9.31k	500Ω
+15V	12.4k	500Ω

NOTE 1: DO NOT SUBSITTUTE COMPONENTS WITHOUT COMPLETE EVALUATION.
NOTE 2: C1 AND C2 MUST BE 0.07Ω MIN ESR AT ROOM TEMPERATURE (25°C). UNITED CHEMICON SXE50VB331M10X30LL, SPRAGUE 672D337F020DM4D.
NOTE 3: ALL CAPS EXCEPT C1 AND C2 ARE WIMA FKC-2 OR X7R CERAMIC, ±10% TOLERANCE. WIMA 914-347-2474

Figure 1. High Performance DC-to-DC Converter

Table 1. Components

#	V_{IN}	V_{OUT}	e (%) @ V_{IN}	L (µH)	D1	R2 (5%)	R3 (1%)	C4 (10%)
1	8V-20V	+5V	83% @ 10	75	MBR330P	1.5k	2.80k	0.0068µF
2	8V-40V	+5V	76% @ 24	91	MBR350	1.5k	2.80k	0.0068µF
3	15V-40V	+12V	86% @ 24	180	MUR415	1.2k	9.79k	0.01µF
4	18V-40V	+15V	86% @ 24	240	MUR415	1.2k	12.7k	0.01µF

Table 2. Performance

#	V_{OUT}	MIN LOAD	REGULATION (MIN TO MAX) LOAD	LINE	RIPPLE REJECTION 50Hz-400Hz	OUTPUT RIPPLE
1	+5V	0.200	0.1%	15mV	60dB	50mV
2	+5V	0.175	0.1%	15mV	60dB	50mV
3	+12V	0.175	0.1%	15mV	60dB	50mV
4	+15V	0.175	0.1%	15mV	60dB	50mV

Note 1: V_{IN} = 24V except #1 at 14V.
Note 2: Temperature = 25°C.
Note 3: Periodic and random deviation (P.A.R.D.).
With optional adjustment = ±2.5%.
Without optional adjustment = ±4.5%.

Table 3. Inductor

L (µH)	NUMBER TURNS	CORE	COILTRONICS P/N	SMALLER TOROID
75	37 #18	T68-52A	CTX75-2-52	CTX75-2-KM
91	38 #18	T80-52B	CTX91-2-52	CTX91-2-KM
180	53 #18	T80-52B	CTX180-2-52	CTX180-2-KM
240	61 #18	T80-52B	CTX240-2-52	CTX240-2-KM

Note 1: ΔL with DC current is 20% max.

For literature on our Switching Regulators, call **(800) 637-5545**. For applications help, call (408) 432-1900, Ext. 456

DESIGN NOTES

A 4-Cell Ni-Cad Regulator/Charger for Notebook Computers – Design Note 54

Tim Skovmand

The new LTC1155 Dual Power MOSFET Driver delivers 12V of gate drive to two N-channel power MOSFETs when powered from a 5V supply with no external components required. This ability, coupled with its micropower current demands and protection features, makes it an excellent choice for high side switching applications which previously required more expensive P-channel MOSFETs.

A notebook computer power supply system is a good example of an application which benefits directly from this high side driving scheme. A four cell, Ni-Cad battery pack can be used to power a 5V notebook computer system. Inexpensive N-channel power MOSFETs have very low ON resistance and can be used to switch power with low voltage drop between the battery pack and the 5V logic circuits.

Figure 1 shows how a battery charger and an extremely low voltage drop 5V regulator can be built using the new LTC1155 and three inexpensive power MOSFETs.

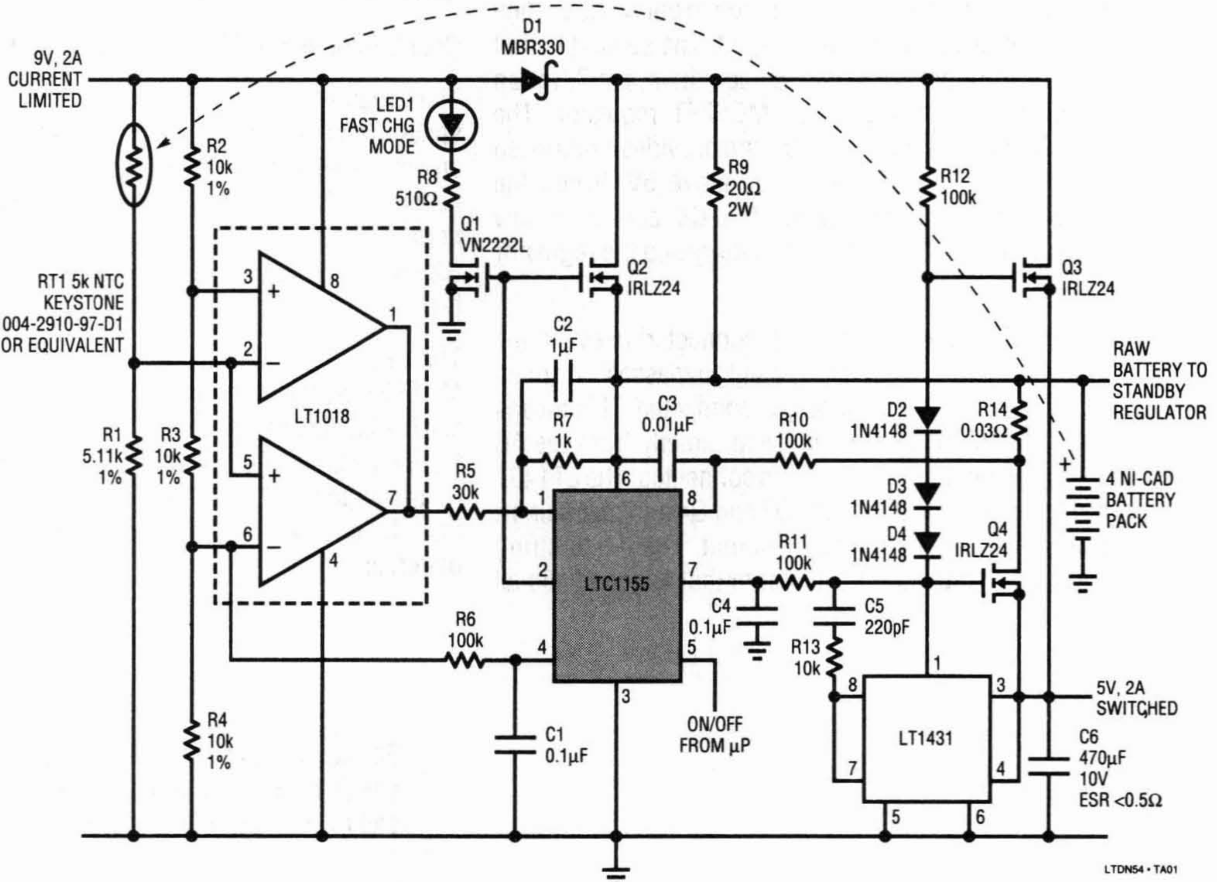

9V, 2A CURRENT LIMITED
D1 MBR330
LED1 FAST CHG MODE
R8 510Ω
R2 10k 1%
R9 20Ω 2W
R12 100k
Q1 VN2222L
Q2 IRLZ24
Q3 IRLZ24
RT1 5k NTC KEYSTONE RL1004-2910-97-D1 OR EQUIVALENT
LT1018
C2 1µF
RAW BATTERY TO STANDBY REGULATOR
R1 5.11k 1%
R3 10k 1%
R7 1k
C3 0.01µF
R10 100k
D2 1N4148
R14 0.03Ω
R5 30k
D3 1N4148
D4 1N4148
4 NI-CAD BATTERY PACK
Q4 IRLZ24
LTC1155
R11 100k
C4 0.1µF
C5 220pF
R6 100k
R13 10k
5V, 2A SWITCHED
R4 10k 1%
C1 0.1µF
ON/OFF FROM µP
LT1431
C6 470µF 10V ESR <0.5Ω
LTDN54 • TA01

Figure 1. The LTC1155 Dual MOSFET Driver Provides Gate Drive and Protection for a 4-Cell Ni-Cad Charger and Regulator

Quick Charge Battery Charger

One half of the LTC1155 Dual MOSFET Driver controls the charging of the battery pack. The 9V, 2A current limited wall unit is switched directly into the battery pack through an extremely low resistance MOSFET switch, Q2. The gate drive output, Pin 2, generates about 13V of gate drive to fully enhance Q1 and Q2. The voltage drop across Q2 is only 0.17V at 2A and, therefore, can be surface mounted to save board space.

An inexpensive thermistor, RT1, measures the battery temperature and latches the LTC1155 OFF when the temperature rises to 40°C by pulling low on pin 1, the Drain Sense Input. The window comparator also ensures that battery packs which are very cold (<10°C) are not quick charged.

Q1 drives an indicator lamp during quick charge to let the computer operator know that the battery pack is being charged properly. When the battery temperature rises to 40°C, the LTC1155 latches OFF and the battery charge current flowing through R9 drops to 150mA.

Extremely Low Voltage Drop Regulator

A four-cell Ni-Cad battery pack produces about 6V when fully charged. This voltage will drop to about 4.5V when the batteries are nearly discharged. The second half of the LTC1155 provides gate voltage drive, pin 7, for an extremely low voltage drop MOSFET regulator. The LT1431 controls the gate of Q4 and provides a regulated 5V output when the battery is above 5V. When the battery voltage drops below 5V, Q4 acts as a low resistance switch between the battery and the regulator output.

A second power MOSFET, Q3, connected between the 9V supply and the regulator output "bypasses" the main regulator when the 9V supply is connected. This means that the computer power is taken directly from the AC line while the charger wall unit is connected. The LT1431 provides regulation for both Q3 and Q4 and maintains a constant 5V at the regulator output. The diode string made up of diodes D2-D4 ensure that Q3 conducts all the regulator current when the wall unit is plugged in by separating the two gate voltages by about 2V.

R14 acts as a current sense for the regulator. The regulator latches OFF at 3A when the voltage drop between the second Drain Sense Input, pin 8, and the supply, pin 6, rises above 100mV. R10 and C3 provide a short delay. The μP can restart the regulator by turning the second input, pin 5, OFF and then back ON.

The regulator is switched OFF by the μP when the battery voltage drops below 4.6V. The standby current for the 5V, 2A regulator is less than 10μA. The regulator is switched ON again when the battery voltage rises during charging.

Very Low Power Dissipation

The power dissipation in the notebook computer is very low. The current limited wall unit dissipates the bulk of the power created by quick charging the battery pack. Q2 dissipates less than 0.5W. R9 dissipates about 0.7W. Q4 dissipates about 2W for a very short period of time when the batteries are fully charged and dissipates less than 0.5W as soon as the battery voltage drops to 5V. The three integrated circuits shown are micropower and dissipate virtually no power.

Cost Effective and Efficient Power System

The circuit shown in Figure 1 consumes very little board space. The LTC1155 is available in a 8-pin SO package and the three power MOSFETs can also be housed in SO packaging. Q4 must be heatsinked properly for the short period of time that the battery voltage is above 5.5V. (Consult the MOSFET manufacturer data sheet for SO heatsink recommendations).

The LTC1155 allows the use of inexpensive N-channel MOSFET switches to directly connect power from a 4-cell Ni-Cad battery pack to the charger and the load. This technique is very cost effective and is also very efficient. Nearly all the battery power is delivered directly to the load to ensure maximum operating time from the batteries.

For literature on our MOSFET Drivers,
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call (408) 432-1900, Ext. 361

LINEAR TECHNOLOGY

DESIGN NOTES

New Low Cost Differential Input Video Amplifiers Simplify Designs and Improve Performance – Design Note 55

John Wright

The LT1190 is a family of high speed amplifiers optimized for video performance on ±5V or single +5V supplies. The family includes three voltage feedback op amps and two video difference amplifiers. All amplifiers slew at 450V/µs, and deliver ±50mA output current for driving cables. The LT1193 video difference amplifier features uncommitted high input impedance (+) and (–) inputs, and can be used in differential or single-ended configurations. In addition, the LT1193 has an adjustable gain of two or greater, with a –3dB bandwidth of 80MHz.

Wideband Voltage Controlled Amplifier

The LT1193 video difference amplifier combined with an MC1496 balanced modulator make a low cost 50MHz Voltage Controlled Amplifier (VCA), shown in Figure 1. The input signal of the MC1496 at pin 1 is multiplied by the Control Voltage on pin 10, and appears as a differential output current at pins 6 and 12. The LT1193 acts to level shift the differential signal and convert it to a single-ended output. Resistor R_B is used to set the bias current in the MC1496 to 1mA in each 200Ω R_L, while R_{CM} is used to shift the differential output into the common mode range of the LT1193. Resistors R1 through R4 bias the MC1496 inputs so that the Control Voltage V_C can be referenced to 0V. Positive V_C causes positive gain; negative V_C gives a phase inversion ($-A_V$), while 0V on V_C gives maximum attenuation (within the V_{OS} of the MC1496 control inputs). The value of R_e is chosen by knowing the maximum input signal:

$$R_e = (V_{IN}\ \text{max})/1\text{mA}$$

For the example shown the maximum input signal is 100mV peak, therefore, $R_e = 100\Omega$. At this maximum input signal there is significant distortion from the r_e modulation of the input pair. Linearity can be improved by increasing R_e at the expense of gain. The maximum voltage gain of the VCA is:

$$\frac{V_O}{V_i} = \left(A_V \text{ of LT1193}\right)\left(\frac{2R_L}{R_e + 2r_e}\right)$$

$$V_O/V_{IN} = 2(2\times200)/(100+52) = 5.26 = 14.42\text{dB}$$

Figures 2 and 3, show the frequency response and harmonic distortion of the VCA.

The voltage gain of the VCA can be increased at the expense of bandwidth by changing the value of load

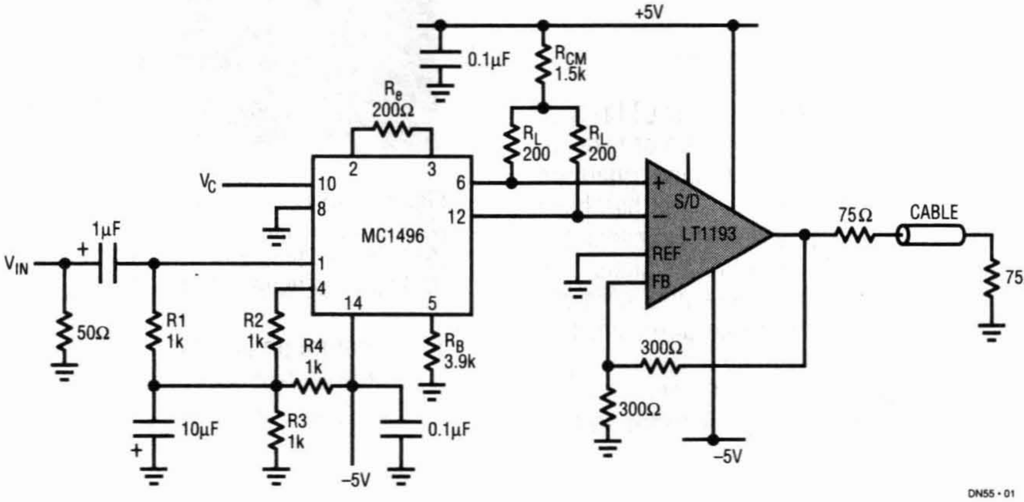


Figure 1. Low Cost 50MHz Voltage Controlled Amplifier

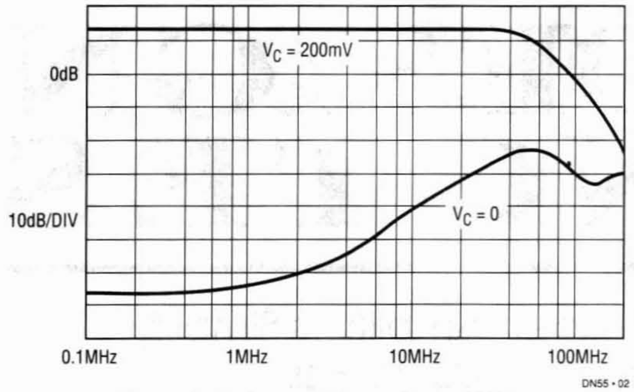


Figure 2. Gain and Attenuation of VCA

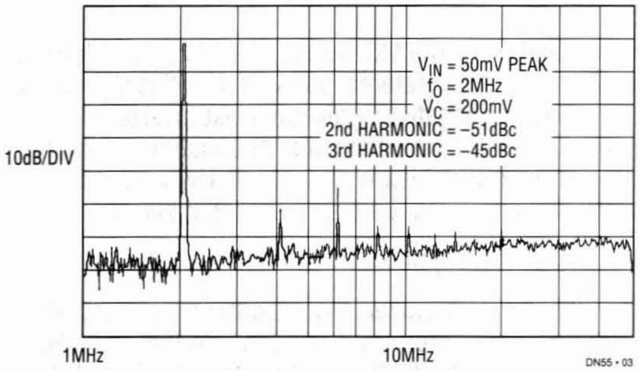


Figure 3. VCA Output Spectrum

resistors R_L. Shorting R_{CM} and increasing R_L to 2k will increase the maximum gain by 20dB and the –3dB bandwidth will drop to approximately 10MHz.

The LT1193 has a shutdown feature that reduces its power dissipation to only 15mW and forces a three-state output. The three-state output occurs when pin 5 is taken to V^-. The high Z state, dominated by the impedance of the feedback network, is useful for multiplexing several amplifiers on the same cable. The impedance of the feedback resistors should not be raised above 1kΩ because stray capacitance on the (–) input can cause instability.

Extending the Input Range on the LT1193

Figure 4 shows a simplified schematic of the LT1193. In normal operation the REF pin 1 is grounded or taken to a DC offset control voltage, while differential signals are applied between pins 2 and 3. The LT1193 has been optimized for gains of 2 or greater, and this means the input stage must handle fairly large input signals. The maximum input signal occurs when the input differential amplifier is tilted over hard in one direction, and 1.2mA flows through the 1kΩ R_e. The maximum input swing is therefore 1.2Vp or 2.4Vp-p. The second differential pair is running at slightly larger current so that when the first input stage limits, the second stage remains biased to maintain the feedback.

Occasionally it is necessary to handle signals larger than 2.4Vp-p at the input. The LT1193 input stage can be tricked to handle up to 4.8Vp-p. To do this, it is necessary to ground pin 3 and apply the differential input signal between pin 1 and 2. The input signal is now applied across two 1k resistors in series. Since the input signal is applied to both input pairs, the first pair will run out of bias current before the second pair, causing the amplifier to go open loop. This effect is shown in Figure 5 for the amplifier operating in a closed loop gain of 1. The LT1193 has a unity gain phase margin of only 40 degrees, so when operating at unity gain, care must be taken to avoid instability.

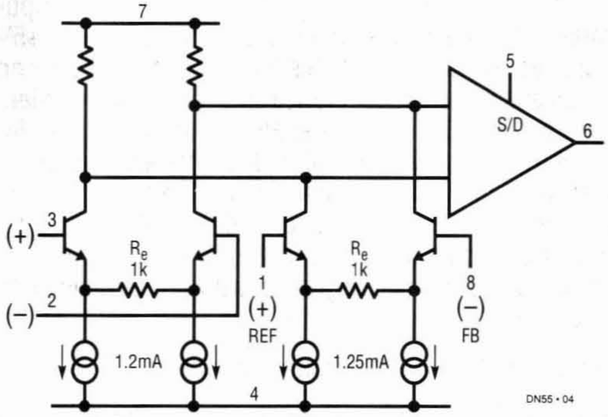


Figure 4. LT1193 Simplified Schematic

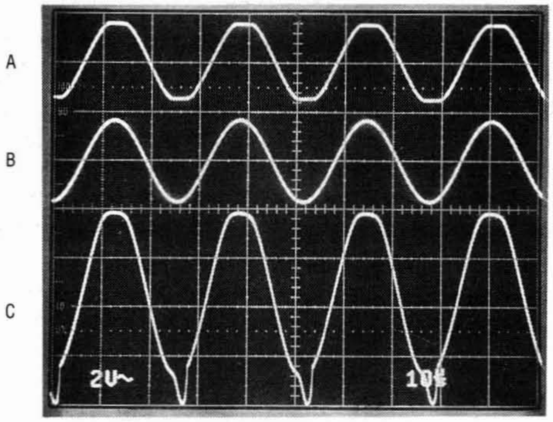


Figure 5. LT1193 in Unity Gain
(A) Standard Inputs, Pins 2 to 3, V_{IN} = 3.6Vp-p
(B) Extended Inputs, Pins 1 to 2, V_{IN} = 3.6Vp-p
(C) Extended Inputs, Pins 1 to 2, V_{IN} = 7.0Vp-p

For literature on our High Speed Amplifiers, call **(800) 637-5545**. For applications help, call (408) 432-1900, Ext. 361

LINEAR TECHNOLOGY
DESIGN NOTES

3V Operation of Linear Technology Op Amps – Design Note 56

George Erdi

The latest trend in digital electronics is the introduction of numerous IC's operating on regulated 3V or 3.3V power supplies. This is a logical development to increase circuit densities and to reduce power dissipation. In addition, many systems are directly powered by two AA cells or 3V Lithium batteries. Clearly, analog IC's which work on 3V with good dynamic range to complement these digital circuits are, and will be, in great demand.

Many Linear Technology operational amplifiers work well on a 3V supply. The purpose of this design note is to list these devices and their performance when powered by 3V. The op amps can be divided into two groups: single and dual supply devices. The single supply op amps are optimized for, and fully specified at, a 5V positive supply with the negative supply terminal tied to ground. Input common mode voltage range goes below ground, and the output swings to within a few millivolts of ground while sinking current. Members of the single supply family are the micropower LT1077/LT1078/LT1079 single, dual and quad op amps with 40µA supply current per amplifier, the LT1178/LT1179 dual and quad with 13µA per amplifier. The LT1006/LT1013/LT1014 single, dual and quad have faster speed and lower voltage noise, at the expense of 300µA per amplifier.

The performance of these devices at 3V is quite similar to the 5V specs. Clearly, input voltage range and output voltage swing have to be reduced by 2V since the supply is 2V less. Offset voltage change from 5V to 3V is determined by the power supply rejection ratio specs. At 114dB or 2µV/V the degradation in offset voltage is only 4µV (= 2V x 2µV/V). Input bias and offset currents, voltage and current noise, as well as offset voltage drift with temperature, are practically unchanged compared to the 5V specifications.

Table I summarizes the performance of the low cost grades of these single supply devices at 3V. One note of caution: the minimum operating voltage for the LT1013/LT1014 is 2.95V. All other devices work on lower supplies, ranging from 1.7V to 2.6V.

Table I. Single Supply Op Amps: Low Cost Grade Specifications V_S = 3V, 0V. T_A = 25°C.

		LT1077CN8 LT1078CN8 LT1079CN		LT1178CN8 LT1179CN		LT1006CN8 LT1013CN8 LT1014CN		
PARAMETER		**TYP**	**MIN/MAX**	**TYP**	**MIN/MAX**	**TYP**	**MIN/MAX**	**UNITS**
Offset Voltage	Single	15	80	—	—	35	95	µV
	Dual/Quad	45	140/170	45	140/170	95	470	µV
Input Voltage Range		−0.3	0	−0.3	0	−0.3	0	V
		+1.8	+1.7	+1.9	+1.7	+1.8	+1.7	V
Output Swing	No Load	0.003	0.006	0.006	0.009	0.015	0.025	V
		2.4	2.2	2.4	2.2	2.4	2.2	V
	2K to Ground	0.0006	0.0010	0.0002	0.0006	0.007	0.015	V
		2.1	1.9	2.0	1.8	2.3	2.0	V
Voltage Gain	R_L = 50K	500	110	180	60	1000	500	V/mV
0.1Hz to 10Hz Noise		0.6	—	1.0	—	0.5	—	µVp-p
Minimum Supply Voltage		—	2.3	—	2.2	—	2.6/2.95	V
With 300µV V_{OS} Degradation		—	1.8	—	1.7	—	—	V
Gain Bandwidth Product		160	—	50	—	700	—	KHz

The LT1101 micropower (= 75µA) instrumentation amplifier completes the single supply family. Again, this in amp in 8 pin packages is fully specified at 5V. Minimum supply voltage is 1.8V; the performance change in going from 5V to 3V supply is minimal.

The second group of devices are dual supply op amps, i.e., the common mode input voltage and the output swing are limited to a diode voltage (= 600mV) above the negative supply terminal for proper operation. In addition, dual supply op amps are traditionally optimized for ±15V operation. Thus, reducing the total supply voltage to 3V represents a significant change. Table II lists the performance of four op amps: the LT1008 and LT1012 are actually fully tested at reduced supplies. The LT1097 and LT1001 performance is inferred from device evaluation data. Dual versions in 14 pin packages are also available: the LT1002 is a dual LT1001; the LT1024 is a dual version of the LT1012.

In most 3V applications the single supply op amps of Table I are more flexible and desirable, since no special biasing is needed to shift the input and the output into the operating range. However, the offset voltage drift with temperature performance of the dual supply devices is better. And, most importantly, when pico-ampere input bias currents are needed, the LT1008/LT1012/LT1097 have no competition. The op amps of Table I are all at least 6nA. The traditional ways of achieving pico-ampere bias current are not available either: JFET input or CMOS chopper-stabilized op amps do not function at 3V supply.

Figure 1 shows an application using the LT1078 to monitor the condition of the 3V battery. One output warns that the battery voltage is dropping, the other output shuts the system down as the battery voltage falls below the threshold value.

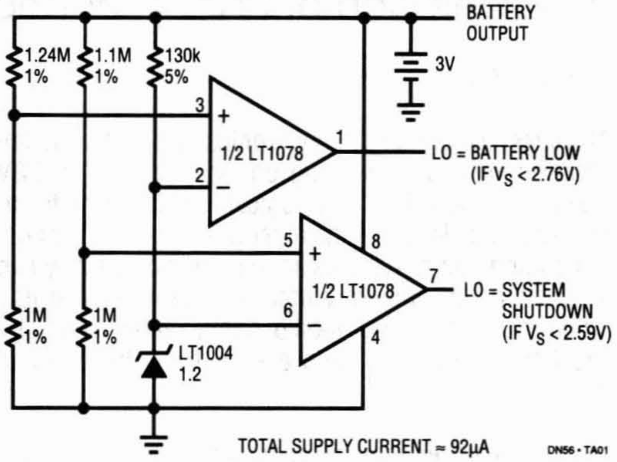

BATTERY OUTPUT
3V
1.24M 1%
1.1M 1%
130k 5%
3
+
2
−
1/2 LT1078
1
LO = BATTERY LOW (IF V_S < 2.76V)
5
+
6
−
8
1/2 LT1078
7
4
LO = SYSTEM SHUTDOWN (IF V_S < 2.59V)
1M 1%
1M 1%
LT1004 1.2
TOTAL SUPPLY CURRENT ≈ 92µA
DN56 • TA01

Figure 1. Low Battery Detector with System Shutdown

Table II. Dual Supply Op Amps at V_S = 3V, 0V. T_A = 25°C. Low Cost Grade Electrical Characteristics.

	LT1097CN8		LT1008CN8		LT1012CN8		LT1001CN8		
PARAMETER	**TYP**	**MIN/MAX**	**TYP**	**MIN/MAX**	**TYP**	**MIN/MAX**	**TYP**	**MIN/MAX**	**UNITS**
Offset Voltage	20	100	40	180	25	120	40	150	µV
Drift with Temperature	0.3	1.3	0.3	1.6	0.3	1.3	0.3	1.3	µV/°C
Input Bias Current	40	280	40	150	40	200	600	3500	pA
Input Offset Current	40	260	30	150	30	200	350	3200	pA
Input Voltage Range	0.65 2.3	0.80 2.2	0.65 2.3	0.80 2.2	0.65 2.3	0.80 2.2	0.75 2.2	0.90 2.1	V V
Output Swing	0.62 2.25	0.8 2.1	0.62 2.25	0.8 2.1	0.62 2.25	0.8 2.1	0.55 2.2	0.7 2.05	V V
Voltage Gain R_L = 10K	600	250	500	200	500	200	300	150	V/mV
0.1Hz to 10Hz Noise	0.5	—	0.5	—	0.5	—	0.35	—	µVp-p
Minimum Supply Voltage	—	2.4	—	2.4	—	2.4	—	1.9	V
Supply Current	350	560	380	600	380	600	390	550	µA
Gain Bandwidth Product	500	—	500	—	500	—	600	—	KHz

For literature on our Single Supply, Micropower, and Precision Op Amps, call **(800) 637-5545**.
For applications help, call (408) 432-1900, Ext. 361

LINEAR TECHNOLOGY

DESIGN NOTES

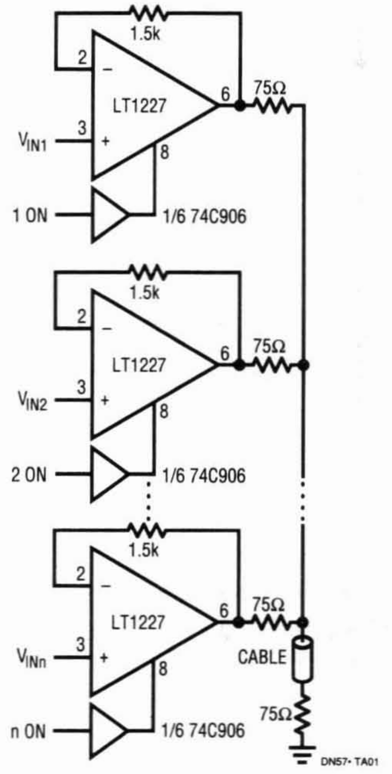
Video Circuits Collection – Design Note 57

William H. Gross

Introduction

This note shows how to make several different video circuits using high speed op amps. All of these circuits work with composite, RGB and monochrome video. For best results, bypass the power supply pins of these amplifiers with 1µF to 10µF tantalum capacitors in parallel with 0.01µF disc capacitors. It is important to terminate both ends of video cables to preserve frequency response. When properly terminated, the cable looks like a resistive load of 150Ω.

Lots of Inputs Video MUX Cable Driver (LT1227)

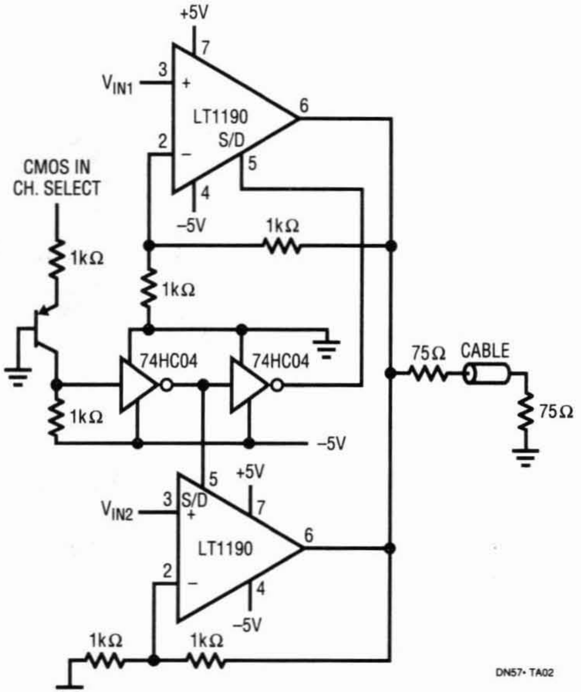

1.5k
2
–
LT1227
6
75Ω
V_{IN1}
3
+
8
1 ON
1/6 74C906
1.5k
2
–
LT1227
6
75Ω
V_{IN2}
3
+
8
2 ON
1/6 74C906
1.5k
2
–
LT1227
6
75Ω
V_{INn}
3
+
8
CABLE
n ON
1/6 74C906
75Ω
DN57 • TA01

Multiplex Amplifiers

Often it is desirable to select one of several signals to send down a cable. Connecting the outputs of several amplifiers together and using the amplifier's shutdown pin to disable all but one accomplishes this goal. The LT1190, LT1191, LT1192, and LT1193 are shutdown by pulling pin 5 to the negative supply.

The LT1223 and LT1227 current feedback amplifiers are shutdown by pulling pin 8 to ground. During normal operation pin 8 is open and at the positive supply potential. An easy way to interface pin 8 to logic is with a logic level N-Channel FET or a 74C906 (open drain hex buffer).

Two Input Video MUX Cable Driver (LT1190)


+5V
7
V_{IN1}
3
+
LT1190
S/D
6
2
–
5
4
CMOS IN
CH. SELECT
–5V
1kΩ
1kΩ
1kΩ
74HC04
74HC04
1kΩ
–5V
75Ω
CABLE
75Ω
5
+5V
V_{IN2}
3
S/D
+
7
LT1190
6
2
–
4
–5V
1kΩ
1kΩ
DN57 • TA02

Differential Gain and Phase of Several Amplifiers

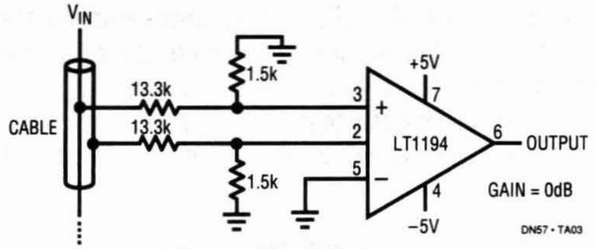
	DIFFERENTIAL			
	LOAD = 1kΩ		LOAD = 150Ω	
PART NO.	GAIN	PHASE	GAIN	PHASE
LT1190*	0.05	0.02	0.23	0.16
LT1191*	0.03	0.01	0.09	0.07
LT1192**	0.10	0.01	0.23	0.15
LT1193*	0.20	0.08	0.20	0.08
LT1194**	0.20	0.08	0.20	0.08
LT1223	0.01	0.02	0.12	0.26
LT1227	0.01	0.01	0.01	0.01
LT1228	0.01	0.01	0.04	0.10
LT1229	0.01	0.01	0.04	0.10

$V_S = \pm15V, A_V = 2$
* $V_S = \pm8V, A_V = 2$
** $V_S = \pm8V, A_V = 10$

Loop Through Cable Receivers

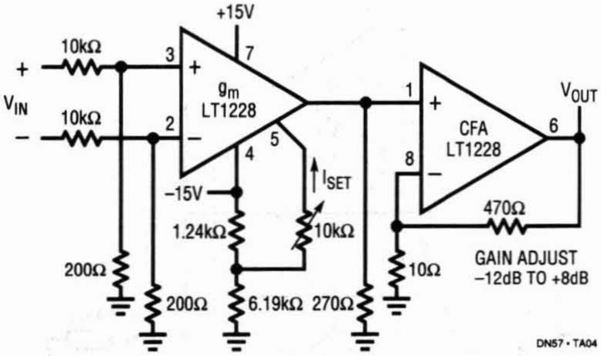
Most video instruments require high impedance differential input amplifiers that will not load the cable even when the power is off.

Differential Input Video Loop Through Amplifier Using a Video Difference Amplifier (LT1194)



V_{IN}
CABLE
13.3k
13.3k
1.5k
1.5k
+5V
LT1194
3
2
5
7
4
6
OUTPUT
GAIN = 0dB
−5V
DN57 • TA03

Electronically Controlled Gain, Video Loop Through Amplifier (LT1228)

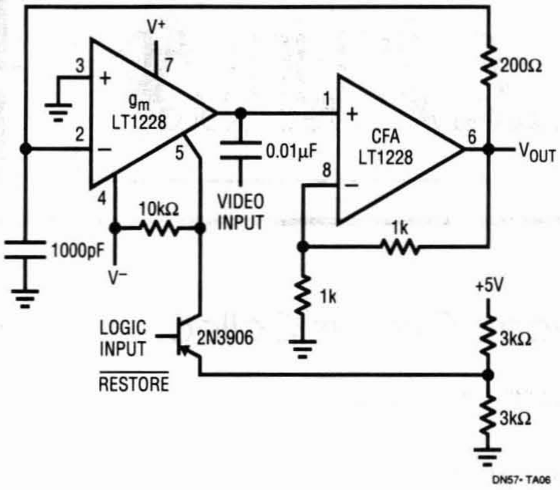


+15V
+
V_{IN}
−
10kΩ
10kΩ
g_m
LT1228
3
2
7
4
5
−15V
I_{SET}
1.24kΩ
10kΩ
200Ω
200Ω
6.19kΩ
270Ω
1
8
CFA
LT1228
6
V_{OUT}
470Ω
10Ω
GAIN ADJUST
−12dB TO +8dB
DN57 • TA04

DC Restore Circuits

The following circuit restores the black level of a monochrome composite video signal to 0V at the beginning of every horizontal line. This circuit is also used with CCD scanners to set the black level.

Video DC Restore (Clamp) Circuit (LT1228)

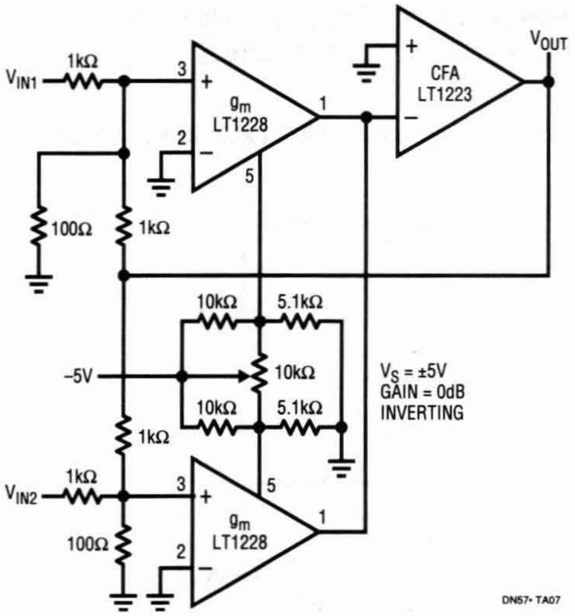


V+
3
2
7
g_m
LT1228
5
4
V−
1000pF
10kΩ
0.01µF
VIDEO
INPUT
1
8
CFA
LT1228
6
V_{OUT}
200Ω
1k
1k
+5V
3kΩ
3kΩ
LOGIC
INPUT
RESTORE
2N3906
DN57 • TA06

Fader Circuits

Using two LT1228 transconductance amplifiers in front of a current feedback amplifier forms a video fader. The ratio of the set currents into pin 5 determines the ratio of the inputs at the output.

Video Fader (LT1228, LT1223)



V_{IN1}
1kΩ
3
2
g_m
LT1228
5
1
100Ω
1kΩ
CFA
LT1223
V_{OUT}
10kΩ
5.1kΩ
−5V
10kΩ
10kΩ
5.1kΩ
1kΩ
V_S = ±5V
GAIN = 0dB
INVERTING
V_{IN2}
1kΩ
100Ω
3
2
5
g_m
LT1228
1
DN57 • TA07

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DESIGN NOTES

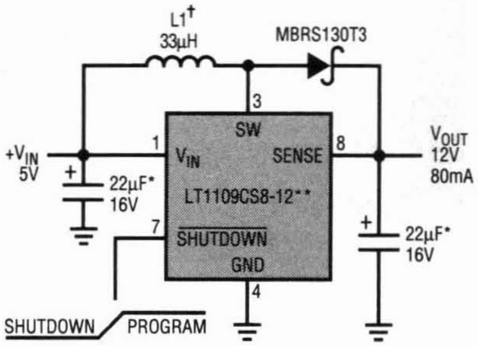
A Simple, Surface Mount Flash Memory Vpp Generator – Design Note 58

Steve Pietkiewicz
Jim Williams

"Flash" type memories add electrical chip-erasure and reprogramming to established EPROM technology. These features make them a cost effective and reliable alternative for updatable non-volatile memory. Utilizing the electrical program-erase capability requires linear circuitry techniques. Intel flash memory, built on the ETOX™ process, specifies programming operation with 12V amplitude pulses. These "Vpp" amplitudes must fall within tight tolerances, and excursions beyond 14.0V will damage the device.

Providing the Vpp pulse requires generating and controlling high voltages within the tightly specified limits. Figure 1's circuit does this. When the Vpp command pulse goes high (trace A, Figure 2) the LT1109 switching regulator drives L1, producing high voltage. DC feedback occurs via the regulator's sense pin. The result is a smoothly rising Vpp pulse (trace B) which settles to the required value. Trace C, a time and amplitude expanded version of trace B, details the desired settling to 12V. Artifacts of the switching regulator's action are discernible, although no overshoot or poor dynamics are displayed.

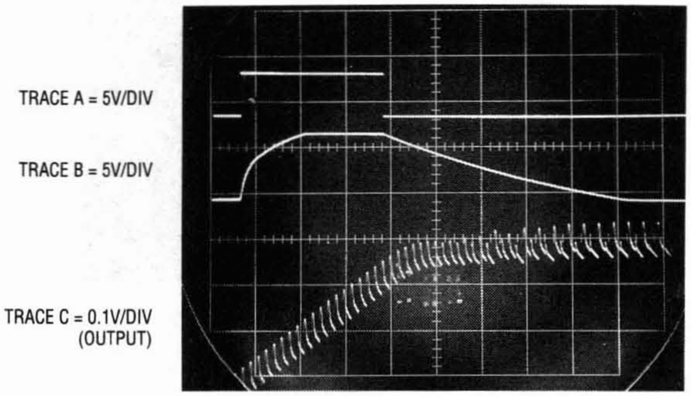
ETOX is a trademark of Intel Corporation.



† L1 = SUMIDA CD54-330N (708-956-0666)
* HILTON CSTDD226M016TC (813-371-2600)
** USE LT1109A FOR 120mA OUTPUT (CONSULT LTC FACTORY)

DN58 • TA02

Figure 1. All Surface Mount Flash Memory Vpp Generator



A & B HORIZ = 1 ms/DIV
C HORIZ = 50µs/DIV

DN58 • TA03

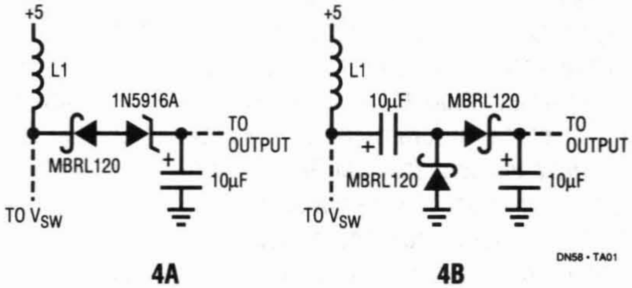
Figure 2. Waveforms for the Flash Memory Pulser Show No Overshoot

This circuit is well suited for providing Vpp power to flash memory. All associated components, including the inductor, are surface mount devices. As such, the complete circuit occupies very little space (see Figure 3). In the shutdown mode the circuit pulls only 300μA. Output voltage goes to V_{CC} minus a diode drop when the converter is in shutdown mode. This is an acceptable and specified condition for flash memories and does not harm the memory. A 0V output is possible by placing a 5.6V Zener diode in series with the output rectifier (Figure 4A). An alternative configuration, suggested by J. Dutra of LTC, AC couples the output to achieve a 0V output (Figure 4B). Both of these methods add component count, decrease efficiency and slightly limit available output current. They are unnecessary unless the user desires a 0V output on the Vpp line.

A good question might be; "Why not set the switching regulator output voltage at the desired Vpp level and use a simple low resistance FET or bipolar switch?" This is a potentially dangerous approach. Figure 5 shows the clean output of a low resistance switch operating directly at the Vpp supply. The PC trace run to the memory chip looks like a transmission line with ill-defined termination characteristics. As such, Figure 5's clean pulse degrades and rings badly (Figure 6) at the memory IC's pins. Overshoot exceeds 20V, well beyond the 14V destruction level. The controlled edge times of the circuit discussed eliminate this problem. Further discussion of this and other circuits appears in LTC Application Note 31, "Linear Circuits for Digital Systems" and LTC Demo Manual DC019, "Flash Memory Vpp Generator."

LINEAR
LINEAR TECHNOLOGY
FLASH MEMORY PROGRAMMER
DEMONSTRATION CIRCUIT
(408) 432-1900
+5V
+VPP
SHUTDOWN
GND
GND

Figure 3. Simple Flash Memory Pulser Uses All Surface Mount Components



4A

4B

Figure 4. Two Arrangements for Obtaining a 0V Output

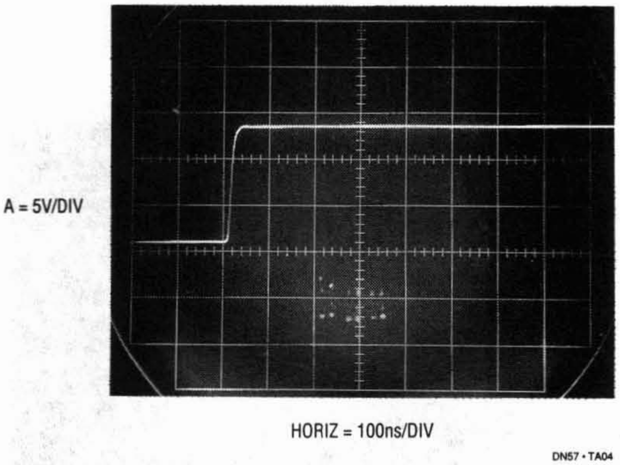


Figure 5. An "Ideal" Flash EPROM Vpp Pulse

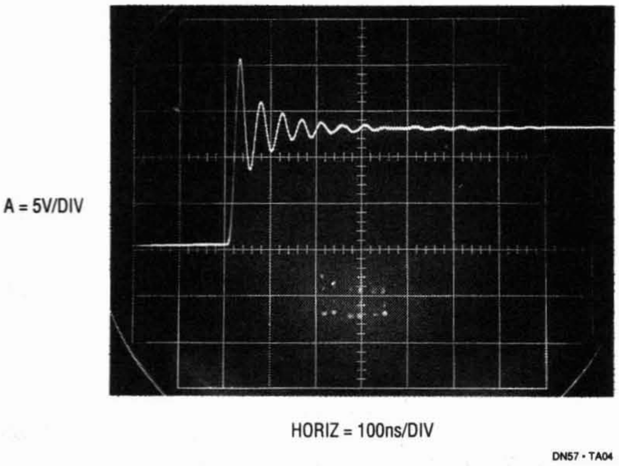


Figure 6. Rings at Destructive Voltages After a PC Trace Run

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DESIGN NOTES

5V High Current Step-Down Switchers – Design Note 59

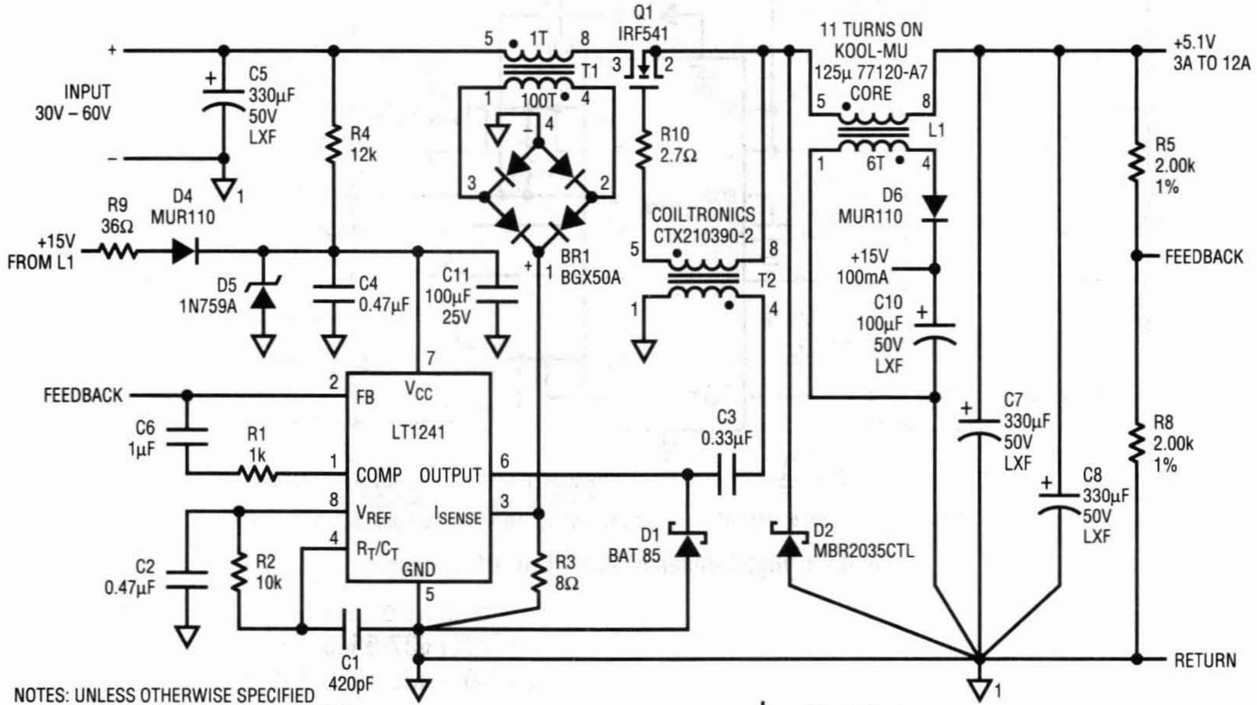
Ron Vinsant and Milton Wilcox

Low Cost High Efficiency (80%), High Power Density DC-to-DC Converter

The LT1241 current mode PWM control IC can be used to make a simple high frequency step-down converter. This converter also has low manufacturing costs due to simple magnetic components. This circuit exhibits a wide input range of 30V to 60V while maintaining its 12A 5V output. It has short circuit protection and uses minimal PC board area due to its 300KHz switching frequency.

Figure 1 shows the LT1241 being used to drive the switching transistor Q1 through a ferrite pulse transformer T2. This transformer is built on a high μ material resulting in an 11 turn bifilar wound toroid that is only 0.15 inches in diameter and can be surface mounted. T1 acts as a current sense transformer whose volt•second balance is assured by the duty cycle limit of 50% inherent in the LT1241. The output inductor (L1) is made of Magnetics Kool-Mu material and is only 0.7 inches in diameter.

Short circuit protection is provided through bootstrap operation of the LT1241. If the output is shorted the LT1241 limits its pulse width to ≤ 250ns. Because there is not enough current supplied to make the aux winding on the output inductor 15V, the LT1241 stops operation. It will then try to start by C11 charging through R4. If the output is still shorted it will stop again. Thus in a short, the circuit starts and stops, protecting itself from overload.


INPUT
30V – 60V
+
–
C5
330μF
50V
LXF
R4
12k
5
1T
8
T1
1
100T
4
Q1
IRF541
3
2
R10
2.7Ω
11 TURNS ON
KOOL-MU
125μ 77120-A7
CORE
5
8
L1
1
6T
4
+5.1V
3A TO 12A
R5
2.00k
1%
FEEDBACK
R9
36Ω
D4
MUR110
+15V
FROM L1
D5
1N759A
C4
0.47μF
C11
100μF
25V
BR1
BGX50A
COILTRONICS
CTX210390-2
T2
D6
MUR110
+15V
100mA
C10
100μF
50V
LXF
FEEDBACK
C6
1μF
R1
1k
FB
VCC
LT1241
COMP
OUTPUT
VREF
ISENSE
RT/CT
GND
C3
0.33μF
C7
330μF
50V
LXF
R8
2.00k
1%
C8
330μF
50V
LXF
C2
0.47μF
R2
10k
R3
8Ω
D1
BAT 85
D2
MBR2035CTL
C1
420pF
RETURN

NOTES: UNLESS OTHERWISE SPECIFIED
1. ALL RESISTANCES ARE IN OHMS, 1/4W, 5%.
2. ALL CAPACITANCES ARE IN MICRO-FARADS, 50V, 10%.
3. MBR2035CTL MOUNTING TAB IS TIED TO THE DEVICE'S CATHODES INTERNALLY.
4. T1 METGLAS MP1305P-4AF CORE.

= POWER GND
= SIGNAL GND
DN59 • TA01

Figure 1.

Synchronous Switching Eliminates Heatsinks in a 50W DC-to-DC Converter

The new LT1158 half bridge N-Channel power MOSFET driver makes an ideal synchronous switch driver to improve the efficiency of step-down (buck) switching regulators. The diode losses in a conventional step-down regulator become increasingly significant as V_{IN} is increased. By replacing the high-current Schottky diode with a synchronously-switched power MOSFET, efficiencies well over 90% can be realized (see Figure 2).

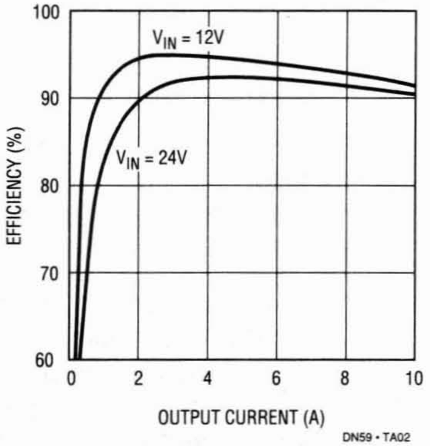
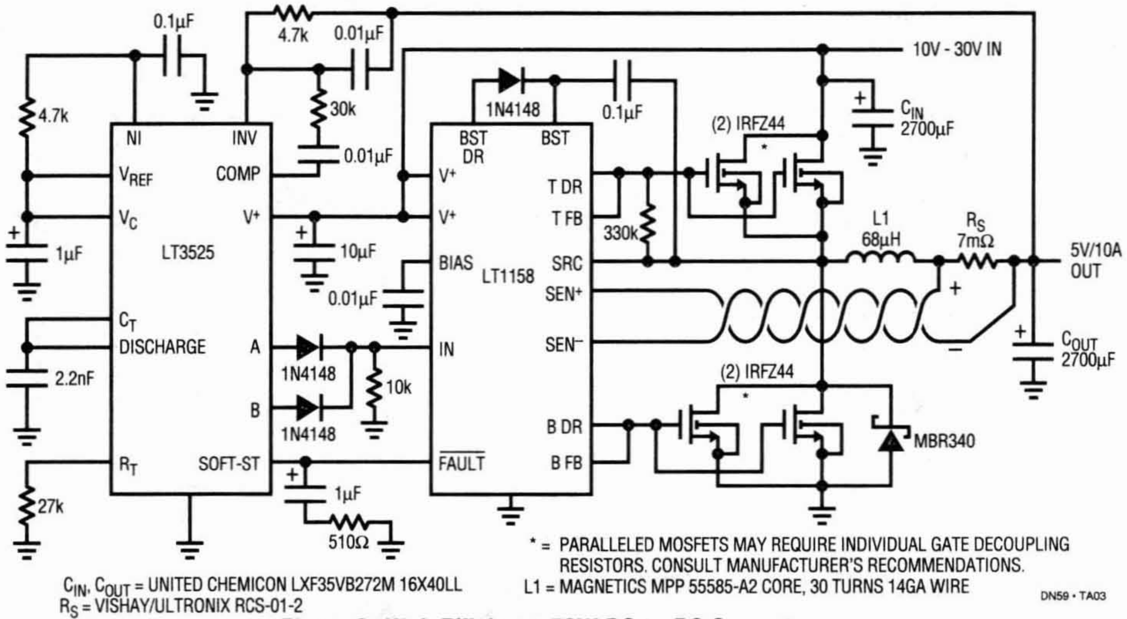


Figure 2. Operating Efficiency for Figure 3 Circuit

In the Figure 3 circuit an LT3525 provides a voltage mode PWM to drive the LT1158 input pin. The LT1158 drives (2) 28mΩ power MOSFETs for each switch, reducing individual device dissipation to 0.7W worst case. This eliminates the need for heatsinks for operation up to 10A at a temperature of 50°C ambient. The inductor and current shunt losses for the Figure 3 circuit are 1.2W and 0.7W respectively at 10A.

An additional loss potentially larger than those already mentioned results from the gate charge being delivered to multiple large MOSFETs at the switching frequency. This driver loss can only be controlled by running the oscillator at as low a frequency as practical — in the case of the Figure 3 circuit, 25kHz. A very low ESR (<20mΩ) output capacitor is used to limit output ripple to less than 50mVp-p with 2.5Ap-p ripple current.

The LT1158 also provides current limit for DC-to-DC converter applications. When the voltage across R_S exceeds 110mV, the LT1158 $\overline{\text{fault}}$ pin conducts, and assumes control of the PWM duty cycle. This provides true current mode short circuit protection with soft recovery. The Figure 3 regulator current limit is set at 15A which raises the dissipation in each bottom MOSFET to 1.7W during a short. Therefore 30°C/W heatsinking must be added for the bottom side MOSFETs if continuous short circuit operation is required. Care should also be taken when routing the sense+ and sense– leads to prevent coupling from the inductor.



0.1µF
4.7k
0.01µF
10V - 30V IN
4.7k
30k
1N4148
0.1µF
NI
INV
BST DR
BST
C_{IN} 2700µF
(2) IRFZ44
0.01µF
V_{REF}
COMP
V+
T DR
V+
T FB
V_C
V+
330k
L1 68µH
R_S 7mΩ
10µF
1µF
LT3525
BIAS
LT1158
SRC
5V/10A OUT
0.01µF
SEN+
C_T
DISCHARGE
A
IN
SEN–
C_{OUT} 2700µF
1N4148
10k
(2) IRFZ44
2.2nF
B
1N4148
B DR
MBR340
R_T
SOFT-ST
$\overline{\text{FAULT}}$
B FB
1µF
27k
510Ω
DN59 • TA03

* = PARALLELED MOSFETS MAY REQUIRE INDIVIDUAL GATE DECOUPLING RESISTORS. CONSULT MANUFACTURER'S RECOMMENDATIONS.

L1 = MAGNETICS MPP 55585-A2 CORE, 30 TURNS 14GA WIRE

C_{IN}, C_{OUT} = UNITED CHEMICON LXF35VB272M 16X40LL

R_S = VISHAY/ULTRONIX RCS-01-2

Figure 3. High Efficiency 50W DC-to-DC Converter

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LINEAR TECHNOLOGY
DESIGN NOTES

The LTC1096 and 1098: Micropower, SO-8, 8-Bit ADCs Sample at 1kHz on 3µA of Supply Current – Design Note 60

William Rempfer and Marco Pan

The LTC1096 and LTC1098 are the lowest power, most compact, sampling analog-to-digital converters in the world. These new 8-bit micropower, sampling ADCs typically draw 100µA of supply current when sampling at 33kHz. Supply current drops linearly as the sample rate is reduced as shown in Figure 1. At a 1kHz sample rate, the supply current is only 3µA. The ADCs automatically power down when not performing conversions, drawing only leakage current.

They are packaged in 8-pin SO packages and operate on 3V to 9V supplies or batteries. Both are fabricated on Linear Technology's proprietary LTBiCMOS™ process.

Two Micropower ADCs

The LTC1096 and LTC1098 use a switched-capacitor, successive-approximation (SAR) architecture. Micropower operation is achieved through three design innovations:

1. An architecture which automatically powers up and down as conversions are requested
2. An ultra low power comparator design, and
3. The use of a proprietary BiCMOS process.

Although they share the same basic design, the LTC1096 and LTC1098 differ in some respects. The LTC1096 has a differential input and has an external reference input pin. It can measure signals floating on a DC common-mode voltage and can operate with reduced spans down to 250mV. Reducing the span allows it to achieve 1mV resolution. The LTC1098 has a two-channel input multiplexer and can convert either channel with respect to ground or the difference between the two.

Longer Battery Life

Tremendous gains in battery life are possible because of the wide supply voltage range, the low supply current, and the automatic power shut down between conversions. Eliminating the voltage regulator and operating directly off the battery saves the power lost in the regulator. At a sample rate of 1kHz, the 3µA supply current is below the self-discharge rate of many batteries. As an example, the circuit of Figure 2, sampling at 1kHz, will run off a Panasonic CR1632 3V lithium coin cell for five years.

The automatic shutdown has great advantages over the alternative of high-side switching a higher power ADC, shown in Figure 3. First, no switching signal or hardware is required. Second, power consumption is orders of magnitude lower with the LTC1096/8. This is because, when an

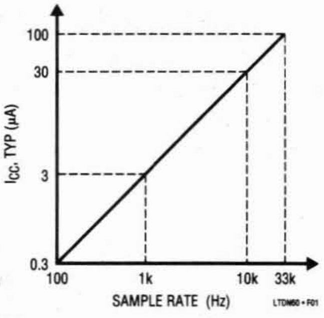


Figure 1. Automatic power shutdown between conversions allows power consumption to drop with sample rate.

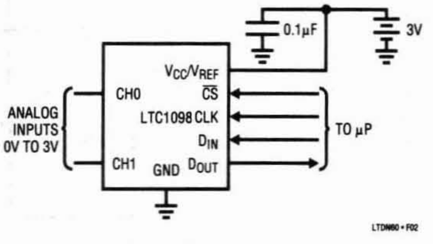
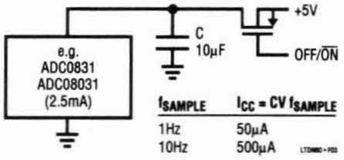


Figure 2. Sampling at 1kHz, this circuit draws only 3µA and will run off a 120mAhr CR1632 3V lithium coin cell for 5 years.



f_{SAMPLE}	$I_{CC} = CV f_{SAMPLE}$
1Hz	50µA
10Hz	500µA

Figure 3. High-side switching a power-hungry ADC wastes power. Repeatedly switching the required bypass capacitor consumes 500µA even when taking readings at only 10Hz.

LTBiCMOS is a trademark of Linear Technology Corporation

ADC is high-side switched, the current consumed in charging the required bypass capacitor is large, even at very low sample rates. In fact, a 10µF bypass capacitor, high-side switched at only 10Hz, will consume 500µA!

A/D Conversion for 3V Systems

The LTC1096/8 are ideal for 3V systems. Figure 4 shows a 3V to 6V battery current monitor which draws only 70µA from the battery it monitors. The battery current is sensed with the 0.02Ω resistor and amplified by the LT1178. The LTC1096 digitizes the amplifier output and sends it to the microprocessor in serial format. The LT1004 provides the full scale reference for the ADC. The other half of the LTC1178 is used to provide low battery detection. The circuit's 70µA supply current is dominated by the op amps and the reference. The circuit can be located near the battery and data transmitted serially to the microprocessor.

Smaller Instrument Size

The LTC1096 and LTC1098 can save board space in compact designs in a number of ways. The S0-8 package saves space. Operating the ADC directly off batteries can eliminate the space taken by a voltage regulator. The LTC1096/8 can also operate with small, 0.1µF or 0.01µF chip bypass capacitors. The serial I/O requires fewer PC traces and fewer microprocessor pins than a parallel-port ADC. Connecting the ADC directly to sensors can eliminate op amps and gain stages. Finally, the ADCs do not need an external sample-and-hold.

AC and DC Performance

The LTC1096/8 are offered with +/– 0.5LSB total unadjusted error for applications that require DC accuracy. The ADCs also have a lot to offer in designs that require AC performance. Figure 5 shows remarkable sampling performance for a device that draws only 100µA running at full speed. Dynamic performance of 7.5 effective bits is maintained up to an input frequency of over 40kHz.

In undersampling applications, this 40kHz input bandwidth remains intact as the sample rate (and power consumption) are reduced. A 40kHz waveform can be undersampled at 1kHz with 7.5 bits of accuracy on a supply current of 3µA!

Conclusion

Extremely low power consumption, 3V operation, small size and other benefits will help the LTC1096 and LTC1098 find their way into a variety of micropower, low-voltage, battery-powered and compact systems. For more information, refer to the LTC1096/8 data sheet, Linear Technology Magazine (Volume II Number 1) and application notes.

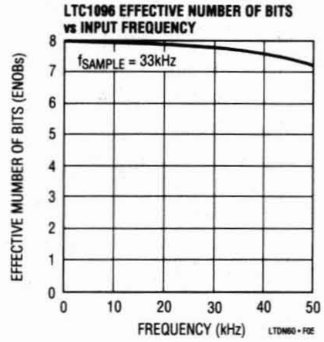


Figure 5. Dynamic accuracy is maintained up to an input frequency of over 40kHz.

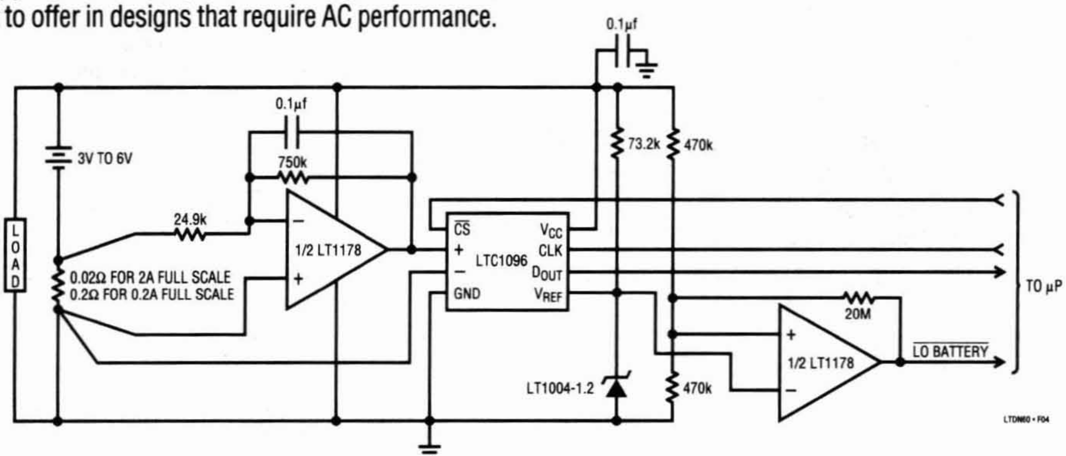


Figure 4. This 0 to 2A battery current monitor draws only 70µA from a 3V to 6V battery.

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LINEAR TECHNOLOGY
DESIGN NOTES

Peak Detectors Gain in Speed and Performance – Design Note 61

John Wright

Introduction

Fast peak detectors place unusual demands on amplifiers. High slew rate is needed to keep the amplifier internal nodes from overracing the output stage. This condition causes either a long overload, or DC accuracy errors. To support the high slew rate at the output, the amplifier must deliver large currents into the capacitive load of the detector. Compounding these problems are issues of amplifier instability with a large capacitive load, as well as the accuracy of the output voltage.

Detecting Sinewaves

The LT1190 is the ideal candidate for this application, with a high 400V/µs slew rate, large 50mA output current, and a wide 70 degree phase margin. The closed-loop peak detector circuit of Figure 1 uses a Schottky diode inside the feedback loop to obtain good accuracy. The 20Ω resistor R_O isolates the 0.01µF load and prevents oscillation. The DC error with a sinewave input is plotted in Figure 2 for various input amplitudes. The DC value is read with a DVM. At low frequency, the error is small and dominated by decay of the detector capacitor between cycles. As frequency rises the error increases because capacitor charging time decreases. During this time the overdrive becomes a very small portion of a sinewave cycle. Finally at approximately 4MHz the error rises rapidly due to the slew rate limitation of the op amp. For comparison purposes the error of an LM118 is also plotted for $V_{IN} = 2V_{P\text{-}P}$.

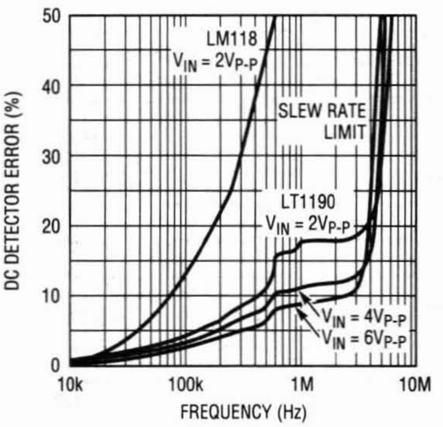

Figure 2. Closed-Loop Peak Detector Error vs Frequency

A fast Schottky diode peak detector can be built with a 1000pF capacitor, and 10k pull down. Although this simple circuit is very fast, it has limited usefulness due to the error of the diode threshold, and its low input impedance. The accuracy of this simple circuit can be improved with the LT1190 circuit of Figure 3. In this open-loop design, the detector diode is D1, and a level shifting or compensating diode is D2. A load resistor R_L is connected to –5V, and an identical bias resistor R_B is used to bias the compensating diode. Equal value resistors ensure that the diode drops are equal. Low values of R_L and R_B (1k to 10k) provide fast response, but at the expense of poor low frequency accu-

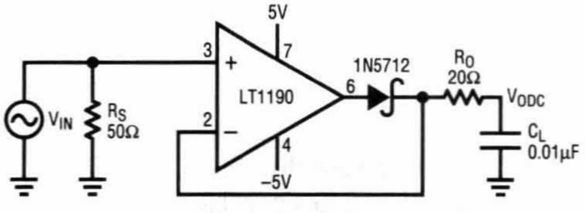

Figure 1. Closed-Loop Peak Detector

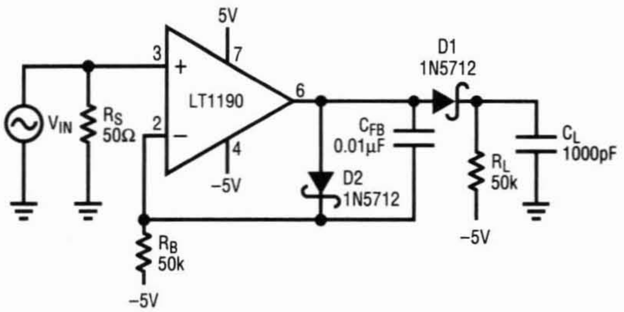

Figure 3. Open-Loop High Speed Peak Detector

racy. High values of R_L and R_B provide good low frequency accuracy, but cause the amplifier to slew rate limit, resulting in poor high frequency accuracy. A good compromise can be made by adding a feedback capacitor C_{FB} which enhances the negative slew rate on the (–) input. The DC error with a sinewave input is plotted in Figure 4 and is read with a DVM. For comparison purposes the LM118 error is plotted as well as the error of the simple Schottky detector.

Detecting Pulses

A fast pulse detector can be made with the circuit of Figure 5. A very fast input pulse will exceed the amplifier slew rate and cause a long overload recovery time. Some amount of dv/dt limiting on the input can help this overload condition, however this will delay the response. Figure 6 shows the detector error vs pulse width. Figure 7 is the response to a $4V_{P-P}$ input that is 80ns wide. The maximum output slew rate in the photo is 70V/µs. This rate is set by the 70mA current limit driving 1000pF. As a performance benchmark, the LM118 takes 1.2µs to peak detect and settle the same amplitude input. This slower response is due in part to the much lower slew rate and lower phase margin of the LM118.

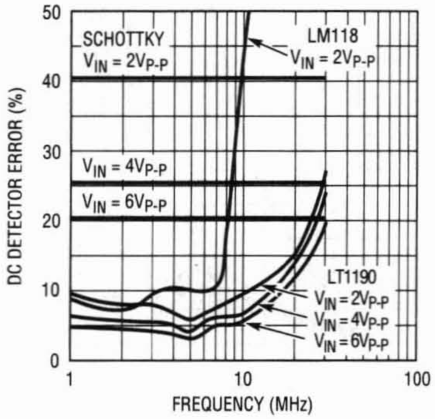

Figure 4. Open-Loop Peak Detector Error vs Frequency

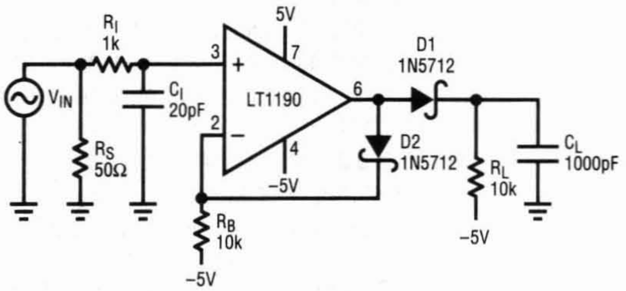

Figure 5. Fast Pulse Detector

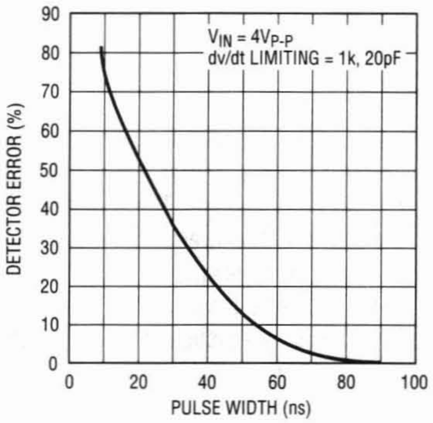

Figure 6. Detector Error vs Pulse Width

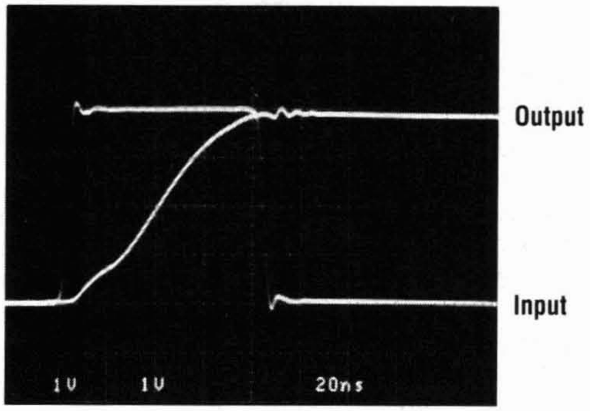

Figure 7. Open-Loop Peak Detector Response

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DESIGN NOTES

No Design Offline Power Supply – Design Note 62

Anthony Bonte and Ron Vinsant

Offline Switcher Eliminates Optocoupler Feedback. Low Cost, Simple, 50W, Universal Input Power Supply.

Linear Technology has broken through the "buy-vs-build" barrier for offline power supplies. The new LT1105[1] current-mode PWM control IC is used to make a simple, triple output power supply (Figure1). The circuit features low cost, high reliability and customizable footprint. It accepts a universal input of 85VAC-270VAC while providing isolated and regulated output voltages of 5V at 5A, 12V at 1.5A and –12V at 0.5A. MTBF is calculated at >100k hours for full load at 25°C ambient. The power supply contains all necessary components including an input EMI filter. All outputs have continuous short-circuit protection. Figure 2 indicates 5V load regulation performance as a function of input line voltage.

The LT1105 eliminates optocoupler feedback by regulating the flyback voltage of the bootstrap bias winding. This reduces the number of components crossing the isolation barrier to one: the transformer. The transformer is designed to meet international safety standards and is subject to a set of compromises involving efficiency, maximum power output, size, coupling, leakage inductance, interwinding capacitance and ultimately cost. A unique sampling error amplifier incorporated into the LT1105 allows operation in spite of the resultant transformer limitations. The error amplifier provides a feedback term allowing load regulation performance to be set with one external resistor. Thus, ±1% line and load regulation performance is achievable for single output voltage power supplies operating in either continuous or discontinuous mode[2].

LTC has simplified the magnetics design task by creating a series of off-the-shelf transformers for a variety of applications. New transformer design continues as an area of development. Transformers in power levels of 50W and 100W are presently available and meet international safety standards UL1950 and IEC950. Completed transformers are available from Coiltronics at 305-781-8900.

The LT1105's totem-pole output drives the gate of external high-voltage FET switch Q1. R10 controls switching transition speed. Transition speed is a trade-off between minimizing switch dV/dt common mode current contributions vs minimizing switching losses. FET conduction losses are set by the values of switch "on" resistance and primary current. The FET voltage rating must exceed the sum of the maximum rectified DC input voltage plus the leakage inductance spike. Finally, the external FET is protected from insufficient or excessive gate drive voltage with a drive protection circuit built into the LT1105.

Short-circuit protection is provided by bootstrap operation of the LT1105. Shorting an output results in switch duty cycle "on" time being limited to 500ns. The transformer cannot store sufficient energy to maintain a regulated bias winding voltage. The LT1105 senses this condition and shuts down the power supply. The power supply then returns to start-up mode. Trickle resistor R11 charges input bypass capacitor C8 to the LT1105 start threshold voltage. If the output remains shorted, the LT1105 starts and stops again. This "burp" mode protects the power supply from overload or indicates an incomplete power loop. Sense resistor R22 sets the maximum switch current available. To guarantee "burp" mode operation under fault conditions, C8 must be prevented from peak-detecting the large leakage inductance spike during maximum switch current cycles. Otherwise, the bootstrapped supply voltage would increase under a fault condition thereby leading to catastrophic failure. Resistor R3 along with C8 forms an R-C filter which prevents the diode D2/C8 combination from peak detection. This ensures well defined start cycles.

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[1] Data Sheet, LT1103/LT1105 Offline Switching Regulator, Linear Technology Corporation, Milpitas, CA., March 1992

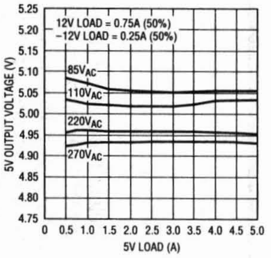
[2] Bonte, A. and Vinsant R., "Offline Switching Regulators Achieve ±1% Regulation in a Flux-Sensed Converter", Seventh Annual Applied Power Electronics Conference, IEEE-7803-0485-392, p 513-516, 1992

WARNING!

DANGEROUS AND LETHAL POTENTIALS ARE PRESENT IN OFFLINE CIRCUITS!

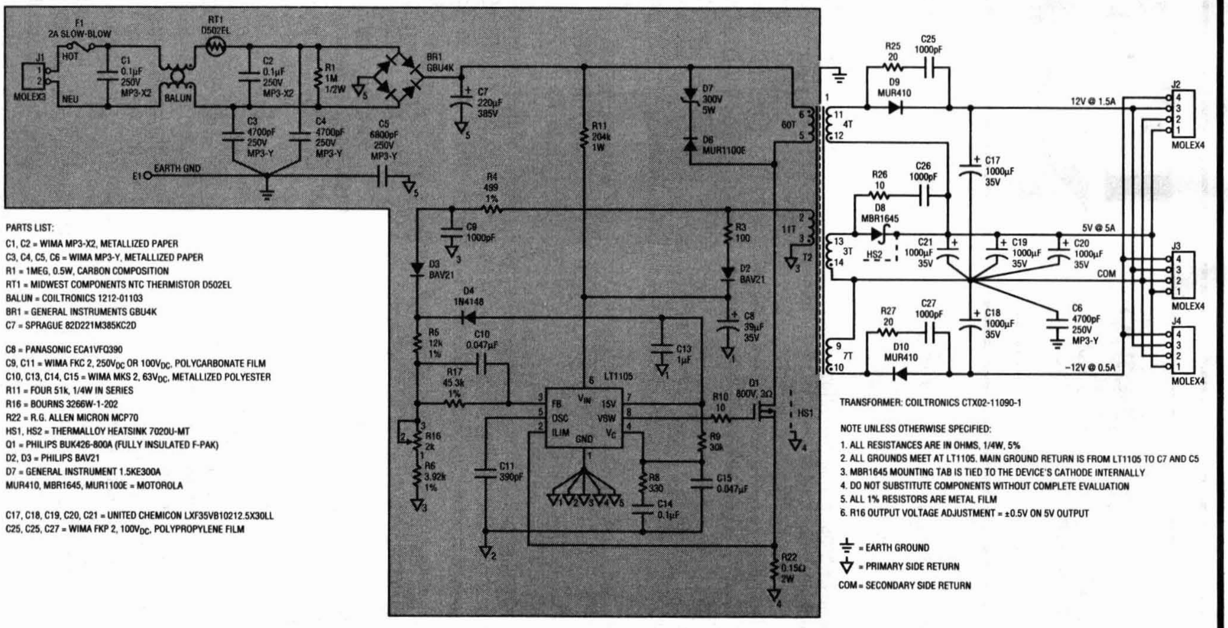
BEFORE PROCEEDING ANY FURTHER, THE READER IS WARNED THAT CAUTION MUST BE USED IN THE CONSTRUCTION, TESTING AND USE OF OFFLINE CIRCUITS. HIGH VOLTAGE, AC LINE-CONNECTED POTENTIALS ARE PRESENT IN THESE CIRCUITS. EXTREME CAUTION MUST BE USED IN WORKING WITH AND MAKING CONNECTIONS TO THESE CIRCUITS. REPEAT: OFFLINE CIRCUITS CONTAIN DANGEROUS, AC LINE-CONNECTED HIGH VOLTAGE POTENTIALS. USE CAUTION.

ALL TESTING PERFORMED ON AN OFFLINE CIRCUIT MUST BE DONE WITH AN ISOLATION TRANSFORMER CONNECTED BETWEEN THE OFFLINE CIRCUIT'S INPUT AND THE AC LINE. USERS AND CONSTRUCTORS OF OFFLINE CIRCUITS MUST OBSERVE THIS PRECAUTION WHEN CONNECTING TEST EQUIPMENT TO THE CIRCUIT TO AVOID ELECTRIC SHOCK. REPEAT: AN ISOLATION TRANSFORMER MUST BE CONNECTED BETWEEN THE CIRCUIT INPUT AND THE AC LINE IF ANY TEST EQUIPMENT IS TO BE CONNECTED.



DN62 • F02

Figure 2. 5V Load Regulation vs Line Voltage


F1
2A SLOW-BLOW
RT1
D502EL
J1
HOT
NEU
MOLEX3
C1
0.1µF
250V
MP3-X2
BALUN
C2
0.1µF
250V
MP3-X2
R1
1M
1/2W
BR1
GBU4K
C7
220µF
385V
C3
4700pF
250V
MP3-Y
C4
4700pF
250V
MP3-Y
C5
6800pF
250V
MP3-Y
E1
EARTH GND
R11
204k
1W
D7
300V
5W
D6
MUR1100E
60T
R4
499
1%
C9
1000pF
D3
BAV21
R3
100
11T
T2
D2
BAV21
D4
1N4148
C8
39µF
35V
R5
12k
1%
C10
0.047µF
C13
1µF
LT1105
VIN
FB
OSC
ILIM
GND
15V
VSW
VC
R17
45.3k
1%
R10
10
Q1
800V, 3Ω
HS1
R16
2k
R6
3.92k
1%
C11
390pF
R9
30k
R8
330
C14
0.1µF
C15
0.047µF
R22
0.15Ω
2W
R25
20
C25
1000pF
D9
MUR410
4T
12V @ 1.5A
J2
MOLEX4
R26
10
C26
1000pF
C17
1000µF
35V
D8
MBR1645
3T
HS2
C21
1000µF
35V
C19
1000µF
35V
C20
1000µF
35V
5V @ 5A
COM
J3
MOLEX4
R27
20
C27
1000pF
C18
1000µF
35V
C6
4700pF
250V
MP3-Y
D10
MUR410
7T
–12V @ 0.5A
J4
MOLEX4

PARTS LIST:

C1, C2 = WIMA MP3-X2, METALLIZED PAPER
C3, C4, C5, C6 = WIMA MP3-Y, METALLIZED PAPER
R1 = 1MEG, 0.5W, CARBON COMPOSITION
RT1 = MIDWEST COMPONENTS NTC THERMISTOR D502EL
BALUN = COILTRONICS 1212-01103
BR1 = GENERAL INSTRUMENTS GBU4K
C7 = SPRAGUE 82D221M385KC2D

C8 = PANASONIC ECA1VFQ390
C9, C11 = WIMA FKC 2, 250V_{DC} OR 100V_{DC}, POLYCARBONATE FILM
C10, C13, C14, C15 = WIMA MKS 2, 63V_{DC}, METALLIZED POLYESTER
R11 = FOUR 51k, 1/4W IN SERIES
R16 = BOURNS 3266W-1-202
R22 = R.G. ALLEN MICRON MCP70
HS1, HS2 = THERMALLOY HEATSINK 7020U-MT
Q1 = PHILIPS BUK426-800A (FULLY INSULATED F-PAK)
D2, D3 = PHILIPS BAV21
D7 = GENERAL INSTRUMENT 1.5KE300A
MUR410, MBR1645, MUR1100E = MOTOROLA

C17, C18, C19, C20, C21 = UNITED CHEMICON LXF35VB10212.5X30LL
C25, C25, C27 = WIMA FKP 2, 100V_{DC}, POLYPROPYLENE FILM

TRANSFORMER: COILTRONICS CTX02-11090-1

NOTE UNLESS OTHERWISE SPECIFIED:

1. ALL RESISTANCES ARE IN OHMS, 1/4W, 5%
2. ALL GROUNDS MEET AT LT1105. MAIN GROUND RETURN IS FROM LT1105 TO C7 AND C5
3. MBR1645 MOUNTING TAB IS TIED TO THE DEVICE'S CATHODE INTERNALLY
4. DO NOT SUBSTITUTE COMPONENTS WITHOUT COMPLETE EVALUATION
5. ALL 1% RESISTORS ARE METAL FILM
6. R16 OUTPUT VOLTAGE ADJUSTMENT = ±0.5V ON 5V OUTPUT

⏚ = EARTH GROUND
▽ = PRIMARY SIDE RETURN
COM = SECONDARY SIDE RETURN

DN62 F01

Figure 1. LT1105 Fully Isolated, Offline Flyback, 100kHz, 50W Converter with Load Regulation Compensation

For literature on our DC to DC Converters, call **(800) 637-5545**. For applications help, call (408) 432-1900, Ext. 456

LINEAR TECHNOLOGY
DESIGN NOTES

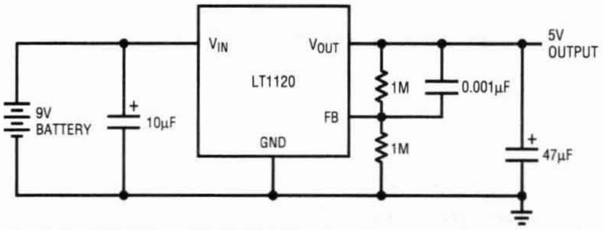
2 AA Cells Replace 9V Battery, Extend Operating Life

Design Note 63

Steve Pietkiewicz

Operating life is an important feature in many portable battery-operated systems. In many cases the power source is the ubiquitous 9V "transistor" battery. 5V generation is accomplished with a linear regulator. Significant gains in battery life can be obtained by replacing the 9V/linear regulator combination with 2 AA cells and a step-up switching regulator. Two (alkaline) AA cells occupy 1.3 cubic inches, the same as a 9V battery, but contains 6WH of energy, compared to just 4WH in an alkaline 9V battery. Two AA cells also cost less than a 9V battery.[1] The additional energy in the AA cells provides longer operating life when compared to a 9V battery based solution.

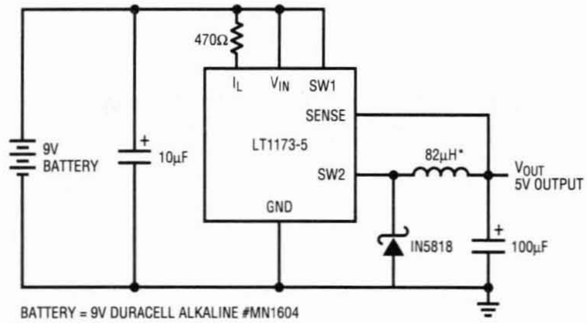
An evaluation of the three approaches with a 30mA load illustrates the differences in battery life. An HP7100B strip chart recorder provides a nonvolatile record of circuit performance. The linear regulator circuit shown in Figure 1 uses an LT1120 micropower low-dropout regulator IC. A minimum of external components are required. No inductors or diodes are needed; however, the linear step-down process is inherently inefficient. The step-down switcher shown in Figure 2 uses an LT1173 configured in step-down mode driven from an alkaline 9V battery. In Figure 3 the step-up circuit uses an LT1173 configured in step-up mode driven from a pair of alkaline AA cells. The two switching circuits require an external inductor, diode and output capacitor in addition to the IC.



BATTERY = 9V DURACELL ALKALINE #MN1604

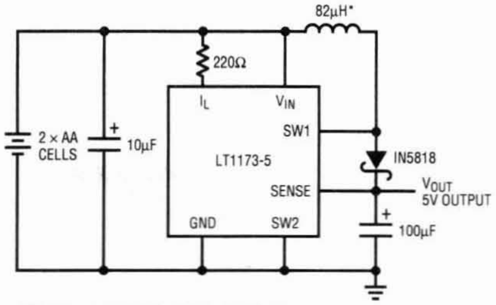
Figure 1. 9V to 5V Linear Regulator

Circuit operation of the switching step-down regulator is straightforward. A comparator inside the LT1173 senses output voltage on its "sense" pin. When V_{OUT} drops below 5V, the on-chip switch cycles. As current ramps up and ramps down in L1, it flows into C1 and the load, raising output voltage. When V_{OUT} rises above 5V, the cycling action stops and the regulator goes into a standby mode, pulling 110µA from the supply. C1 is left to supply energy to the load. These "bursts" of cycles occur as needed to keep the output voltage at 5V. 50mV of hysteresis at the sense pin eliminates the need for frequency compensation. The step-up regulator operates in a similar fashion, although in this case the inductor current flows into the load only on the discharge half of the switch cycle. Output voltage is regulated in a similar manner.



BATTERY = 9V DURACELL ALKALINE #MN1604
*TOKO 262LYF-0091K

Figure 2. 9V to 5V Step-Down Converter



BATTERY = 2× DURACELL "AA" ALKALINE #MN1500
*TOKO 262LYF-0091K

Figure 3. 3V to 5V Step-Up Converter

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[1] A quick check at the local drugstore yielded $2.99 for a 4-pack of alkaline AA cells and $2.49 for a single 9V battery (after $1.00 mail-in rebate).

Efficiency curves for the three circuits are shown in Figures 4 and 5. The linear regulator circuit has efficiency of 52% with a fresh battery. As the input-output differential decreases, the efficiency increases and at end of battery life exceeds 90%. Regulator ground current limits efficiency at drop-out. The switch-mode step-down circuit has almost constant efficiency, ranging from 84% at 6.3V input to 82% at 9.5V input. Minimum V_{IN} is set by the drop of the emitter follower switch inside the LT1173. Performance for the step-up converter is shown in Figure 5. At higher inputs, the switch drop is a lower percentage of supply, resulting in higher efficiency.

The three regulators show substantial differences in operating life. The linear regulator operates for 16.5 hours, as shown in Figure 6. Figure 7 shows a 19 hour operating life for the step-down switching circuit. The step-up regulator circuit's performance, detailed in Figure 8, yields an operating life of 26 hours. This is an increase of 58% over the linear step-down approach at less cost and 37% over the switching step-down approach.

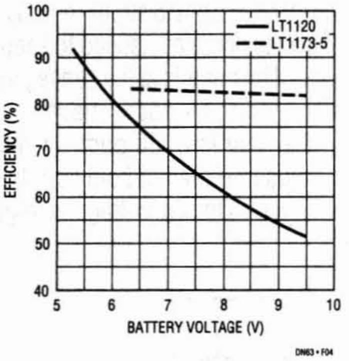

Figure 4. Step-Down Conversion Efficiency – 5V Output, 30mA Load

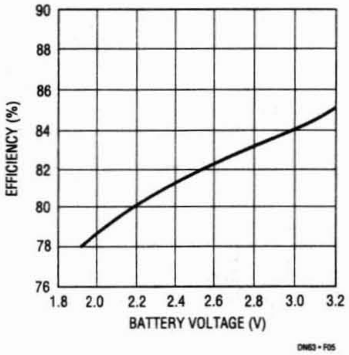

Figure 5. Step-Up Conversion Efficiency – 5V Output, 30mA Load

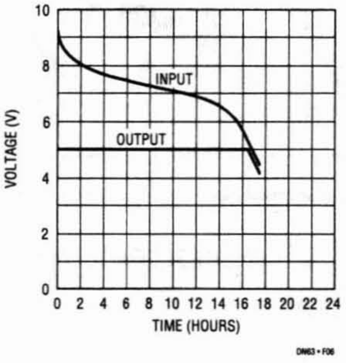

Figure 6. 9V to 5V Step-Down Linear – LT1120, 30mA Load

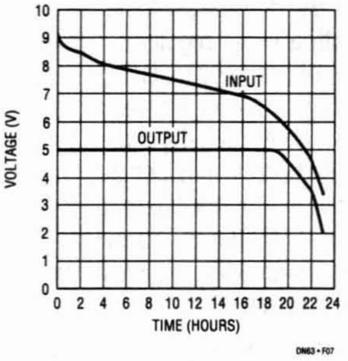

Figure 7. 9V to 5V Step-Down Switcher – LT1173-5, 30mA Load

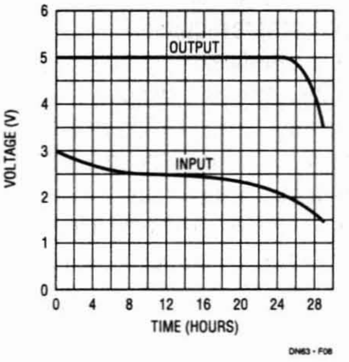

Figure 8. 3V to 5V Step-Up Switcher – LT1173-5, 30mA Load

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DESIGN NOTES

RS232 Transceivers for Hand Held Computers Withstand 10kV ESD – Design Note 64

Sean Gold

Battery-powered computers and instrumentation are often subjected to severe electrical stress which imposes some stringent demands on serial communication interfaces. As always, operating from a battery mandates minimal power consumption. Transceivers must also tolerate repetitive Electrostatic Discharge (ESD) pulses because cable connections frequently come in contact with humans and other charged bodies.

Linear Technology's LT1237 addresses the above requirements. The LT1237 is a complete RS232 port, with three drivers, five receivers and a regulated charge pump. Supply current is typically 6mA, but the device can be shut down with two separate logic controls. The driver disable pin shuts off the charge pump and the drivers – leaving all receivers active, I_{SUPPLY} = 4mA. The ON/$\overline{OFF}$ pin shuts down all circuitry except for one micropower receiver, I_{SUPPLY} = 60µA. The active receiver is useful for detecting start-up signals. The LT1237 operates up to 120kBaud and is fully compliant with all RS232 specifications. Connections to the RS232 cable are protected with internal ESD structures that can withstand repetitive ±10kV human body model ESD pulses.

Figure 1 shows a typical application circuit. The LT1237's flowthrough pinout and its ability to use small surface mount capacitors, helps reduce the interface's overall footprint.

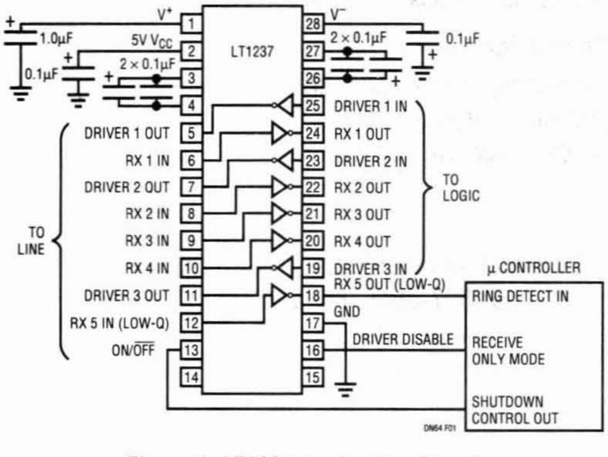
V+
1.0µF
5V V_{CC}
0.1µF
2 × 0.1µF
LT1237
V−
2 × 0.1µF
0.1µF
1
2
3
4
5
6
7
8
9
10
11
12
13
14
28
27
26
25
24
23
22
21
20
19
18
17
16
15
DRIVER 1 OUT
RX 1 IN
DRIVER 2 OUT
RX 2 IN
RX 3 IN
RX 4 IN
DRIVER 3 OUT
RX 5 IN (LOW-Q)
ON/$\overline{OFF}$
TO LINE
DRIVER 1 IN
RX 1 OUT
DRIVER 2 IN
RX 2 OUT
RX 3 OUT
RX 4 OUT
DRIVER 3 IN
RX 5 OUT (LOW-Q)
GND
DRIVER DISABLE
TO LOGIC
µ CONTROLLER
RING DETECT IN
RECEIVE ONLY MODE
SHUTDOWN CONTROL OUT
DN64 F01

Figure 1. LT1237 Application Circuit

Interfacing with 3V Logic

Hand held computers are rapidly moving to 3V logic to save power. Yet higher voltage buses are still utilized elsewhere in the system for display driving and other functions. The LT1330 is functionally equivalent to the LT1237 but operates from 5V with a separate logic supply to interface directly with 3V logic. (Figure 2)

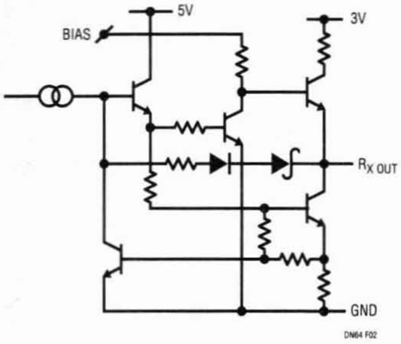
5V
3V
BIAS
$R_{X\,OUT}$
GND
DN64 F02

Figure 2. Receiver Output Stages in the LT1330 are Biased From a Separate Logic Supply to Easily Interface with 3V Systems

ESD Protection Techniques

Even though the I/O pins on the LT1237 and LT1330 are protected, a basic understanding of electrostatic discharge, its causes and its remedies, is helpful when designing with these circuits.

ESD generated by triboelectric charging of the human body is often the most troublesome problem for portable computers.[1] Energy imparted during a discharge is usually in the form of a rapidly rising high voltage pulse with a slow exponential tail. ESD pulses can be modeled with the switching circuit shown in Figure 3. ESD contributes frequency components well into the GHz range. At such frequencies, nearby cables and PC board traces look like receiving antennas for ESD noise.

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[1] Triboelectricity is the charge created as a result of friction between bodies.

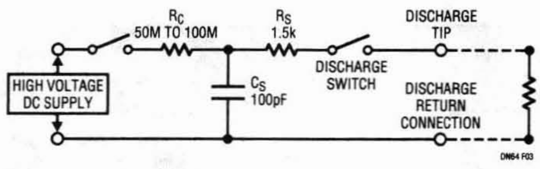

Figure 3. Human Body Circuit Model for ESD Pulses

Circuit damage from ESD can occur as a result of three effects: (1) High current heating, which destroys junctions or metallization. (2) Intense electromagnetic fields, which break down junctions or thin oxides. (3) Radiated noise, which drives the circuit into invalid or locked up states.

Any action which eliminates the charge generator, circumvents charge transfer, or enhances the circuit's ability to absorb energy, will increase a circuit's tolerance of ESD. Eliminating the ubiquitous charge generators and disrupting charge transfer are difficult tasks because they demand strict control of the circuit's operating environment. A more practical approach is to limit ESD entry points by shielding the circuit's enclosure and covering the RS232 port's connector when it is not in use.

Another practical remedy is to increase a transceiver's ability to absorb energy by clamping the RS232 line to ground with fast acting avalanche diodes or dedicated transient suppressors (Figure 4). Discrete suppressors are widely available and are extremely effective. Designers are often reluctant to use discrete suppressors because they are expensive. Costing up to $0.40/pin, they can sometimes exceed the cost of the transceiver.

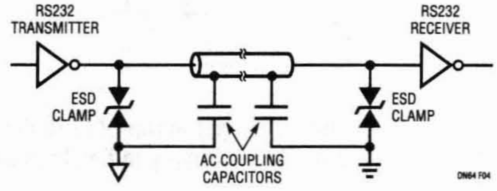

Figure 4. Older Interface Designs Used External ESD Clamps

The LT1237 and LT1330 incorporate the clamps for diverting ESD energy on chip. These active structures quickly respond to positive or negative signals at threshold voltages higher than RS232 signals, yet below destructive levels for the device. The path of high current flow is through large pn junctions which increases the capacity to absorb energy.

When a discharge occurs, the resulting current flow is insignificant when the transceiver is turned off or powered down. When operating, the resulting current may debias internal circuitry and lock up the circuit. Observations have shown these nondestructive errors to be highly dependent upon the logical state of the transceiver. Cycling the power clears the circuit.

When very high levels of ESD protection are required, an external LC filter (Figure 5) can be used to drop ESD energy into a range that can be safely dissipated within the transceiver.

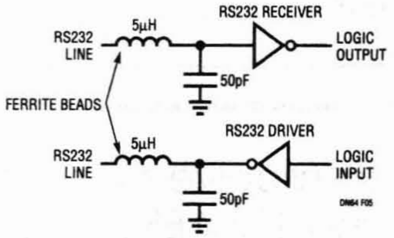

Figure 5. External LC Filters Provide Protection From Very High Levels of ESD Yet Cost Less Than Discrete Supressors

PC Board Layout

Energy shunted through an ESD clamp can still cause problems if the impedance of the return path is large enough to create a sizable voltage drop. Such voltage drops may damage unprotected components that share the common return line. Including a low inductance ground plane in the PC board is therefore essential for good ESD protection. For the LT1237 and LT1330, the AC path to ground through V^- must also be low impedance. Adding a few hundred picofarads of low ESR capacitance in parallel with the primary storage capacitor provides a good AC ground.

When using discrete transient suppressors or filters, place components as close as possible to the connector with short paths to the return plane. Make the spacing between the circuit board traces as wide as possible. ESD pulses can easily arc from one trace to another when the spacing between traces is narrow. Arcing occurs slowly compared with ESD rise time, so air spark gaps alone will not protect circuitry from ESD. Dedicated spark gaps are effective for limiting ESD energy when used with additional suppression devices.

Do not float the cable shield with respect to local ground. Designers may feel inclined to do this to avoid circulating current due to differences in ground potential. Instead, AC couple the grounds so they are shorted at ESD frequencies.

Conclusion

The techniques described here cannot entirely eliminate ESD problems, but understanding ESD's nature and using careful circuit design, will help protect against its intrusion.

For literature on our family of RS232 transceivers, call **(800) 637-5545**. For applications help, call (408) 432-1900, Ext. 456

Send Color Video 1000 Feet Over Low Cost Twisted-Pair

Design Note 65

John Wright

It is now possible to send and receive color composite video signals appreciable distances on a low cost twisted-pair. This technique is similar to the push toward twisted-pair cables in EtherNet systems to replace costly coaxial cable connections. The cost advantage of these techniques is significant. Standard 75Ω RG-59/U coaxial cable costs between 25¢ and 50¢ per foot, but a PVC twisted-pair is only pennies per foot. This means hundreds of dollars are saved in installations as short as 1000 feet, easily paying for additional electronics. The system also provides for "drops" or receiver taps along the twisted-pair.

This bidirectional "video bus" consists of the low cost LT1190 Op Amp and the LT1193 Video Difference Amplifier shown in Figure 1. A pair of LT1190s at TRANSMIT 1, is used to generate differential signals to drive the line which is back-terminated in its characteristic impedance. These amplifiers have high 50mA load driving ability, while maintaining a very high 450V/µs slew rate and 50MHz gain-bandwidth. The twisted-pair receiver is an LT1193 Video Difference Amplifier at RECEIVE 1, and it converts signals from differential to single-ended. The LT1193 offers features unavailable with other op amp configura-

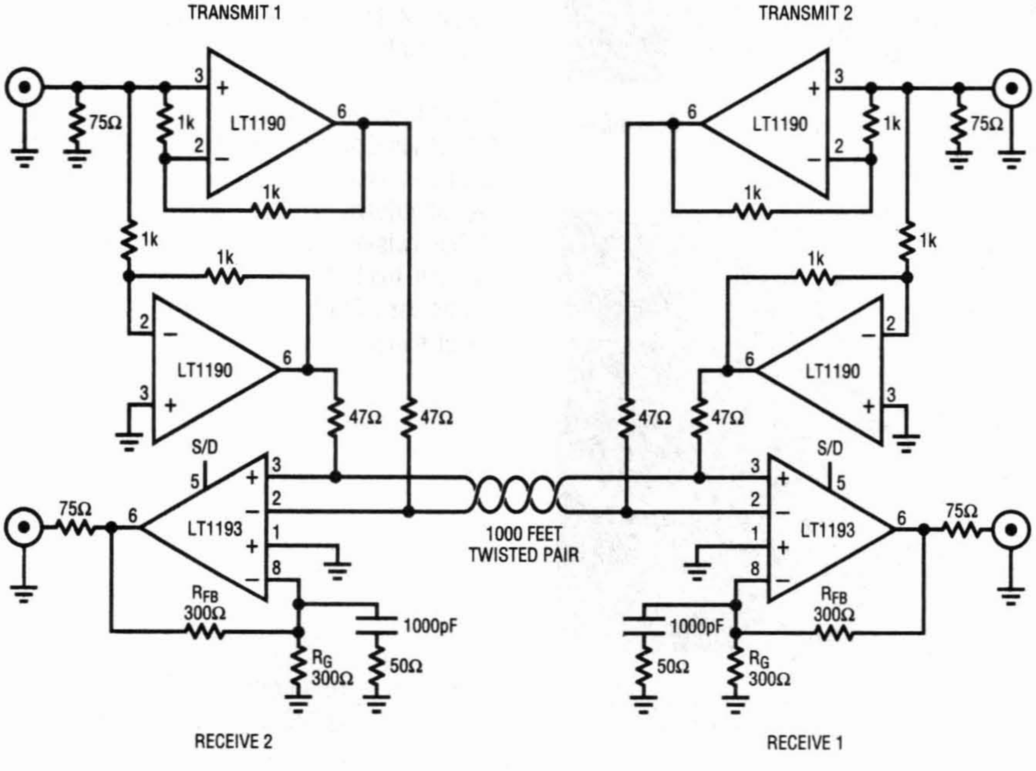

Figure 1. Bidirectional Video Bus

tions. In addition to speed and load driving ability, the LT1193 provides high input impedance (+) and (–) inputs, and common-mode rejection in excess of 40dB at 10MHz. Because of the LT1193's unique topology, it is possible to provide cable compensation at the amplifier's feedback node as shown. In this case, 1000 feet of twisted-pair is compensated with 1000pF and 50Ω to boost the –3dB bandwidth of the system from 750kHz to 4MHz. The effect of this compensation can be seen in Figure 2 and Figure 3. This bandwidth is adequate to pass 3.58MHz chroma subcarrier, and the 4.5MHz sound subcarrier. Attenuation in the cable can be compensated by lowering the gain-set resistor R_G in Figure 1. At TRANSMIT 2, another pair of LT1190s serves the dual function of providing cable termination via low output impedance, and generating differential signals for TRANSMIT 2.

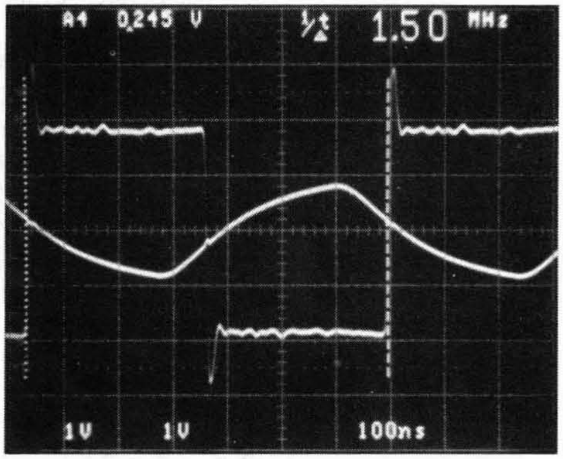

Figure 2. 1.5MHz Square Wave Input and Unequalized Response Through 1000 Feet of Twisted-Pair

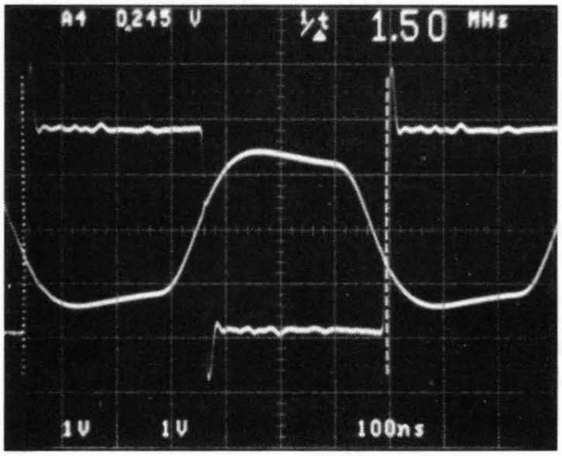

Figure 3. 1.5MHz Square Wave Input and Equalized Response Through 1000 Feet of Twisted-Pair

A good indication of the system's ability to pass color composite video is shown in Figure 4. This multiburst pattern was passed through 1000 feet of low cost PVC twisted-pair, and it contains a 3.58MHz chroma subcarrier and a 4.5MHz sound subcarrier. Although the scope photo shows these frequencies to be attenuated about 3dB, a clean picture is present at the end of the twisted-pair. Additional receiver taps can be added along the twisted-pair. The trick is to leave the taps unterminated and limit their length. Longer drops cause the 3.58MHz chroma subcarrier to reflect and interfere with the phase of the transmitted subcarrier. The effect is color smudge or in the limit ghosting.

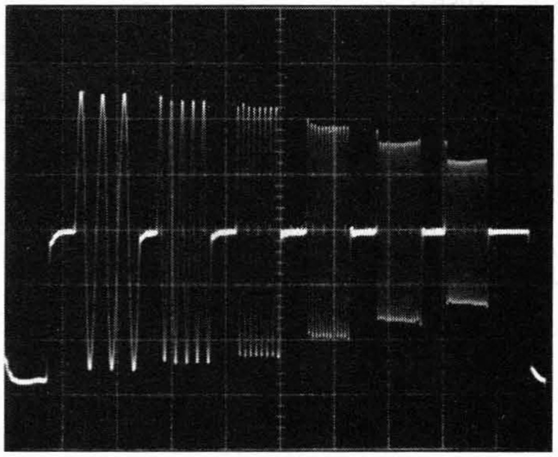

Figure 4. Multiburst Pattern Passed Through 1000 Feet of Twisted-Pair

The LT1190 and LT1193 include a shutdown feature that drops their dissipation to only 15mW when not in use. This feature is useful for shutdown of unused receivers, however shutdown of the drivers will result in mistermination of the twisted-pair. If power consumption is a major concern, the LT1190 and LT1193 can be replaced with the low power LT1195 and LT1187, resulting in only a slight performance degradation.

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LINEAR TECHNOLOGY
DESIGN NOTES

New 5V and 3V, 12-Bit ADCs Sample at 300kHz on 75mW and 140kHz on 12mW – Design Note 66

William Rempfer

Four new sampling A/D converters from Linear Technology stand out above the rest of the crowd. These new 5V and 3V 12-bit ADCs offer the best speed/power performance available today (see Figure 1). They also provide precision reference, internally trimmed clock, and fast sample-and-hold. With additional features such as single supply operation and high impedance analog inputs, they reduce system complexity and cost. This article will describe the new ADCs, discuss the 5V performance of the LTC1273/5/6 and then the 3V performance of the LTC1282.

Complete ADCs Provide Lowest Power and Highest Speed on Single or Dual Supplies

The LTC1273/5/6 and LTC1282 provide complete A/D solutions at previously impossible speed/power levels. As shown in Table 1, the LTC1273/5/6 all have the same 300kHz maximum sampling rate and 75mW typical power dissipation. The LTC1273 digitizes 0V to 5V inputs from a single 5V rail. The LTC1275 and LTC1276 operate on ±5V rails and digitize ±2.5V and ±5V inputs, respectively.

Table 1. Four New Complete ADCs Offer High Speed and Low Power on Single or Dual 5V or 3V Supplies

DEVICE	POWER SUPPLIES	INPUT RANGE	SAMPLE RATE	S/(N + D) @ F_{INPUT}	P_{DISS} (typ)
LTC1273	Single 5V	0V to 5V	300kHz	70dB @ 100kHz	75mW
LTC1275/6	±5V	±2.5/±5V	300kHz	70dB @ 100kHz	75mW
LTC1282	Single 3V or ±3V	0V to 2.5V or ±1.25	140kHz 140kHz	68dB @ 70kHz	12mW

The LTC1282 samples at 140kHz and typically dissipates only 12mW from either 3V or ±3V supplies. It digitizes 0V to 2.5V inputs from a single 3V supply or ±1.25V inputs from ±3V supplies.

Complete function is provided by the on-chip sample-and-holds, precision references, and internally trimmed clocks. The high impedance analog inputs are easy to drive and can be multiplexed without buffer amplifiers. A single 5V or 3V power supply is all that is needed to digitize unipolar inputs. (Bipolar inputs require ±5V or ±3V supplies but the negative supply draws only microamperes of current). But most significant are the speed/power ratios which are higher than any other ADC in this speed range.

5V ADCs Sample at 300kHz on 75mW of Power

The LTC1273/5/6 have excellent DC specs, including ±1/2LSB linearity and 25ppm/°C full-scale drift. In addition, they have excellent dynamic performance. As Figure 2 shows, the ADCs provide 72dB of Signal-to-Noise + Distortion (11.7 effective bits) at the maximum sample rate of 300kHz. The S/(N + D) ratio is over 70dB (11.3 effective bits) for input frequencies up to 100kHz.

This 300kHz sample rate and dynamic performance comes at a power level that is more stingy than any other ADC in this speed range. Figure 1 shows a graph of speed/power ratio for the competitive ADCs. The speed/power ratio is defined as the maximum sample rate in kHz divided by the typical power dissipation in mW. The 4.0 kHz/mW of the LTC1273/5/6 is better than the best competitive ADC.

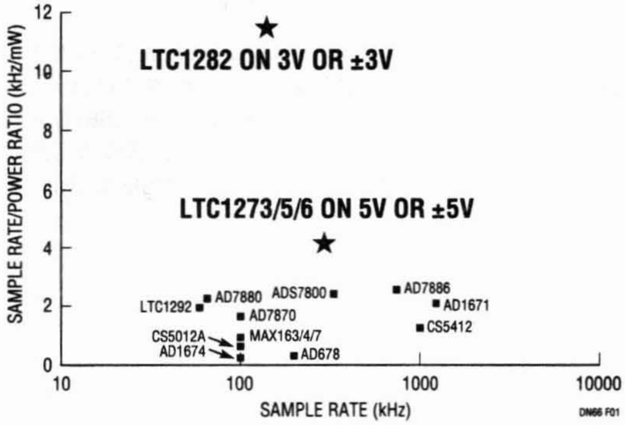

Figure 1. The LTC1273/5/6 and LTC1282 Have Up to 45 times Higher Speed/Power Ratios than Competitive ADCs

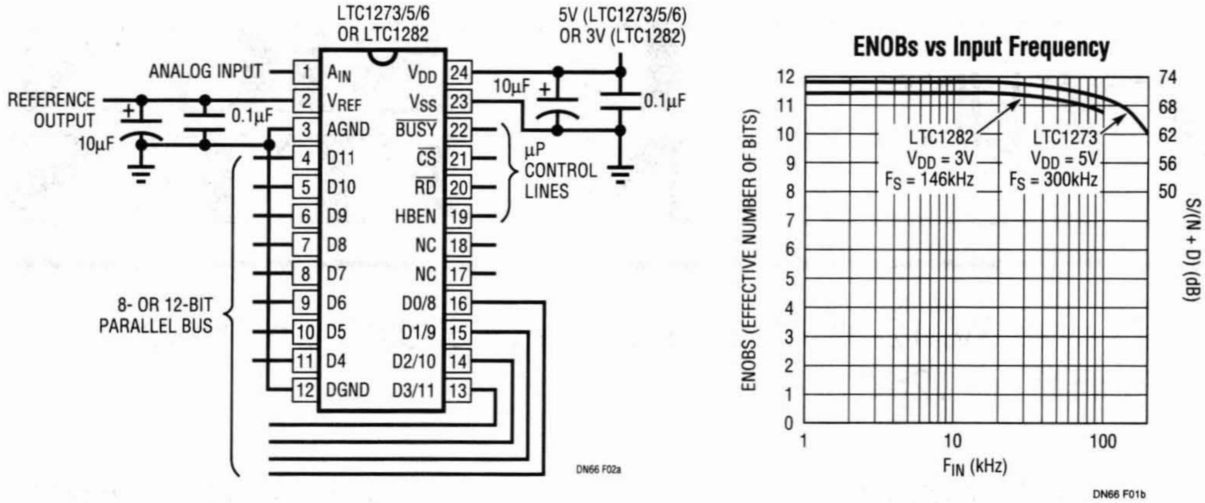
LTC1273/5/6
OR LTC1282
5V (LTC1273/5/6)
OR 3V (LTC1282)
ANALOG INPUT
REFERENCE
OUTPUT
10µF
0.1µF
10µF
0.1µF
1 A_{IN}
2 V_{REF}
3 AGND
4 D11
5 D10
6 D9
7 D8
8 D7
9 D6
10 D5
11 D4
12 DGND
24 V_{DD}
23 V_{SS}
22 BUSY
21 CS
20 RD
19 HBEN
18 NC
17 NC
16 D0/8
15 D1/9
14 D2/10
13 D3/11
µP
CONTROL
LINES
8- OR 12-BIT
PARALLEL BUS
DN66 F02a
ENOBs vs Input Frequency
ENOBS (EFFECTIVE NUMBER OF BITS)
S/(N + D) (dB)
F_{IN} (kHz)
LTC1282
V_{DD} = 3V
F_S = 146kHz
LTC1273
V_{DD} = 5V
F_S = 300kHz
0
1
2
3
4
5
6
7
8
9
10
11
12
50
56
62
68
74
1
10
100
DN66 F01b

Figure 2. The 300kHz LTC1273 Gives 70dB S/(N + D) with 100kHz Inputs. The 140kHz LTC1282 Gives 68dB S/(N + D) at Nyquist.

Even More Power Savings: 3V ADC Samples at 140kHz on 12mW

The low power, 3V LTC1282 provides even more impressive speed/power performance. As fast and dynamically accurate as many power hungry, dual and triple supply ADCs, this complete 3V or ±3V sampling ADC provides extremely good performance on only 12mW of power! DC specs include ±1/2LSB maximum linearity and the internal reference provides 25ppm maximum full-scale drift. Figure 2 shows 11.4 effective bits at 140kHz sample rate with 11 effective bits at the nyquist frequency of 70kHz. The speed/power ratio, as shown in Figure 1, is an outstanding 11.7kHz/mW.

The LTC1282 is ideal for 3V systems but will also find uses in 5V designs where the lowest possible power consumption is required. It interfaces easily to 3V logic but can also talk well to 5V systems. The LTC1282 can receive 5V CMOS levels directly and its 0V to 3V outputs can meet 5V TTL levels and connect directly to 5V systems.

The performance comparison in Table 2 shows that using the 3V LTC1282 gives great savings in power with only modest reductions in speed, accuracy and noise. The power dissipation has been reduced 6 times with only a 50% reduction in speed. Linearity and drift don't degrade at all in going to the 3V device. The noise of the LTC1282 is slightly higher, due to the reduced input span and the lower operating current, but the converter still gives more than 70dB S/(N + D).

Table 2. 5V and 3V Reference Comparison

Parameter	LTC1273 on a 5V Supply	LTC1282 on a Single 3V or ±3V Supplies
Power Dissipation (typ)	75mW	12mW
Sample Rate	300kHz	140kHz
Conversion Time (max)	2.7µs	6µs
INL (max)	1/2 LSB	±1/2 LSB
Typical ENOBs	11.7	11.4
Linear Input Bandwidth (ENOBs > 11Bits)	125kHz	70kHz

Conclusion

These new 5V and 3V ADCs offer the best speed/power performance available today. They also provide precision reference, internally trimmed clock, and fast sample-and-hold. With additional features such as single supply operation and high impedance analog inputs, they reduce system complexity and cost. For performance, power and cost, these new ADCs must be considered for new designs.

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LINEAR TECHNOLOGY
DESIGN NOTES

A 1mV Offset, Clock-Tunable, Monolithic 5-Pole Lowpass Filter – Design Note 67

Nello Sevastopoulos

The LTC1063 is the first monolithic lowpass filter simultaneously offering outstanding DC and AC performance. It features internal or external clock tunability, cutoff frequencies up to 50kHz, 1mV typical output DC offset, and a dynamic range in excess of 12 bits for over a decade of input voltage.

The LTC1063 approximates a 5-pole Butterworth lowpass filter. The unique internal architecture of the filter allows outstanding amplitude matching from device to device. Typical matching ranges from 0.01dB at 25% of the filter passband to 0.05dB at 50% of the filter passband. This capability is important for multichannel data-acquisition systems where channel-to-channel matching is critical.

Using the Filter's Internal Oscillator

An internal or external clock programs the filter's cutoff frequency. The clock-to-cutoff frequency ratio is 100:1. In the absence of an external clock, the LTC1063's internal precision oscillator can be used. An external resistor and capacitor set the device's internal clock frequency (Figure 1).

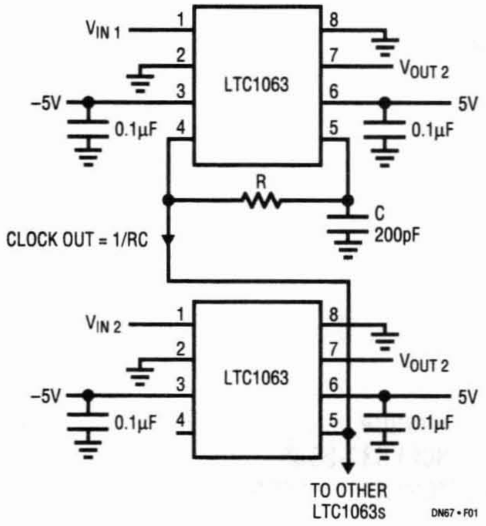

Figure 1. Synchronizing Mulitple LTC1063s

The internal oscillator output is brought out at pin 4 so that it can be used as a synchronized master clock to drive other LTC1063s. Ten or more filters can be locked together to a single LTC1063 clock output as shown in Figure 1.

DC Performance

The LTC1063's output DC offset voltage (typically 1mV or less) is optimized for ±5V supply applications. Output offset is low enough to compete with discrete type RC active filters using low offset op amps. Figures 2a and 2b show an LTC1063 filter operating as a clock-sweepable lowpass filter exhibiting no more than 200µV of total output offset variation over 3 decades of cutoff frequency.

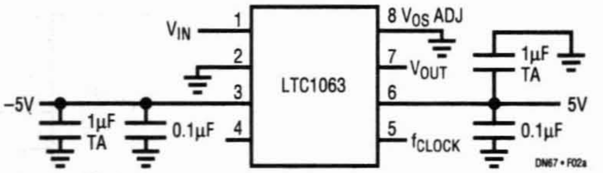

Figure 2a. LTC1063 Operating as a Clock-Sweepable Lowpass Filter

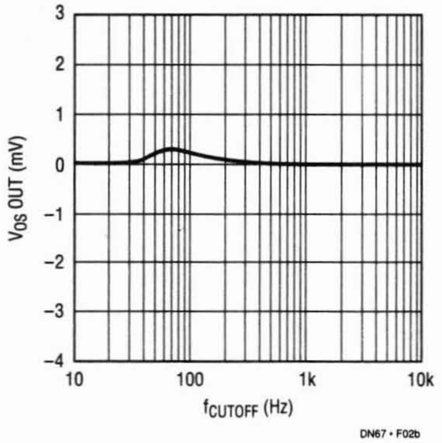

Figure 2b. Output DC Offset vs f_{CUTOFF} for Figure 2a's Circuit

This measurement was taken with a combination of ceramic and tantalum capacitors and a clean PC board layout. DC offset is also affected by input signal DC voltage. The same circuit, Figure 2a, shows a total of 1mV of output offset voltage change with an 8V input change thus, giving a CMRR of 78dB.

Dynamic Range

The LTC1063 has both low noise and very low, 50μV_{RMS}, clock feedthrough. The wideband noise is the integral of the noise spectral density; it is usually expressed in μV_{RMS} and is virtually independent of filter cutoff frequency. The LTC1063 has a wideband noise specification of 90μV_{RMS}. This number is clock frequency and power supply independent.

The LTC1063's AC design however, is based on optimum dynamic range rather than just wideband noise. Dynamic range measurements take into the account the device's total harmonic distortion. Figure 3a shows the typical connection for dynamic range measurement. An inverting buffer is preferred over a unity-gain follower. Large input common-mode signals can severely degrade the distortion performance of noninverting buffers. It is also important to make sure the undistorted op amp swing is equal to or better than that of the filter. Figure 3b shows the device's operating distortion plus noise versus input signal amplitude measured with a standard 1kHz pure sine wave input. The THD improves with increased power supply voltage.

Figure 3b illustrates how the filter can handle inputs to 4V_{RMS} (11.2V_{P-P}) with less than 0.02% THD. At this input level, the dynamic range is only limited by distortion and not by wideband noise. The signal-to-noise ratio at 4V_{RMS} input is 93dB. Optimum signal-to-noise plus distortion according to Figure 3b is 83dB, yet a comfortable 80dB (0.01%) is achieved for input levels between 1V_{RMS} and 2.4V_{RMS}.

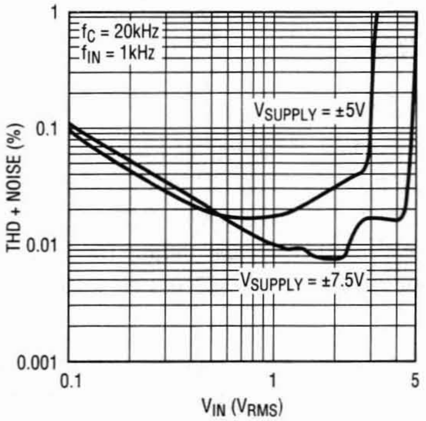

Figure 3b. Plot of Distortion + Noise vs V_{IN}

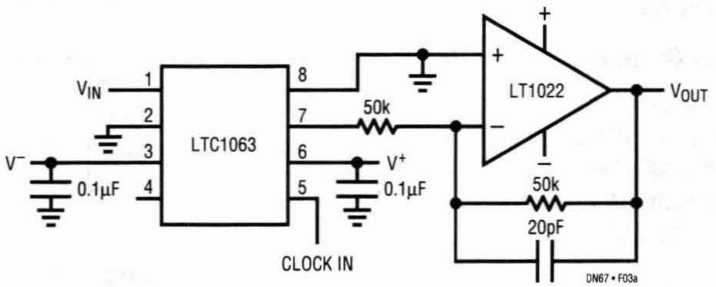

Figure 3a. Typical Connection for Measuring Distortion + Noise and Signal to THD + Noise Ratio

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DESIGN NOTES

New Synchronous Stepdown Switching Regulators Achieve 95% Efficiency – Design Note 68

Brian Huffman and Milt Wilcox

The new LTC1148 and LTC1149 synchronous switching regulator controllers make high efficiency DC/DC conversion possible in a wide range of applications. These controllers share a current-mode architecture which combines synchronous switching for maximum efficiency at high currents with an automatic low current operating mode, called Burst Mode™, which makes 90% efficiencies possible at output currents as low as 10mA.

Figure 1 shows a typical LTC1148 surface mount application providing 5V at 2A from an input voltage of 5.5V to 13.5V. The operating efficiency, shown in Figure 2, peaks at 97% and exceeds 90% from 10mA to 2A with a 10V input. Q1 and Q2 comprise the main switch and synchronous switch, respectively, while inductor current is measured via the voltage drop across current shunt R_{SENSE}. R_{SENSE} is the key component used to set the output current capability according to the formula $I_{OUT} = 100mV/R_{SENSE}$. Advantages of current control include excellent line and load transient rejection, inherent short-circuit protection and controlled startup currents. Peak inductor current is limited to $150mV/R_{SENSE}$ or 3A for the Figure 1 circuit.

The timing capacitor C_T sets the offtime according to the formula $t_{OFF} = 1.3 \times 10^4 \times C_T$. The constant offtime architecture maintains a constant inductor ripple current, while the operating frequency varies with input voltage. The Figure 1 circuit has an offtime of approximately 6µs, resulting in an operating frequency which varies from 60kHz to 90kHz over an 8V to 12V input range.

When the output current drops below approximately $15mV/R_{SENSE}$, the LTC1148 automatically enters Burst Mode™ to reduce switching losses. In this mode, the LTC1148 holds both MOSFETs off and sleeps at 200 µA supply current, while the output capacitor supports the load. When the output capacitor discharges 50mV, the LTC1148 briefly turns back on, or "bursts," to recharge the capacitor. The

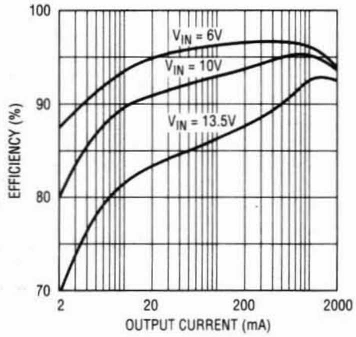
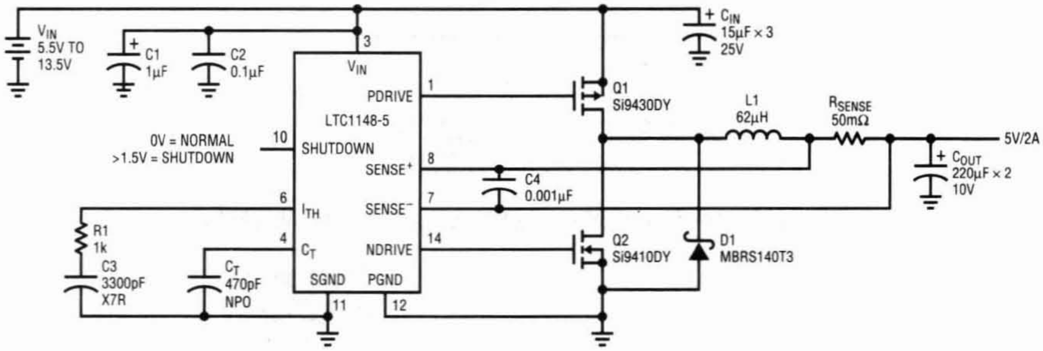


Figure 2. LTC1148-5: 5.5V to 13.5V Efficiency



C1(TA)
C_{IN} AVX (TA) TAJD156K025RLR, ESR = 0.3Ω, I_{RMS} = 0.707A
C_{OUT} AVX (TA) TAJE227K010RLR, ESR = 0.08Ω, I_{RMS} = 1.4A
Q1 SILICONIX PMOS, BVDSS = 20V, RDS_{ON} = 0.1Ω, C_{RSS} = 400pF, Q_G = 50nC
Q2 SILICONIX NMOS, BVDSS = 30V, RDS_{ON} = 0.05Ω, C_{RSS} = 160pF, Q_G = 30nC

D1 MOTOROLA SCHOTTKY, VBR = 40V
R_{SENSE} IRC LR2512-01-R050J P_D = 1W
L1 COILTRONICS CTX62-2-MP, DCR = 0.035Ω, MPP CORE (THROUGH HOLE)
L1-1 COILTRONICS CTX02-11715-2, DCR = 0.11Ω, FERRITE CORE (SURFACE MOUNT)
ALL OTHER CAPACITORS ARE CERAMIC

Figure 1 LTC1148 (5.5V-13.5V to 5V/2A) Surface Mount

Burst Mode™ is a trademark of Linear Technology Corporation.

timing capacitor pin 4, which goes to 0V during the sleep interval, can be monitored with an oscilloscope to observe burst action. You will observe the circuit bursting less and less frequently as the load current is reduced. Complete shutdown reduces the supply current to only 10μA.

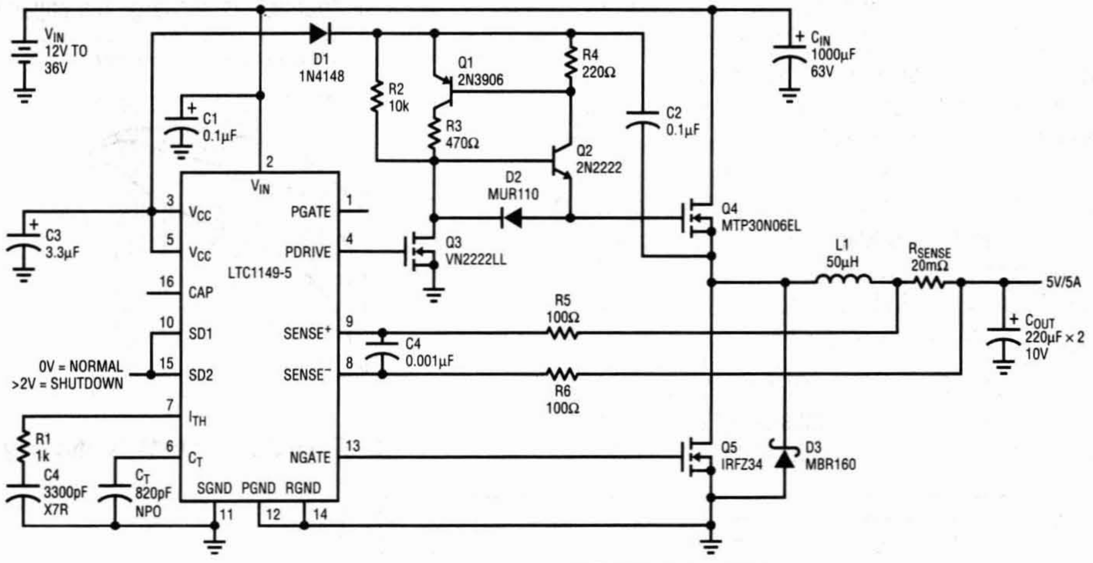
For applications which require greater than 13.5V, the higher voltage LTC1149 includes all of the operating features of the LTC1148 plus an internal regulator and a gate drive level shift circuit which allow operation up to V_{IN} = 48V. The design and performance of an LTC1149 based circuit is similar to that of the Figure 1 LTC1148 circuit, with a slight increase in sleep current (600μA) and shutdown current (150μA) due to the additional LTC1149 high voltage circuitry.

Although highly efficient at output currents of under 2A, P-channel MOSFETs can become a dominate loss element at higher output currents, limiting overall circuit efficiency. Consequently, N-channel MOSFETs are better suited for use in high current applications because they have a substantially lower ON resistance. The circuit shown in Figure 3 utilizes the low loss characteristics of N-channel MOSFETs, providing efficiency in excess of 90% at an output current of 5A.

Figure 3's operation is similar to that of the Figure 1 circuit, but it utilizes an LTC1149, which accommodates higher input voltages, and has been modified to drive the top N-channel MOSFET. The circuit operation is as follows: the LTC1149 provides a PDRIVE output (Pin 4) that swings between ground and 10V which turns Q3 on and off. While Q3 is on, the N-channel MOSFET (Q4) is off because its gate is pulled low by Q3 through D2. During this interval, the NGATE output (pin 13) turns the synchronous switch (Q5) on, creating a low resistance path for the inductor current.

In order to turn Q4 on, its gate must be driven above the input voltage. This is accomplished by bootstrapping capacitor C2 off the source of Q4. The LTC1149 V_{CC} output (pin 3) supplies a regulated 10V output that is used to charge C2 through D1 while Q4 is off. With Q4 off, C2 charges to 5V for the first cycle in Burst Mode™ and 10V thereafter.

When Q3 turns off, the N-channel MOSFET is turned on by the SCR connected NPN-PNP (Q1 and Q2) network. Resistor R2 supplies Q2 with enough base drive to trigger the SCR. Q2 then forces Q1 to turn on which supplies more base drive to Q2. This regenerative process continues until both transistor are fully saturated. During this period, the source of Q4 is pulled to the input voltage. While Q4 is on, its gate source voltage is approximately 10V, fully enhancing the N-channel MOSFET.


VIN 12V TO 36V
D1 1N4148
Q1 2N3906
R4 220Ω
CIN 1000μF 63V
R2 10k
C1 0.1μF
R3 470Ω
C2 0.1μF
Q2 2N2222
D2 MUR110
Q4 MTP30N06EL
VIN
VCC
PGATE
PDRIVE
LTC1149-5
CAP
SD1
SD2
SENSE+
SENSE−
ITH
CT
NGATE
SGND PGND RGND
C3 3.3μF
Q3 VN2222LL
L1 50μH
RSENSE 20mΩ
5V/5A
R5 100Ω
C4 0.001μF
R6 100Ω
COUT 220μF × 2 10V
0V = NORMAL
>2V = SHUTDOWN
R1 1k
C4 3300pF X7R
CT 820pF NPO
Q5 IRFZ34
D3 MBR160
1
2
3
4
5
6
7
8
9
10
11
12
13
14
15
16

C3(TA) LOW ESR
C_{IN} NICHICON (AL) UPL1J102MRH, ESR = 0.027Ω, I_{RMS} = 2.370A
C_{OUT} SANYO (0S-CON) 10SA220M, ESR = 0.035Ω, I_{RMS} = 2.360A
Q1 PNP, BVCEO = 30V
Q2 NPN, BVCEO = 40V
Q3 SILICONIX NMOS, BVDSS = 60V, RDS_{ON} = 5Ω

Q4, Q5 NMOS, BVDSS = 60V, RDS_{ON} = 0.05Ω,
D1, D2 SILICON, VBR = 75V
D3 MOTOROLA SCHOTTKY, VBR = 50V
R_{SENSE} KRL NP-2A-C1-0R020J, P_D = 3W
L1 COILTRONICS CTX50-5-52, DCR = 0.021Ω, IRON POWDER CORE
ALL OTHER CAPACITORS ARE CERAMIC

Figure 3. LTC1149-5 (12V-36V to 5V/5A) Using N-Channel MOSFETs.

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LINEAR TECHNOLOGY
DESIGN NOTES

Low Parts Count DC/DC Converter Circuit With 3.3V and 5V Outputs – Design Note 69

Ron Vinsant

This Design Note describes a simple low cost dual output step-down converter circuit based on the LT1076 five terminal switching regulator.

Performance

Input voltages can range from 8V to 30V. The load range on the 5V is 0.05A to 0.5A while the 3.3V load range is 0.1A to 1A. The circuit is self-protecting under no load conditions; it will "burp" in the same fashion as many off-line flyback power supplies.

Output voltage regulation is excellent. Over all load and line conditions, including cross regulation, the 3.3V output varies from 3.25V to 3.27V. The 5V output varies from 4.81V to 5.19V under the same conditions.

In a typical application of 0.5A on the 3.3V and 0.25A on the 5V, efficiency is typically 76%. With an input voltage of 30V and full load, the efficiency drops to 66%. In normal operating regions efficiency is always better than 70%.

The 5V ripple is less than 75mV and the 3.3V ripple less than 50mV over all line and load conditions.

This design can help save both parts and cost by the elimination of a second regulator. Only a few additional parts are required to make the second output. They are: two resistors, a Schottky diode, a small ceramic capacitor and a filter electrolytic; only 5 additional components! The normal single winding inductor has one small winding added to create the additional output.

Performance Table

V_{IN}	V_{OUT}, OUTPUT 1 (5V)	V_{OUT}, OUTPUT 2 (3.3V)
	@ I_{OUT} = 0.4A	**@ I_{OUT} = 1A**
8V	4.81	3.26
30V	5.07	3.26
	@ I_{OUT} = 0.05A	**@ I_{OUT} = 1A**
8V	5.14	3.25
30V	5.19	3.25
	@ I_{OUT} = 0.4A	**@ I_{OUT} = 0.1A**
8V	4.81	3.26
30V	5.02	3.27
	@ I_{OUT} = 0.05A	**@ I_{OUT} = 0.1A**
8V	5.07	3.26
30V	5.11	3.26

The circuit has been built in our lab and has only been evaluated for room temperature performance. No stability analysis has been done.

Inductor

The inductor is based on a EP-13 ferrite core which is available from a number of vendors. In our breadboard we used a Ferroxcube core in 3C81 material gapped to 6 mils (center gap). The 3.3V winding is 22 turns of #25 AWG while the 5V winding is 13 turns of #28 AWG. Any magnetics vendor should be able to wind this device. The inductor has only a 14°C temperature rise. Coiltronics at (305) 781-8900, or Hurricane Labs at (801) 635-2003 can supply this inductor off the shelf.

Capacitors

Ripple current in the output capacitors C2 and C3 is 250mA$_{RMS}$ total with the input voltage at 30V and maximum load on the two outputs.

The input capacitor (C1), which undergoes higher stress, has a ripple current of 830mA maximum at 14V input and maximum load.

The input and output capacitors have been chosen primarily for ESR, not for voltage. The 50V rating of the capacitors is not due to stress from the circuit but from the fact that the lowest ESR for a particular can size occurs at 50V, in this series of capacitors, from this specific manufacturer.

The capacitors in the frequency compensation network should be at least X7R ceramic, never Z5U, and if broad temperature operation is expected, polyester or polycarbonate film caps should be used.

Layout

In order to achieve proper performance it is important to lay out the circuit as shown in Figure 1. Use a single point ground at the output of the converter as shown. The term "short" indicates that the trace should be as short as possible between the two points shown. These traces should have a minimum width of 0.2" in 2 oz. copper for a length of less than 1.5". Traces longer than this should be avoided on heavier lines of the schematic.

Heat Sinking

Any heat sink of 30°C/W or lower will keep the LT1076 at an acceptable temperature up to a 70°C ambient. See the LT1076 data sheet for further information.

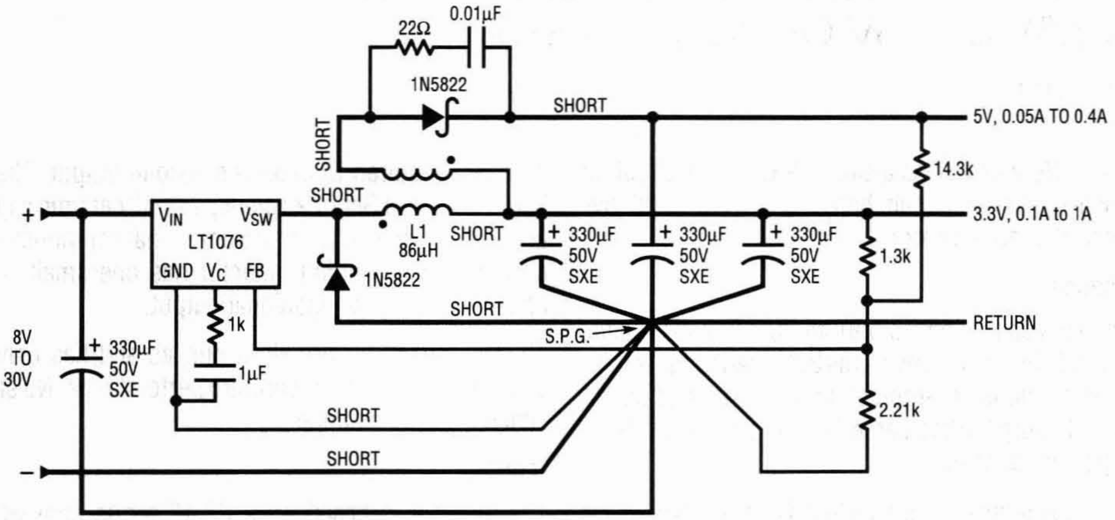
22Ω
0.01μF
1N5822
SHORT
SHORT
5V, 0.05A TO 0.4A
SHORT
14.3k
+
V_{IN}
V_{SW}
LT1076
GND
V_C
FB
L1
86μH
SHORT
330μF
50V
SXE
330μF
50V
SXE
330μF
50V
SXE
3.3V, 0.1A to 1A
1.3k
1N5822
SHORT
RETURN
S.P.G.
1k
8V
TO
30V
330μF
50V
SXE
1μF
SHORT
2.21k
SHORT
–

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Figure 1. 3.3V to 5V Dual Output DC/DC Converter

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SECTION 3: REFERENCE READING

SECTION 3—REFERENCE READING

Avoiding Passsive–Component Pitfalls RR1-1
Analog Signal–Handling for High Speed and Accuracy RR2-1
Prevent Emitter–Follower Oscillation RR3-1

AVOIDING PASSIVE-COMPONENT PITFALLS

The Wrong Passive Component Can Derail Even the Best Op Amp or Data Converter Here Are Some Basic Traps to Watch for.

by Doug Grant and Scott Wurcer

You've just spent $25 or more for a precision op amp or data converter, only to find that, when plugged into your board, the device doesn't meet spec. Perhaps the circuit suffers from drift, poor frequency response, oscillations—or simply doesn't achieve the accuracy you expect. Well, before you blame the device itself, you should examine your passive components—including capacitors, resistors, potentiometers, and yes, even the printed circuit boards themselves. Subtle effects of tolerance, temperature, parasitics, aging, and user assembly procedures can unwittingly sink your circuit. And these effects all too often go unspecified or underspecified by manufacturers.

In general, if you use data converters having 12 bits or more of resolution, or op amps that cost more than $5, you should pay particularly close attention to passive-component selection. To put the problem in perspective, consider the case of a 12-bit digital-to-analog converter (DAC). One half LSB (least-significant bit) corresponds to 0.012% of full scale, or only 122 parts per million (ppm)! The host of passive-component phenomena can quickly accumulate errors far exceeding this level.

Buying the most-expensive passive components won't necessarily solve your problems either. Often, the correct 25-cent capacitor will yield a better-performing, more cost-effective design than the premium-grade $8 part. Although not necessarily easy, understanding and analyzing passive-component effects may prove quite rewarding, once you understand a few basics.

CAPACITORS

Most designers are generally familiar with the range of capacitors available. But the mechanisms by which both static and dynamic errors can occur in precision circuit designs are easy to forget because of the tremendous variety of capacitor types, e.g.: glass, aluminum foil, solid tantalum and tantalum foil, silver mica, ceramic, Teflon, and the film capacitors, including polyester, polycarbonate, polystyrene, and polypropylene types.

Figure 1 is a workable model of a non-ideal capacitor. The nominal capacitance, C, is shunted by a resistance R_p, representing insulation resistance or leakage. A second resistance, R_s—equivalent series resistance, or ESR—appears in series with the capacitor and represents the resistance of the leads and capacitor plates.* Inductance, L—the equivalent series inductance, or ESL, models the inductance of the leads and plates. Finally, resistance R_{da} and capacitance C_{da} together form a simplified model of a phenomenon known as dielectric absorption. Dielectric absorption can ruin the dynamic performance of both fast and slow circuits.

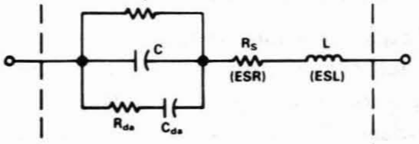

Figure 1. Capacitor equivalent circuit.

Dielectric Absorption

We begin with dielectric absorption, also known as "soakage" and sometimes as "dielectric hysteresis"—perhaps the least understood and potentially most damaging capacitive effect. Upon discharge, most capacitors are reluctant to give up all of their former charge. Figure 2 illustrates the effect. After being charged to V volts at time t_0, the capacitor is shorted by the switch at time t_1. At time t_2, the capacitor is open-circuited; a residual voltage slowly builds up across its terminals and reaches a nearly constant value. This voltage is due to "dielectric absorption."

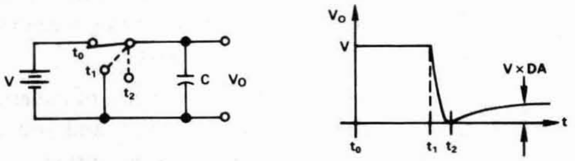

Figure 2. Residual voltage characterizes capacitor dielectric absorption.

Standards techniques for specifying or measuring dielectric absorption are few and far between. Measured results are usually expressed as the percentage of the original charging voltage that reappears across the capacitor. Typically, the capacitor is charged for more than 1 minute, then shorted for an established time between 1 and 10 seconds. The capacitor is then allowed to recover for approximately 1 minute, and the residual voltage is measured (see reference 10).

In practice, dielectric absorption makes itself known in a variety of ways. Perhaps an integrator refuses to reset to zero, a voltage-to-frequency converter exhibits unexpected nonlinearity, or a sample-and-hold exhibits varying errors. This last manifestation can be particularly damaging in a data-acquisition system, where adjacent channels may be at voltages which differ by nearly full scale. Figure 3 illustrates the case in a simple sample-hold.

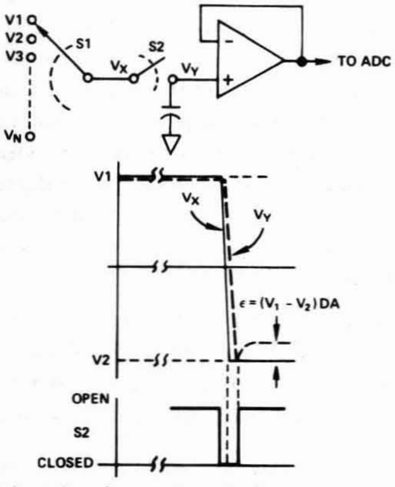

Figure 3. Dielectric absorption induces errors in sample-and-hold application.

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*Capacitor phenomena aren't that easy to separate out. This matching of phenomena and models is for convenience in explanation.

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The dielectric absorption is a characteristic of the dielectric material itself, although it can be affected by inferior manufacturing processes or electrode materials. As a percentage of the charging voltage, dielectric absorption specifications range from a low of 0.02% for Teflon, polystyrene, and polypropylene capacitors to a high of 10% or more for some aluminum electrolytics. For some time-frames, the D.A. of polystyrene can be as low as 0.002%.

Common ceramic and polycarbonate types display typical dielectric absorptions of 0.2%; this corresponds to one-half of an LSB at only 8 bits! Silver mica, glass, and tantalum capacitors typically exhibit even larger dielectric absorptions, ranging from 1.0% to 5.0%, with those of polyester devices falling in the vicinity of 0.5%. As a rule, if your capacitor's spec sheet does not discuss dielectric absorption *in your time frame and voltage range*, exercise caution.

Dielectric absorption can produce long tails in the transient response of fast-settling circuits, such as those found in high-pass active filters or ac amplifiers. In some devices used for such applications, Figure 1's R_{da}-C_{da} model of dielectric absorption can have a time constant of milliseconds.* In fast-charge, fast-discharge applications, the dielectric absorption resembles "analog memory"; the capacitor tries to remember its previous voltage.

In some designs, you can compensate for the effects of dielectric absorption if it is simple and easily characterized, and you are willing to do custom-tweaking. In an integrator, for instance, the output signal can be fed back through a suitable compensation network, tailored to cancel the circuit equivalent of the dielectric absorption by placing a negative impedance effectively in parallel. Such compensation has been shown to improve sample- and-hold circuit performance by factors of 10 or more (Reference 7).

Parasitics and Dissipation Factor

In Figure 1, a capacitor's leakage resistance, R_p, the effective series resistance, R_s, and effective series inductance, L, act as parasitic elements which can degrade an external circuit's performance. The effects of these elements are often lumped together and defined as a dissipation factor, or DF.

A capacitor's leakage is the small current that flows through the dielectric when a voltage is applied. Although modeled as a simple insulation resistance (R_p) in parallel with the capacitor, the leakage actually is nonlinear with voltage. Manufacturers often specify leakage as a megohm-microfarad product, which describes the dielectric's self-discharge time constant, in seconds. It ranges from a low of 1s or less for high-leakage capacitors, such as aluminum and tantalum devices, to the 100's of seconds for ceramic capacitors. Glass devices exhibit self-discharge time-constants of 1,000 or more; but the best leakage performance is shown by Teflon and the film devices (polystyrene, polypropylene), with time constants exceeding 1,000,000 megohm-microfarads. For such a device, leakage paths—created by surface contamination of the device's case or in the associated wiring or physical assembly—can overshadow the dielectric's leakage.

Effective series inductance, ESL (Figure 1) arises from the inductance of the capacitor leads and plates, which, particularly at the higher frequencies, can turn a capacitor's normally capacitive reactance into an inductive reactance. Its magnitude depends on construction details within the capacitor. Tubular wrapped-foil devices display significantly more lead inductance than molded radial-lead configurations. Multilayer ceramic and film-type devices typically exhibit the lowest series impedances, while tantalum and aluminum electrolytics typically exhibit the highest. Consequently, electrolytic types usually prove insufficient for high-speed local bypassing applications.

Manufacturers of capacitors often specify effective series inductance by means of impedance-versus-frequency plots. These show graphically, and not surprisingly, that the devices display predominantly capacitive reactance at low frequencies, with rising impedance at higher frequencies because of their series inductance.

Effective series resistance, ESR (resistor R_s of Figure 1), is made up of the resistance of the leads and plates. As noted, many manufacturers lump the effects of ESR, ESL, and leakage into a single parameter called *dissipation factor*, or DF. Dissipation factor measures the basic inefficiency of the capacitor. Manufacturers define it as the ratio of the energy lost to energy stored per cycle by the capacitor. The ratio of equivalent series resistance to total capacitive reactance—at a specified frequency—approximates the dissipation factor, which turns out to be equivalent to the reciprocal of the figure of merit, Q.

Dissipation factor often varies as a function of both temperature and frequency. Capacitors with mica and glass dielectrics generally have DF values from 0.03% to 1.0%. For ceramic devices, DF ranges from a low of 0.1% to as high as 2.5% at room temperature. And electrolytics usually exceed even this level. The film capacitors usually are the best, with DF's of less than 0.1%.

Tolerance, Temperature, and Other Effects

In general, precision capacitors are expensive and—even then—not necessarily easy to buy. In fact, choice of capacitance is limited by the the range of available values and tolerances. Tolerances of ± 1% for some ceramics and most film-type devices are common, but with possibly unacceptable delivery times. Most film capacitors can be made available with tolerances of less than ± 1%, but on special order only.

Most capacitors are sensitive to temperature variations. Dissipation factor, dielectric absorption, and capacitance itself are all functions of temperature. For some capacitors, these parameters vary approximately linearly with temperature; in others they vary quite nonlinearly. Although not usually important for sample-and-hold applications, an excessively large temperature coefficient (ppm/°C) can prove harmful to the performance of precision integrators, voltage-to-frequency converters, and oscillators. NPO ceramic capacitors, with temperature-drift as low as 30 ppm/°C, usually do the best. On the other hand, aluminum electrolytics' temperature coefficients can exceed 10,000 ppm/°C.

A capacitor's maximum working temperature should also be considered. Polystyrene capacitors, for instance, melt near 85°C, compared to Teflon's ability to survive temperatures up to 200°C.

Sensitivity of capacitance and dielectric absorption to applied voltage can also hurt capacitor performance in a circuit application. Although capacitor manufacturers do not always clearly specify voltage coefficients, the user should always consider the possible effects of such factors. For instance, when maximum voltages are applied, some high-density ceramic devices can experience a decrease in capacitance of 50% or more!

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*Much longer time constants are also quite usual. In fact, some devices can be modeled by several paralleled R_{da}–C_{da} circuits, with a wide range of time constants.

Similarly, the capacitance and dissipation factor of many types vary significantly with frequency, mainly as a result of a variation in dielectric constant. In this regard, the better dielectrics are polystyrene, polypropylene, and Teflon.

Assemble Critical Components Last

The designer's worries don't end with the design process. Commonly used printed-circuit-board assembly techniques can prove ruinous to even the best of designs. For instance, some commonly used p-c board cleaning solvents can infiltrate certain electrolytic capacitors—those with rubber end caps are particularly susceptible. Even worse, some of the film capacitors, polystyrene in particular, actually melt when contacted by some solvents. Rough handling of the leads can damage still other capacitors, creating random or even intermittent circuit problems. Etched-foil types are particularly delicate in this regard. To avoid these difficulties, it may be advisable to mount especially critical components as the last step in the board assembly process—if possible.

Designers should also consider the natural failure mechanisms of capacitors. Metallized film devices, for instance, often self-heal. They initially fail due to conductive bridges that develop through small perforations in the dielectric films. But the resulting fault currents can generate sufficient heat to destroy the bridge, thus returning the capacitor to normal operation (at slightly lower capacitance). Of course, applications in high-impedance circuits may not develop sufficient current to clear the bridge.

Tantalum capacitors also exhibit a degree of self-healing, but—unlike film capacitors—the phenomenon depends on the temperature at the fault location rising slowly. Therefore, tantalum capacitors self-heal best in high impedance circuits which limit the surge in current through the capacitor's defect. Use caution, therefore, when specifying tantalums for high-current applications.

Electrolytic capacitor life often depends on the rate at which capacitor fluids seep through end caps. Epoxy end seals perform better than rubber seals, but an epoxy sealed capacitor can explode under severe reverse-voltage or overvoltage conditions.

RESISTORS AND POTS

Designers have a broad range of resistor technologies to choose from, including carbon composition, carbon film, bulk metal, metal film, and both inductive and non-inductive wire-wound types. As perhaps the most basic—and presumably most trouble-free—of components, the resistor is often overlooked as a potential source of errors in high-performance circuits. Yet, an improperly selected resistor can subvert the accuracy of a 12-bit design by developing errors well in excess of 122 ppm, (½ LSB). When did you last take the time to actually read a resistor data sheet? You'd be surprised at what can be learned from an informed review of the data.

Consider the circuit of Figure 4, which amplifies a 0-to-100-mV input signal 100 times for conversion by a 12-bit ADC with a 0-to-10-volt input range. The gain-setting resistors can be bought in initial tolerances of as low as ±0.001% (10 ppm) in the form of precision bulk metal-film devices. Alternatively, the initial tolerance of the resistors may be corrected through calibration or selection. Consequently, the initial gain accuracy of the circuit can be set to whatever tolerance is required, limited perhaps by the accuracy of calibration instrumentation.

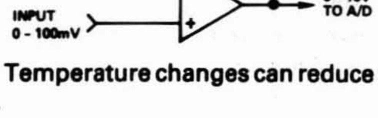

Figure 4. Temperature changes can reduce amplifier accuracy.

Temperature changes, however, can limit the accuracy of the amplifier of Figure 4 in several ways. The absolute temperature coefficients of the resistors are unimportant, as long as they track. Even so, carbon composition resistors, with temperature coefficients of approximately 1,500 ppm/°C, would not suit the application. Even if the tempcos could be matched to an unlikely 1%, the resulting 15 ppm/°C differential would prove inadequate—a shift of as little as 8°C would create a ½-LSB error of 120 ppm.

Manufacturers do offer metal film and bulk metal resistors with absolute temperature coefficients ranging between ±1 and ±100 ppm/°C. Beware, though; temperature coefficients can vary a great deal, particularly among resistors from different batches. To avoid this problem, expensive matched resistor pairs are offered by a few manufacturers, with temperature coefficients that track one another to within 2 to 10 ppm/°C. Low-priced thin-film networks are good and are widely used.

Unfortunately, even matched resistor pairs cannot fully solve the problem of temperature-induced resistor errors. Figure 5a illustrates error-inducing through self-heating. The resistors have identical temperature coefficients but dissipate considerably different amounts of power in this circuit. With an assumed thermal resistance (data sheet) of 125°C/W for ¼-watt resistors, resistor R1's temperature rises by 0.0125°C, while resistor R2's temperature rises by 1.24°C. With a temperature coefficient of 50 ppm/°C, the result is an error of 62 ppm (0.006%).

Even worse, the effects of self-heating create nonlinear errors. In the example of Figure 5a, with half the voltage input, the resulting error is only 15 ppm. Figure 5b graphs the resulting nonlinear transfer function for the circuit of Figure 5a. This is by no means a worst-case example; smaller resistors would give even worse results due to their higher thermal resistance.

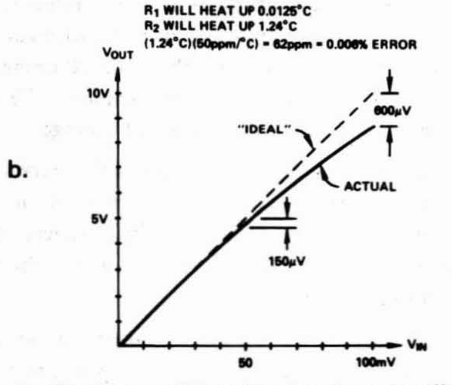
R1
R2
V_X
V_I 0 TO 100mV
V_O = 0 TO 10V
a.
R_1 = 100Ω, ±0.001%, +50ppm/°C
R_2 = 9.9kΩ, ±0.001%, +50ppm/°C
θ_{FA} = 125°C/W
AT V_I = 0V, V_O = 0V, V_X = 0V
P_D IN R_1 = P_D IN R_2 = 0
AT V_I = 100mV, V_O = 10V, V_X = 100mV
P_D IN $R_1 = \frac{(0.10)^2}{100\Omega}$ = 0.1mW
P_D IN $R_2 = \frac{(9.9)^2}{9.9k\Omega}$ = 9.9mW
R_1 WILL HEAT UP 0.0125°C
R_2 WILL HEAT UP 1.24°C
(1.24°C)(50ppm/°C) = 62ppm = 0.006% ERROR
b.
V_{OUT}
10V
5V
"IDEAL"
ACTUAL
600μV
150μV
50
100mV
V_{IN}

Figure 5. Resistor self-heating leads to nonlinear amplifier response. (a) Anatomy of temperature-induced nonlinearity. (b) Nonlinear transfer function (scale exaggerated).

The use of higher-wattage resistors for those devices that dissipate the greatest power can minimize the effects of resistor self-heating. Alternatively, thin- or thick-film resistor networks minimize the effects of self heating by spreading the heat more evenly over all the resistors in a given package.

Often overlooked as a source of error, the temperature coefficient of resistance of typical wire or pc-board interconnects can add to a circuit's errors. Metals used in p-c boards and for interconnecting wires (e.g., copper) have a temperature coefficient as high as 3,900 ppm/°C. A precision 10-ohm, 10 ppm/°C wirewound resistor, with 0.1-ohms of interconnect resistance, for instance, effectively turns into a 45 ppm/°C resistor. The temperature coefficients of interconnects play a particularly significant role in precision hybrids, where thin-film interconnects have non-negligible resistance.

One final consideration applies mainly to designs that see widely varying ambient temperatures: a phenomenon known as temperature retrace describes the change in resistance which occurs after a specified number of cycles of exposure to low and high ambients with constant internal dissipation. Temperature retrace can exceed 10 ppm, even for some of the better metal-film components.

In summary, to design resistance circuits for minimum temperature-related errors, consider the following (along with their cost):

- Closely match resistance-temperature coefficients.
- Use resistors with low absolute temperature coefficients.
- Use resistors with low thermal resistance (higher power ratings, larger cases).
- Tightly couple matched resistors thermally; (use standard resistance networks or multiple resistors in a single package).
- For large ratios, consider using stepped attenuators.

Resistor Parasitics

Resistors can exhibit significant levels of parasitic inductance or capacitance, especially at high frequencies. Manufacturers often specify these parasitic effects as a reactance error, in % or ppm, based on the ratio of the difference between the impedance magnitude and the dc resistance, to the resistance, at one or more frequencies.

Wirewound resistors are especially susceptible to difficulties. Although resistor manufacturers offer wirewound components in either normal or noninductively wound form, even noninductively wound resistors create headaches for designers. These resistors still appear slightly inductive (of the order of 20 μH) for R values below 10,000 ohms. Noninductively wound resistors that exceed 10,000 ohms actually exhibit about 5 pF of shunt capacitance.

These parasitic effects can raise havoc in dynamic circuit applications. Of particular concern are applications using wirewound resistors with values both greater and less than 10,000 ohms. Here it is not uncommon to see peaking, or even oscillation. These effects become evident at frequencies in the low-kHz range.

Even in low-frequency circuit applications, parasitic effects in wire wound resistors can create difficulties. Exponential settling to 1 ppm takes 20 time constants or more. Parasitics associated with wire wound resistors can increase settling time beyond the length of those time constants significantly.

Unacceptable amounts of parasitic reactance are often found even in resistors that aren't wirewound. For instance, some metal-film types have significant interlead capacitance, which shows up at high frequencies. Carbon resistors do the best at high frequencies.

Thermoelectric Effects

The junction between any two dissimilar metals creates a thermal EMF. In many cases, it can easily produce the dominant error in a precision circuit design. In wire wound resistors, for instance, the resistance wire generates a thermal EMF of 42 microvolts/°C when joined to the leads (A typical lead material is Alloy 180, consisting of 77% copper and 23% nickel). If the resistor's two terminations see the same temperature, the EMFs cancel and no net error results. However, if the resistor is mounted vertically a temperature gradient may exist between the bottom and top of the resistor because of air flow past the long lead and its lower heat capacity.

For a temperature difference of as little as 1°C, an error voltage of 42 microvolts results, a level which easily overwhelms the 25-microvolt offsets of typical precision op amps! A horizontally mounted resistor (Figure 6) can resolve the difficulty. Alternatively, some resistor manufacturers offer, on special order, tinned copper leads, which reduce the thermal EMF to 2.5 microvolts/°C.

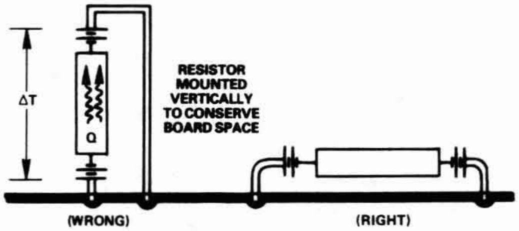

Figure 6. Thermal gradients create significant thermoelectric circuit errors.

In general, designers should strive to avoid thermal gradients on or near critical circuit boards. Often this means thermally isolating components that dissipate significant amounts of power. Thermal turbulence created by large temperature gradients can also result in dynamic noise-like low-frequency errors.

Voltage, Failure, and Aging

Resistors are also plagued by changes as a function of applied voltage. The deposited-oxide high-megohm type components are especially sensitive, with voltage coefficients ranging from 1 ppm/volt to more than 200 ppm/volt. This is another reason to exercise caution in precision applications, such as high-voltage dividers.

Resistors' failure mechanisms can also create circuit difficulties if not carefully considered. Carbon-composition resistors fail safely by turning into open circuits. Consequently, in some applications, these components play a useful secondary role as a fuse. Replacing such a resistor with a carbon-film type can lead to trouble, since carbon-film devices can fail as short circuits. (Metal-film components usually fail as open circuits.)

All resistors tend to change slightly in value with age. Manufacturers specify long-term stability in terms of change—ppm/year. Values of 50 or 75 ppm/year are not uncommon among metal film resistors. For critical applications, metal-film devices should be burned-in for at least one week at rated power. During burn-in, R values can shift by up to 100 or 200 ppm. Metal film resistors may need 4,000 or 5,000 operational hours for full stabilization, especially if they are deprived of a burn-in period.

Resistor Excess Noise

Most designers have some familiarity with thermal, or Johnson, noise in resistors. But a less widely recognized second noise phenomenon, called excess noise, can prove particularly troublesome in precision op amp and converter circuits. Excess noise becomes evident only when current passes through a resistor.

To review briefly, thermal noise results from the thermally induced random vibration of charge carriers in a resistor. Although the average current from these vibrations remains zero, instantaneous charge motions result in an instantaneous voltage across the resistor's terminals.

Excess noise, on the other hand, occurs primarily when dc flows in a discontinuous medium, such as a carbon composition resistor. The current flows unevenly through the compressed carbon granules, creating microscopic particle-to-particle "arcing". The phenomenon gives rise to a 1/f noise-power spectrum, in addition to the thermal noise spectrum. In other words, the excess spot noise voltage increases as the inverse square-root of frequency.

Excess noise often surprises the unwary designer. Resistor thermal noise and op amp noise set the noise floor in typical op-amp circuits. Only when voltages appear across input resistors and cause current to flow does the excess noise become a significant—and often dominant—factor. In general, carbon composition resistors generate the most excess noise. As the conductive medium becomes more uniform, excess noise becomes less significant. Carbon film resistors do better, and metal film resistors do better yet.

Manufacturers specify excess noise in terms of a noise index—the number of microvolts of rms noise in the resistor in each decade of frequency per volt of dc drop across the resistor. The index can rise to 10dB (3 microvolts per dc volt per decade of bandwidth) or more. Excess noise is most significant at low frequencies. Above 100 kHz, thermal noise predominates.

Potentiometers

Trim potentiometers can suffer from most of the phenomena that plague fixed resistors. Users must also remain vigilant against additional hazards unique to these components.

For instance, many trim potentiometers are not sealed and can be severely damaged by board-washing solvents, and even by excessive humidity. Vibration—or simply extensive use—can damage resistive-element and wiper terminations. Contact noise, tempcos, parasitic effects, and limitations on adjustable range can all hamper circuit operation. Furthermore, the limited resolution of wirewound types and the hidden limits to resolution in cermet and plastic types (hysteresis, incompatible material tempcos, slack) make the obtaining and maintaining of precise settings anything but an "infinite resolution" process. Rule: Use infinite care and infinitesimal adjustment range to avoid infinite frustration.

PRINTED-CIRCUIT BOARDS

Printed-circuit boards act as "unseen components" in all precision circuit designs. Since designers rarely consider the electrical characteristics of PC boards as additional circuit components, the circuit's performance usually ends up worse than predicted.

Printed-circuit-board effects that are harmful to precision circuit performance include leakage resistances, voltage drops in ground foils, stray capacitances, dielectric absorption and related "hook" (a salient feature of the circuit's step-response waveform). In addition, the tendency of p-c boards to absorb atmospheric moisture ("hygroscopicity") means that changes in humidity often cause the contributions of some parasitic effects to vary from day to day.

In general, printed-circuit-board effects can be divided into two categories—those that most noticeably affect the static or dc operation of the circuit, and those that most noticeably affect dynamic or a-c circuit operation.

Static PC-Board Effects

Leakage resistance is the dominant static circuit board effect. Contamination of the board's surface, in the form of flux residues, deposited salts, and other debris can create leakage paths between circuit nodes. Even on well cleaned boards, it is not unusual to find 10 nA or more of leakage to nearby nodes from 15-volt supply rails.* Nanoamperes of leakage current into the wrong nodes often cause volts of error at a circuit's output; for example, 10 nA into a 10-megohm resistance causes 0.1 V of error.

To identify nodes sensitive to the effects of leakage currents, ask the simple question: If a spurious current of a few nanoamperes or more were injected into this node, would it matter?

If the circuit is already built, you can localize moisture sensitivity to a suspected node with a classic test. While observing the circuit's operation, blow on potential trouble spots through a simple soda straw. The soda straw focuses the breath's moisture, which, with the board's salt content in susceptible portions of the design, disrupts circuit operation upon contact.

There are several means of eliminating simple surface leakage problems. Thorough washing of circuit boards to remove residues helps considerably. A simple procedure includes vigorously brushing the boards with isopropyl alcohol, followed by a thorough washing with deionized water and an 85°C bakeout for a few hours. Be careful when selecting board-washing solvents, though. If cleaned with Freon-based solvents, some water-soluble fluxes create salt deposits, exacerbating the leakage problem.

Unfortunately, if a circuit displays a sensitivity to leakage, even the most rigorous cleaning can offer only a temporary solution. Problems soon return upon exposure to handling, foul atmospheres, and high humidity. *Guarding*, on the other hand, offers a fairly reliable and permanent solution to the problem of surface leakage. Well-placed guards can eliminate leakage problems, even for circuits exposed to harsh industrial environments.

Guarding principles are simple: Surround sensitive nodes with conductors that can readily sink stray currents, and maintain those conductors at the exact potential of the sensitive node. The guard potential must be maintained close to the potential of the sensitive node, otherwise the guard will serve as a source rather than a sink. For example, to keep the leakage current into a node below a picoampere, assuming 1000-megohm leakage resistance, the guard and the node must be within 1.0 millivolts of one another.

Figures 7a and 7b illustrate the guarding principle as applied to typical inverting and non-inverting op-amp applications. Figure 7c illustrates an actual circuit-board layout for a guard. Note that, to be most effective, the guard pattern should appear on both sides of the circuit board. Try to include the guards when first laying out a new board pattern, from the beginning of the layout process. At later stages, there is usually insufficient space left to locate them optimally—if at all.

Dynamic PC-Board Effects

Although static pc board effects can come and go with changes in humidity or board contamination, problems that most noticeably

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*Unfortunately, the standard op-amp pinout places the − 15V supply pin right next to the + input, which is often hoped to be at high impedance.

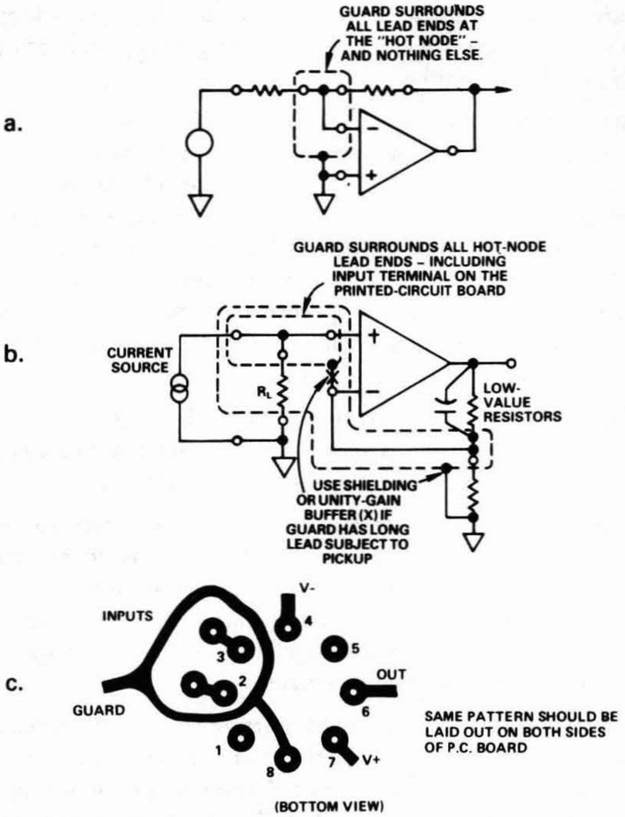
GUARD SURROUNDS ALL LEAD ENDS AT THE "HOT NODE" – AND NOTHING ELSE.
a.
GUARD SURROUNDS ALL HOT-NODE LEAD ENDS – INCLUDING INPUT TERMINAL ON THE PRINTED-CIRCUIT BOARD
b.
CURRENT SOURCE
R_L
LOW-VALUE RESISTORS
USE SHIELDING OR UNITY-GAIN BUFFER (X) IF GUARD HAS LONG LEAD SUBJECT TO PICKUP
c.
INPUTS
GUARD
V-
OUT
V+
1
2
3
4
5
6
7
8
SAME PATTERN SHOULD BE LAID OUT ON BOTH SIDES OF P.C. BOARD
(BOTTOM VIEW)

Figure 7. Proper circuit guarding resolves both static and dynamic pc-board induced errors. (a) Use of guard in inverting application. (b) Use of local guard in non-inverting application. Voltage buffer would help in guarding cable. (c) Printed-circuit board guard pattern for op amp.

affect the dynamic performance of a circuit usually remain relatively constant. Short of a new design, they can't be fixed by washing or any other simple fixes. As such, they can permanently and adversely affect a design's specifications and performance.

The problems of stray capacitance, linked to lead and component placement, are reasonably well known to most circuit designers. Since lead placement can be permanently dealt with by correct layout, any remaining difficulty is solved by training assembly personnel to orient components or bend leads in an optimal way.

Dielectric absorption, on the other hand, represents a more troublesome and still poorly understood circuit-board phenomenon. Like dielectric absorption in capacitors, dielectric absorption in a printed-circuit board can be modeled by a series resistor and capacitor connecting two closely spaced nodes (Figure 8). Its effect is inverse with spacing and linear with length. The model's effective capacitance ranges from 0.1 to 2.0 pF, with the resistance ranging from 50 to 500 MΩ. Values of 0.5 pF and 100 MΩ are most common. Consequently, circuit-board dielectric absorption interacts the most with high-impedance circuits.

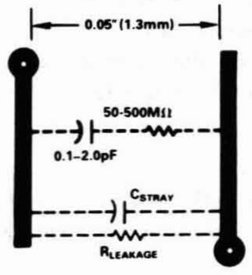

Figure 8. Dielectric absorption plagues dynamic response of pc-based circuits.

Such dielectric absorption most noticeably influences dynamic circuit response, for example, settling time. Unlike circuit leakage, the effects are not usually linked to humidity or other environmental conditions, but rather, are a function of the board's dielectric properties. The chemistry involved in producing plated-through holes seem to exacerbate the problem. If your circuits do not meet expected transient response specs, you should consider circuit-board dielectric absorption as a possible cause.

Fortunately, there are solutions. As in the case of capacitor dielectric absorption, external components can be used to compensate for the effect. More importantly, surface guards that totally isolate sensitive nodes often completely eliminate the problem (The guards must be duplicated on both sides of the board).

Circuit-board "hook", similar if not identical to dielectric absorption, is characterized by a variation in effective circuit-board capacitance with frequency. In general, it affects the transient response of high-impedance circuits where the board's capacitance is an appreciable portion of the total circuit capacitance. Circuits operating at frequencies below 10 kHz are the most susceptible. As in circuit-board dielectric absorption,the board's chemical makeup very much influences its effects.

DON'T OVERLOOK ANYTHING

Remember, if your precision op-amp or data-converter-based design does not meet specs, try not to overlook anything in your efforts to find the error sources. Analyze both active and passive components, and try to identify and challenge any assumptions or preconceived notions that may blind you to the facts. Take nothing for granted.

For example, when not tied down to prevent motion, cable conductors, moving within their surrounding dielectrics, can create significant static charge buildups that cause errors, especially when connectd to high-impedance circuits. Rigid cables, or even costly low-noise Teflon-insulated cables, are an expensive alternative.

As more high-precision op amps and higher resolution data converters become available, and system designs call for higher speed and accuracy, a thorough understanding of the error sources described in this article becomes more important. ▶

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10. Specification MIL C-19978D: *Capacitor, fixed, plastic (or paper and plastic) dielectric, general specification for.*

ANALOG SIGNAL-HANDLING FOR HIGH SPEED AND ACCURACY

You're Paying for Accuracy in IC Converters; Don't "Blow It" in the Analog Circuit Wiring

by A. Paul Brokaw

You've bought an IC a/d or d/a converter that's specified for 10-bit-and-better resolution and accuracy. Or, you've bought a current-ouput DAC with submicrosecond settling to 1/2 LSB. Much design effort, technological development, and process competence have been expended to solve the hardest part of your interface problem. But . . . you aren't out of the woods yet! Here are some of the issues that you will have to come to grips with to preserve speed, resolution, and accuracy:

1. If your DAC is a current-output type and you want voltage, the use of an op amp requires that you deal with the dynamic and steady-state signal-interfacing problems.
2. You will have to minimize interference introduced via common power-supply connections.
3. You will have to decide where "ground" should be and how to keep it there.
4. If "ground" is remote, you will have to couple to it without reduced accuracy or succumbing to interference.
5. If your analog signal is being converted by a successive-approximations converter, you may have to buffer the source from fast transients incidental to conversion.

To become aware of these potential problems is to have taken the first step towards solving them. Since all circuits and systems differ in important little ways, there are no"cook-book" solutions that can be blithely employed for satisfactory results in all cases. However, a little thought will go a long way towards solving them. The purpose of this Brief is to remind you of some of the things you should be thinking about.

DAC's AND OP AMPS – DYNAMIC PROBLEMS

A current-output DAC is usually connected to the summing point of an inverting op amp, and then the feedback loop is closed via the internal "span" resistor, R_F, as Figure 1 shows. The output impedance of the DAC can generally be treated as a parallel combination of resistance and capacitance. The shunt capacitance, C_O, combines with R_F to add a pole to the open-loop response, which may result in poor closed-loop response.

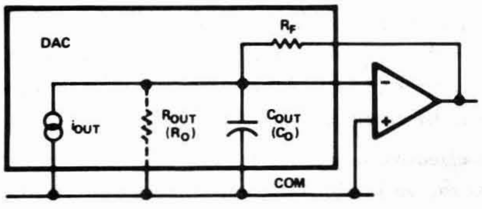

Figure 1. Equivalent circuit of current-output DAC.

Figure 2 shows how the open-loop amplitude and phase response might appear if the spurious pole due to C_O is below the undisturbed system-crossover frequency. Not only will the closed-loop bandwidth be reduced, but –more seriously– excess phase shift will be introduced. The extra phase shift reduces the system frequency stability margins and may cause ringing (and perhaps even oscillation).

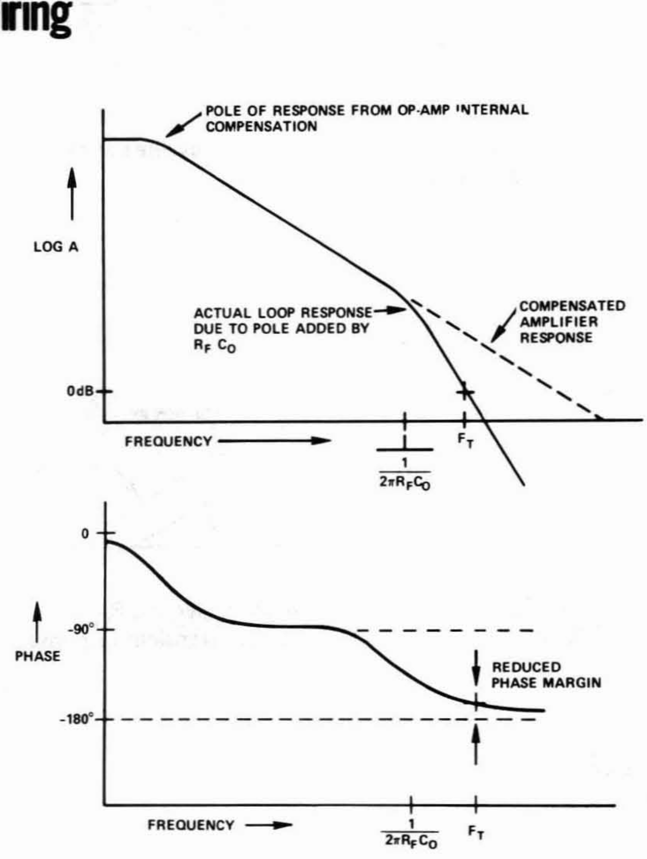

Figure 2. Amplitude and phase response of the circuit of Figure 1. The additional pole increases settling time by reducing bandwidth and increasing both overshoot and ringing.

As Figure 3a shows, the loop-stability margins can be restored by connecting a feedback capacitor, C_F, in parallel with the feedback resistor. This capacitance creates a zero in the open-loop transfer function, which can be adjusted to correct the phase margin. However, if R_{OUT} is very large (as is often the case with current-output DAC's), the large pole-zero mismatch remaining (Figure 3b) may result in slow settling.

Even with finite values of R_{OUT}, a small residual pole-zero mismatch (Figure 3c) may result in long-settling "tails"; the DAC output voltage may appear to settle quickly, but then it slowly changes –by a significant amount– to its final value, over the course of tens of microseconds, or even milliseconds.[1]

The residual mismatch will be eliminated when the DAC-output circuit and the feedback network form a frequency-compensated voltage divider, i.e., when $R_O C_O = R_F C_F$. This condition can usually be satisfied, but sometimes it requires large values of C_F. Unfortunately, C_F–which introduces an open-loop zero–also produces a closed-loop pole, which reduces the overall bandwidth and results in increased settling time.

R_F is generally fixed by the desired DAC gain; the minimum value of C_O is a property of the converter not under the system-

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[1] This process is discussed in some detail, with waveforms, in the Appendix to an article, "Settling Time of Operational Amplifiers," by Bob Demrow, appearing in ANALOG DIALOGUE 4-1 (1970).

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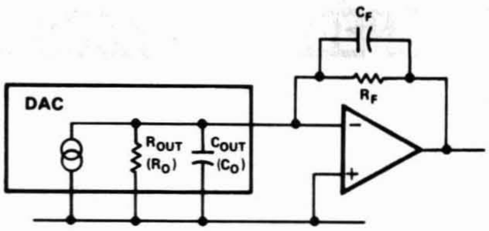

Figure 3a. Improving loop stability by the use of feedback capacitance, C_F.

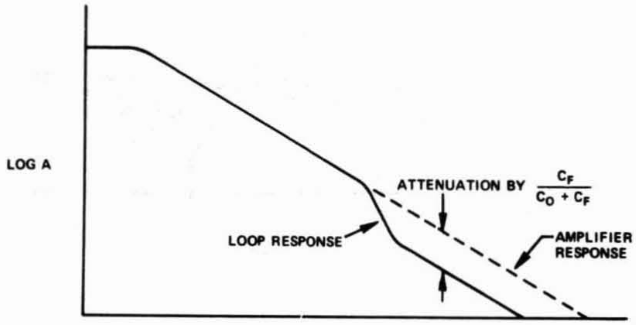

Figure 3b. Response of circuit 3a, neglecting R_{OUT}. Pole-Zero mismatch may yield poor transient response.

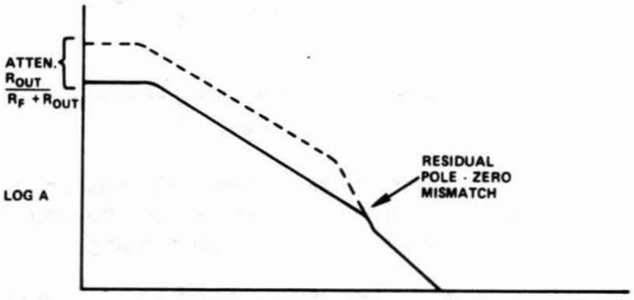

Figure 3c. Response of circuit 3a with finite R_{OUT}.

designer's control. Therefore, C_F and R_O are the only two parameters that can be manipulated (reduced). As R_O' (the effective value of R_O) is reduced by shunting the DAC output with a resistor, the required value of C_F is reduced, and the closed-loop bandwidth is increased (Figure 4). The unity-gain bandwidth of the op amp, b, limits the open-loop system bandwidth, which, in turn, limits the realization of closed-loop bandwidth. As R_O' is reduced, the *open-loop* bandwidth obtainable for a fixed op-amp bandwidth, b, is also reduced.

A compromise can be reached by adjusting R_O' to provide the same open- and closed-loop bandwidth. For a fixed C_O and R_F, the values of R_O' and C_F can be determined from:

$$R_O' C_O = R_F C_F = \frac{1 + \sqrt{1 + 8b\pi R_F C_O}}{4b\pi} \qquad (1)$$

The resistive component at the DAC output also influences the effect ot the amplifier offset (V_{OS}) and noise on the overall output voltage. Both are magnified by $(1 + R_F/R_O)$.

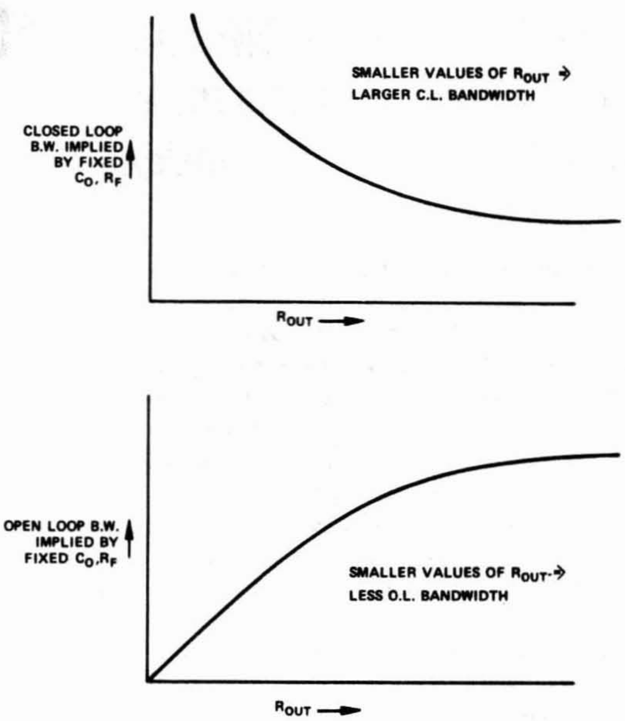

Figure 4. Effect of varying R_{OUT} (R_O') on open-loop and closed-loop bandwidth.

DAC's AND OP AMPS - NULLING PROBLEMS

Perhaps the best way to control V_{OS} in an op amp used with a DAC is at the source—to choose an op amp with sufficiently low offset over the temperature range (such as the AD510). The next-best way is to null the op-amp's offset by the standard V_{OS} trim, taking pains to connect the pot wiper to the appropriate supply terminal *at the device.*[2] The amplifier's offset-trim adjustment should be used *only* for V_{OS} nulling; if it is used to compensate for offsets caused by the flow of bias current through the feedback resistor, as well as for offsets occurring in external circuitry, the amplifier input stage will have to be unbalanced, which will cause its V_{OS} tempco to be degraded.

If the amplifier lacks offset-adjust terminals, or if it is necessary to compensate for the additional sources of offset mentioned above in one convenient place, there are two commonly used ways of providing the trim; they are shown in Figure 5. The more-desirable approach is shown in 5a; the correction is applied to the amplifier's positive input terminal, as a voltage. Since it is effectively in series with V_{OS}, the V_{OS} correction is unaffected by changes of R_O'.

The less-effective way is to introduce a current at the summing point, as shown in 5b. If the resistances in the circuit (including R_O') are constant, there is no problem. However, if R_O' can vary, the output offset will change. If the change of R_O' is a function of the applied *digital code*, the result can be increased differential nonlinearity.

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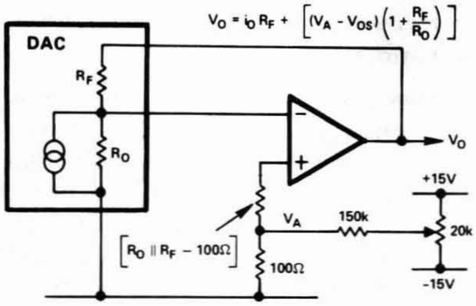
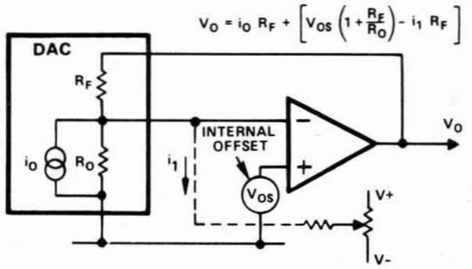
[2] The reasons for this are well-documented in the Application Note, "An IC-Amplifier User's Guide to Decoupling, Grounding, and Making Things Go Right for a Change," by the author, available from Analog Devices. A heavily edited version appeared in EDN Magazine, October 5, 1975.


$V_O = i_O R_F + \left[(V_A - V_{OS})\left(1 + \frac{R_F}{R_O}\right)\right]$
DAC
R_F
R_O
V_O
+15V
V_A
150k
20k
$[R_O \parallel R_F - 100\Omega]$
100Ω
-15V

(a) Nulling offset with voltage applied to op-amp reference input.


$V_O = i_O R_F + \left[V_{OS}\left(1 + \frac{R_F}{R_O}\right) - i_1 R_F\right]$
DAC
R_F
i_O
R_O
i_1
INTERNAL OFFSET
V_{OS}
V_O
V+
V-

(b) Nulling offset with current added at op-amp summing point.

Figure 5. External offset-null methods.

For example, if the DAC is an inverted R-2R-ladder type, as shown in Figure 6, the output resistance, R_O, approaches R for codes containing many 1's, 3R for codes containing a single 1, and ∞ for all-0's. If R = 10kΩ, the resistance looking back into the network is about 10kΩ for more than four 1's and 30kΩ for a single 1. Thus, for the one-bit transition from 0011111111 to 0100000000, the error voltage, $V_{OS}(1 + R_F/R_O)$, changes from 2 V_{OS} to $(4/3)V_{OS}$. If the offset had been nulled at all-0's ($1 + R_F/R_O = 1$, since $R_O \rightarrow \infty$), the offset error will be $+V_{OS}$ at the first code and $(+1/3)V_{OS}$ at the second code; the incremental change of error will be $(-2/3)V_{OS}$. If V_{OS} is not much smaller than the voltage equivalent of the least-significant bit, a tangible error will result. It will be especially pernicious in the case of a multiplying-DAC application with small analog inputs. The solution is simple: use Figure 5a instead of 5b.

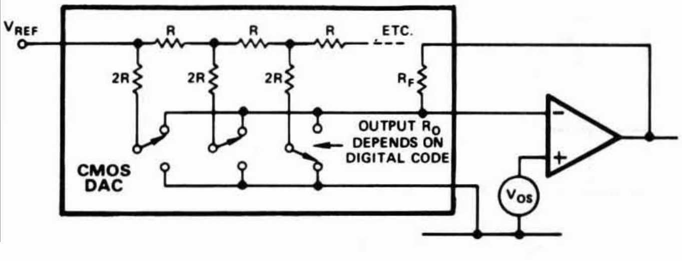

V_{REF}
R
R
R
ETC.
2R
2R
2R
R_F
OUTPUT R_O DEPENDS ON DIGITAL CODE
CMOS DAC
V_{OS}

Figure 6. Variable output resistance of inverted R-2R ladder in CMOS and voltage-switching DAC's.

"Foreign" currents in common ground and power lines can introduce offset, noise, and other errors that will be amplified in the same way as V_{OS} errors. It is important to refer the amplifier circuit (and its external V_{OS} trim), the load across which the output voltage is developed, and the DAC's reference input — all of these — to the DAC terminals, in the manner shown in Figure 7.

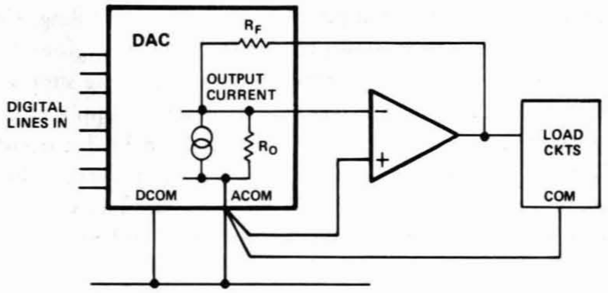

DAC
R_F
OUTPUT CURRENT
DIGITAL LINES IN
R_O
DCOM
ACOM
LOAD CKTS
COM

Figure 7. Referring buffer amplifier and load circuits to analog common.

BYPASSING AND DECOUPLING

In "virtual-ground" systems, such as an op amp, driven by a current-output DAC, the DAC output current doesn't actually return to ground, but to one of the power supplies, by way of the op amp's output stage (Figure 8). To reduce the impedance in the high-frequency current path, the bypass capacitor should be connected so as to return the currents from one (or both) power terminals to ground *at the DAC.* If the DAC output is active, it may require bypassing of its own supplies for the same reason.

> WARNING: You and your drafting department may have conflicting objectives. Your objective is to design circuits that work and to communicate the important details to whoever assembles them. Your drafting department (or so it may seem) has the objective of drawing nice, neat, squared-off diagrams, in which the lines representing conductors are nicely equipotential. You may have noticed that, in Figures 7 and 8, these niceties have been avoided. The lines are configured to resemble closely the job that the wires perform, converging at the common analog connection. Again, the bypass-capacitor lead, in Figure 8, wends its way purposefully around the op amp's acute angle to its power-supply terminal, rather than shooting straight up to meet the power-supply line (a sure recipe for costly debugging). If you think your drafting depart-

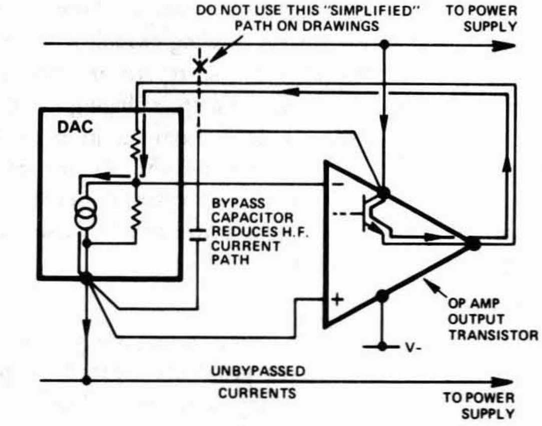
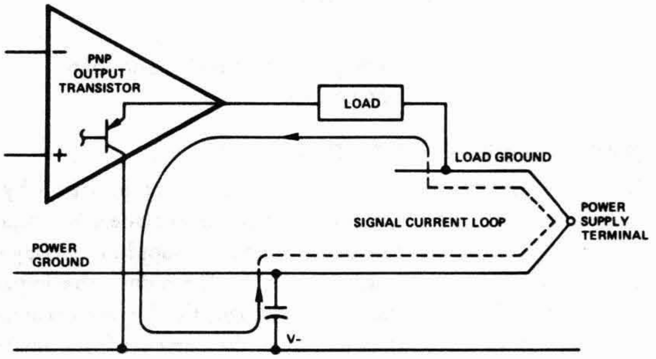

DO NOT USE THIS "SIMPLIFIED" PATH ON DRAWINGS
TO POWER SUPPLY
DAC
BYPASS CAPACITOR REDUCES H.F. CURRENT PATH
OP AMP OUTPUT TRANSISTOR
V-
UNBYPASSED CURRENTS
TO POWER SUPPLY

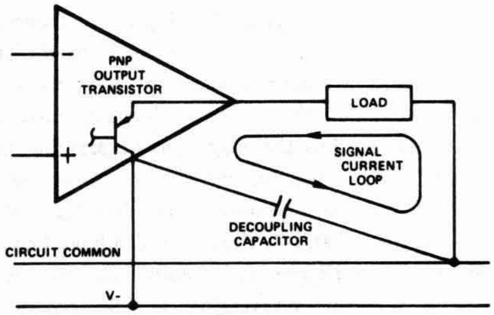
Figure 8. Bypassing power supplies for virtual-ground applications. Arrows show unbypassed current flow.

ment may have a mind of its own, you may want to include a special message for the person who builds the circuit to be sure that it gets built the way you want it built.

Figure 9a shows an example of ineffective decoupling. Here, the op amp drives a load, which connects to a long ground line (returning to the power-supply terminal), and the supply-decoupling for the amplifier returns to the power supply through another long line. The return path for the load current is as long as, or longer than, the supply lines powering the op amp. The "local" decoupling is not only ineffective; it may actually contribute to noise on the power-ground bus.


PNP
OUTPUT
TRANSISTOR
LOAD
LOAD GROUND
SIGNAL CURRENT LOOP
POWER
SUPPLY
TERMINAL
POWER
GROUND
V-

(a) Decoupling for negative supply ineffective.


PNP
OUTPUT
TRANSISTOR
LOAD
SIGNAL
CURRENT
LOOP
DECOUPLING
CAPACITOR
CIRCUIT COMMON
V-

(b) Decoupling negative supply optimized for "grounded" load

Figure 9. Effective and ineffective decoupling.

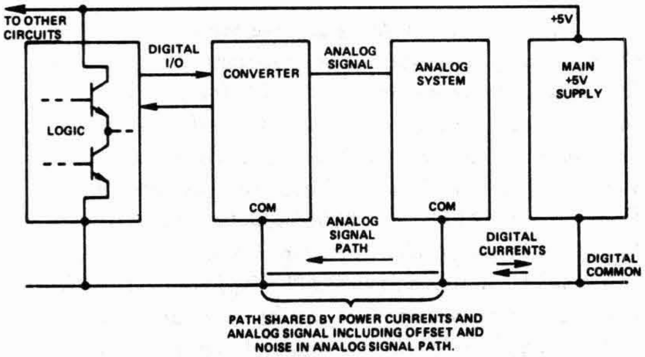
The cardinal rule of decoupling is: *Make it easy for the current to get back by the shortest path.* Figure 9b shows a more-effective scheme, in which the decoupling capacitor connects by the shortest path between the load return and the load-voltage control element. Here, an op amp, swinging a resistive load-circuit negative, drives the load from an internal PNP transistor, connected to V–. Decoupling the V– pin of the op amp to the low side of the load provides the most direct return path for high-frequency currents, and bypasses them around ground and power buses.

GROUNDING

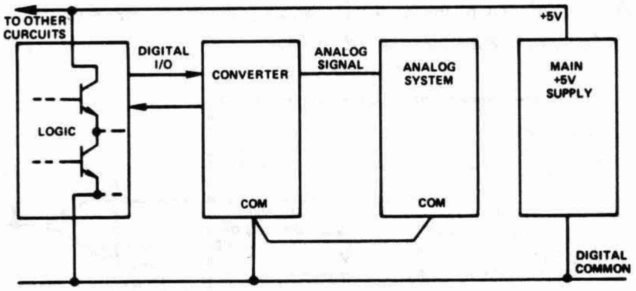
Great amounts of effort, and many decoupling components, are spent in the attempt to correct problems created by poor ground-current management. In large systems, and in systems which deal with both high-level and low-level signals, "ground" (or common bus) management becomes an important aspect of design. The worst sin— allowing low-level analog signals to share conductors with logic returns or power connections— is an invitation to trouble.

Figure 10a shows an example of a path, shared by digital and analog signals, between the common connections of a converter and an analog system. If the least-significant bit is worth 2.5mV, and digital on-off current fluctuations of the order of 100mA are flowing an a lead with 0.1Ω resistance, the resulting 4-LSB uncertainty (not including spikes and glitches) suggests that it would be folly to waste money on a 12-bit converter, when 10-bit resolution is the very best that can be hoped for, because of wiring limitations.

As Figure 10b shows, in concept, an analog subsystem can be locally interconnected, with a single-wire connection to the digital common. This signal connection carries only the digital currents required for the *converter's* digital interface. Moreover, analog signals are not forced to share a conductor, even with those currents. The analog subsystem should be powered by a supply with a local common return, which may be connected to the digital common but does not share any current-carrying conductors. Ideally, there are no "foreign currents" flowing between the analog system and the digital system, except for those within the converter. If the two systems are joined only at the converter, the foreign currents share the shortest path, and their effect is minimized.


TO OTHER
CIRCUITS
+5V
DIGITAL
I/O
CONVERTER
ANALOG
SIGNAL
ANALOG
SYSTEM
MAIN
+5V
SUPPLY
LOGIC
COM
COM
ANALOG
SIGNAL
PATH
DIGITAL
CURRENTS
DIGITAL
COMMON
PATH SHARED BY POWER CURRENTS AND
ANALOG SIGNAL INCLUDING OFFSET AND
NOISE IN ANALOG SIGNAL PATH.

(a) Shared path produces interference and errors.


TO OTHER
CURCUITS
+5V
DIGITAL
I/O
CONVERTER
ANALOG
SIGNAL
ANALOG
SYSTEM
MAIN
+5V
SUPPLY
LOGIC
COM
COM
DIGITAL
COMMON

(b) This connection minimizes common impedance between analog and digital (including converter digital currents).

Figure 10. Proper and improper grounding.

In practical systems, it is often impossible to avoid multiple foreign-current paths. In systems which include several d/a and a/d converters, for example, each converter is a path for digital currents, yet it must have access to the analog signal common. Frequently, the ground problem in such systems can be treated by using an analog common which handles *only* analog signal returns - and a separate system of returns for all digital or high-level signals (Figure 11). Occasionally, a third system of analog power commons may be used to advantage. Since the analog common must be connected to the digital common at no more than one point, safety diodes should be added to any modularized system. These diodes prevent large voltages from developing between ground systems if the key grounding unit, or "Mecca", should be removed from the system.

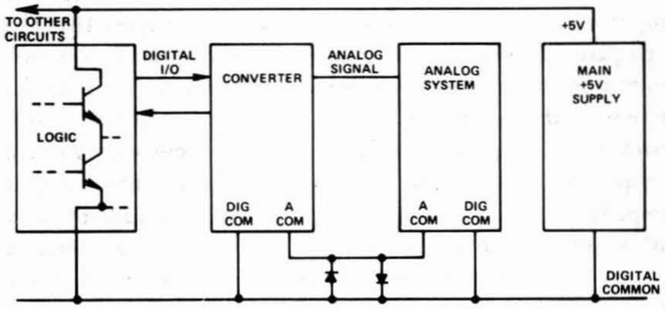


Figure 11. Improved ground current management (analog and digital common must be joined in either converter or analog system. Diodes are fault protection if this connection is broken.)

WHEN COMMON GROUND IS IMPRACTICAL

In large systems, it is often impractical to rely on a single common point for all analog signals. In these cases, some form of differential (or even *isolation*) amplifier is required to translate signals between ground systems. For the inveterate op-amp user, a simple subtractor, or "dynamic bridge" circuit may come to mind. These circuits translate a signal which is referred to one ground system into a similar or amplified signal, referred to a different ground system (Figure 12). The common-mode rejection of the amplifier and a resistance-ratio match are used to eliminate the effects of voltage differences between the two grounds, or common points.

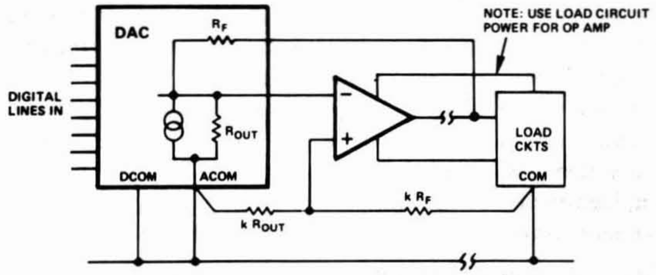


Figure 12. Use of differential amplifier to eliminate the effects of common-mode voltage.

It is generally wise to power the op amp from the power available at the *load* side of the circuit, and/or to decouple it with respect to the *load* common. The reason for this can be deduced from the circuit architecture of the most-common types of op amps (Figure 13).

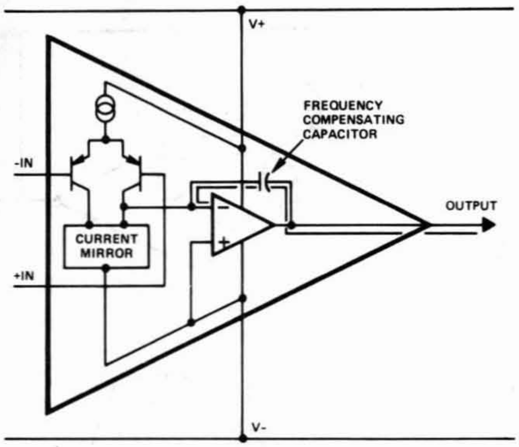


Figure 13. Typical op-amp circuit architecture. Reference for output integrator is V−.

An op amp converts a differential input signal to a single-ended output signal. In many popular op amps, the differential-to-single-ended conversion is done with respect to V− (some use V+), and the resulting signal drives an integrator.[3] The integrator characteristic is used to frequency-compensate the amplifier, and the integrator input is referred to the single-ended output, at V-. The integrator acts as a unity-gain follower for fast signals applied to its non-inverting (or reference) input. As a result, signals applied to the V- terminal have their high-frequency components conveyed directly to the output. Signals having frequency components above the amplifier *closed-loop* bandwidth will be transmitted from V- to the output with little or no attenuation.

As Figure 14a shows, if the op amp used as a subtractor amplifier is powered from or bypassed to the same common line as the input signal, any high-frequency signals associated with that common will appear as part of the output signal. If the ground-noise includes appreciable high-frequency noise (such as logic currents produce), the common-mode rejection will be defeated.

If, on the other hand (14b), the op-amp supply terminals are referred to the *output* signal common, no extraneous signals are coupled into the integrator. Any ground noise appears as a common-mode input signal and is reduced by the common-mode rejection of the amplifier (which is typically very much better than the negative-supply-voltage rejection at high frequencies).

Since noise-rejection performance of the subtractor depends on carefully matched source and feedback resistance ratios, it cannot be used in all situations. Whenever the source impedance cannot be controlled, or is exceptionally high, the subtractor (or dynamic bridge) becomes impractical. In this situation, ground noise and other remote-grounding difficulties can often be avoided by the use of an *instrumentation amplifier.*

IC instrumentation amplifiers, such as the AD521, accept differential input signals at high impedance, provide a fixed gain (which can be selected without introducing overall feedback that joins the input and output circuitry), and

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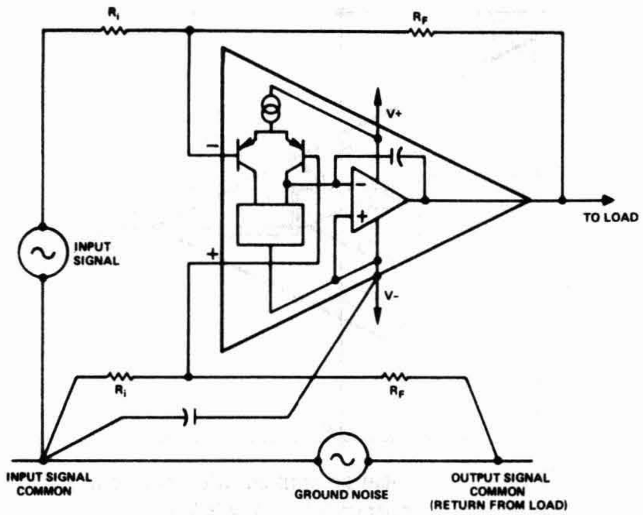
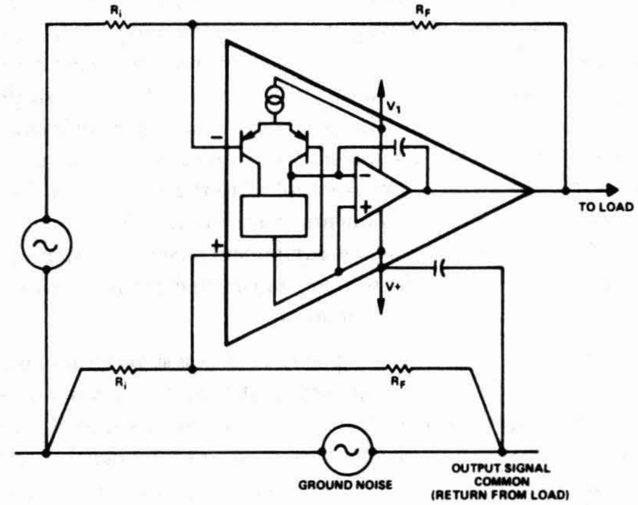
[3] The reference mentioned in footnote 2 provides considerable detail regarding the integrator-reference and compensation schemes of some 32 device families.



R_i
R_F
V+
V-
TO LOAD
INPUT SIGNAL
R_i
R_F
INPUT SIGNAL COMMON
GROUND NOISE
OUTPUT SIGNAL COMMON (RETURN FROM LOAD)

(a) Decoupling to *input* common includes ground noise in the path from the load to the integrator driving the output.



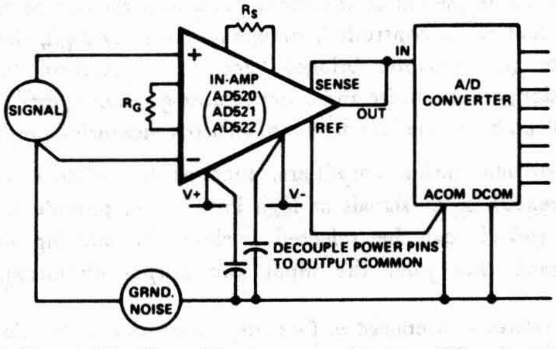
R_i
R_F
V_1
V+
TO LOAD
R_i
R_F
GROUND NOISE
OUTPUT SIGNAL COMMON (RETURN FROM LOAD)

(b) Decoupling to *output* common eliminates ground noise from integrator reference path. Ground noise is minimized in output signal.

Figure 14. Proper and improper decoupling of subtractors using op-amp with integrator referred to V−.

develop the output voltage with respect to a reference terminal, which may be connected to the input common of a remote load-circuit (Figure 15).

Some instrumentation amplifiers are quite versatile and can provide additional functions, while isolating the common returns. For example, the output-reference terminal can be used to add fixed or variable bias voltages to the output.



R_S
IN-AMP
AD520
AD521
AD522
R_G
SIGNAL
SENSE
OUT
REF
IN
A/D CONVERTER
ACOM DCOM
V+
V-
DECOUPLE POWER PINS TO OUTPUT COMMON
GRND. NOISE

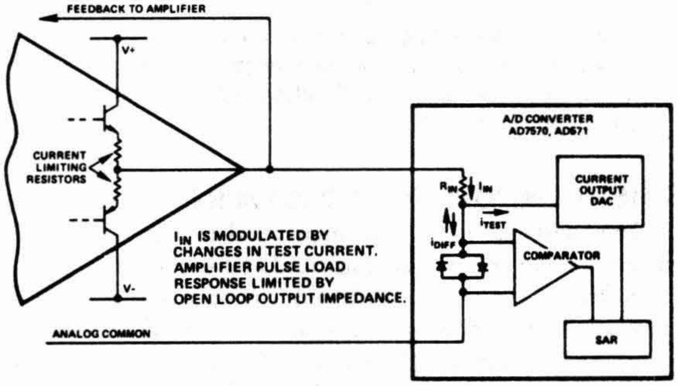
Figure 15. Use of instrumentation amplifier to interface separate ground systems.

If the common-mode voltages are very large, or if galvanic isolation is essential for safety, isolation amplifiers, such as the 286 (described elsewhere in these pages), or amplifiers powered by dc-to-dc converters may be highly desirable.

A/D CONVERTERS

The input impedance of many analog-to-digital converters changes during the conversion process and can affect the performance of an amplifier furnishing the input signal.

For example, in successive-approximation converters, the input current is compared to a trial current (Figure 16). The comparison point is diode-clamped, but it may swing plus-and-minus several hundred millivolts. This gives rise to a modulation of the input current. The output impedance of a feedback amplifier is made artifically low by the loop gain. At high frequencies, where the gain is low, the amplifier output impedance rises to its open-loop value. In the case of most IC amplifiers, the open-loop output impedance is a minimum of 25 ohms, due to current-limiting resistors (but is more typically 100-200 ohms).



FEEDBACK TO AMPLIFIER
V+
CURRENT LIMITING RESISTORS
V-
I_{IN} IS MODULATED BY CHANGES IN TEST CURRENT. AMPLIFIER PULSE LOAD RESPONSE LIMITED BY OPEN LOOP OUTPUT IMPEDANCE.
ANALOG COMMON
A/D CONVERTER AD7570, AD571
R_{IN}
I_{IN}
I_{TEST}
I_{DIFF}
CURRENT OUTPUT DAC
COMPARATOR
SAR

Figure 16. Relationship between successive-approximations A/D converter and op amp that is the source of the input signal.

Even a few-hundred microamperes, reflected from the change in converter loading, can introduce errors in instantaneous input voltage. If the conversion speed and the bandwidth of the amplifier are compatibly fast, the output may return to the nominal voltage before the converter makes its comparison, so that little or no error is introduced. However, many precision amplifiers have relatively narrow bandwidth. This means that they recover very slowly from output transients. Naturally, precision amplifiers are more likely to be used in high-resolution systems, where small errors are less tolerable. As a result, fast, high-resolution systems may suffer from amplifier output-transient errors.

There are a number of ways of solving the problem. Perhaps the easiest is to use an a/d converter that has its own on-board buffer, e.g., the AD572, or most modular types. In other cases, a sample-hold, with low output impedance, may serve as a buffer, as well as to provide the sampling function. Another solution is to use (carefully) a wideband op amp, such as the AD509, which does not include output current-limiting resistors. Finally, it is not difficult to construct an inside-the-loop buffer that can stiffen the output of a slow, accurate amplifier.

Figure 17 shows a simple unity-gain buffer, constructed from an NPN and a PNP transistor in a compound connection. The output impedance of this buffer remains low at high frequencies. A good rule-of-thumb for selecting transistor types to use in complementary-compound is that the input device – in this case, the NPN– should be a high-frequency transistor, and the output device– the PNP– should be a relatively slower transistor.

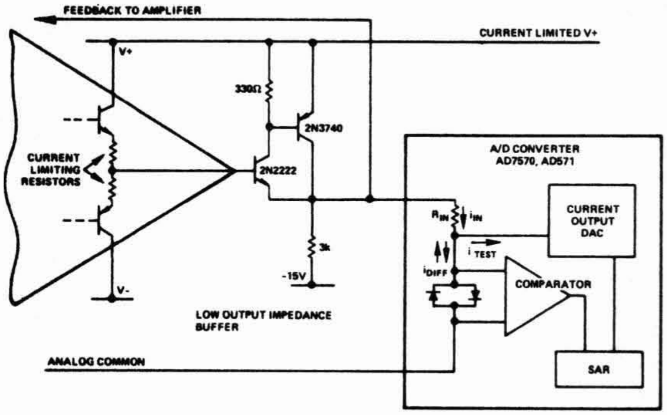

FEEDBACK TO AMPLIFIER
CURRENT LIMITED V+
V+
330Ω
2N3740
CURRENT LIMITING RESISTORS
2N2222
A/D CONVERTER
AD7570, AD571
R_{IN}
i_{IN}
CURRENT OUTPUT DAC
i_{TEST}
i_{DIFF}
3k
-15V
COMPARATOR
V-
LOW OUTPUT IMPEDANCE BUFFER
ANALOG COMMON
SAR

Figure 17. Inside-the-loop buffer provides stiff drive for unipolar ADC.

Since the buffer is not current-limited, a small power-device, capable of pulling down a 200-300mA current-limited supply without damage, has been suggested as the PNP. If the system is definitely safe from overloads, a smaller PNP can be used. This buffer is intended for positive unipolar signals; the 3kΩ resistor provides ample bias to keep the output impedance low over the active range.

A more-complex, protected buffer, for better performance with bipolar input signals is shown in Figure 18. An AD580 voltage reference can be used as a constant-current load to keep the buffer active over the bipolar range. This buffer also includes a bypassed resistor to limit the available output current without pulling down the power bus.

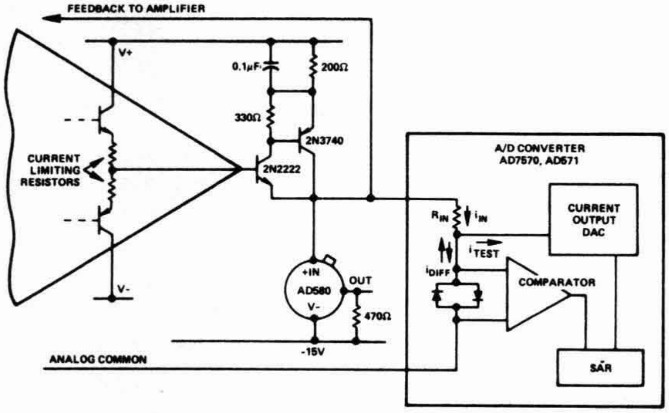

FEEDBACK TO AMPLIFIER
V+
0.1µF
200Ω
330Ω
2N3740
CURRENT LIMITING RESISTORS
2N2222
A/D CONVERTER
AD7570, AD571
R_{IN}
i_{IN}
CURRENT OUTPUT DAC
i_{TEST}
i_{DIFF}
+IN
AD580
V-
OUT
470Ω
COMPARATOR
V-
-15V
ANALOG COMMON
SAR

Figure 18. Protected buffer capable of driving bipolar signals into ADC.

TO CONCLUDE

As we told you, our objective was to make you aware of some of the analog problems of implementing interface circuitry, to start you thinking about how to solve them, and to give you some concrete ideas (but not "cookbook remedies"). We hope that they will help make you next system startup somewhat less painful. ▶▶▶

Prevent emitter-follower oscillation

by understanding its causes. You can minimize problems by adding an inexpensive resistor or ferrite bead.

You can use graphical analysis and minor circuit changes to prevent oscillation in emitter-follower output stages. For most applications a simplified analysis can pinpoint the causes of oscillation and help you avoid loss of system performance and possible damage to transistors and other components.[1,2,3]

Oscillations occur at 50 kHz and higher

When emitter-follower circuits break into oscillation, they usually do so at some frequency between 50 kHz and 500 MHz. The frequency, of course, depends on the transistor's f_T and its source and load impedances (Fig. 1).

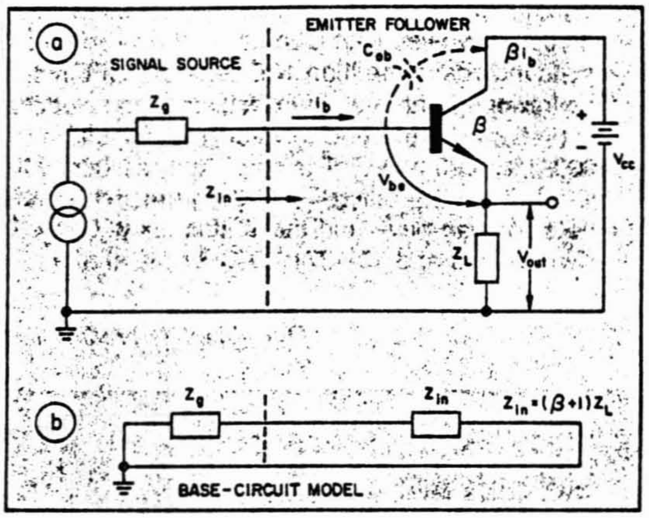
Because the influential transistor characteristics—notably f_T and C_{ob}—vary with voltage and current, the emitter-follower oscillations sometimes occur in only part of the signal range—coming and going as the signal waveform rises and falls.

Let's first analyze the emitter-follower stability, using a one-pole model for the transistor's current gain, $\beta(f)$. This model will show how interactions among the source and load impedances and the transistor can result in oscillation because of the transistor's negative input resistance at some frequencies.

In analyzing the oscillation problem, different authors use different mathematical techniques to model the circuit. Basically any analysis proceeds as follows:

- At high frequencies, an R-C emitter load is transformed by $\beta(f)$ to appear at the transistor base as a negative resistance in series with a capacitor. (Both the resistance and the capacitance are frequency-dependent.)
- When an inductive source impedance is placed at the base, it results in oscillation if the external resistance of the base circuit is small enough. Then the total resistance in the loop is zero or negative at the frequency at which $X_L = X_C$.

Michael Chessman, Project Engineer, and **Nathan Sokal,** Director of Engineering, Design Automation Inc., 809 Massachusetts Ave., Lexington, MA 02173.



1. **The emitter-follower transistor circuit** (a) provides large current gain, β, but can be unstable at certain frequencies. A simplified base model (b) allows easy determination of the conditions for stability.

The usual solution to this instability is to overwhelm the apparent negative resistance with an external positive resistor at the base, so that the sum of the resistances is positive. For example, if we assume Z_L to be a parallel R-C load, we must do three things to prevent oscillation:

(1.) Determine the resulting emitter-follower input impedance, Z_{in}, and show that the real part, $\mathrm{Re}[Z_{in}]$, can be negative.

(2.) Examine the subsequent circuit conditions required for oscillation.

(3.) Use remedial techniques to prevent oscillation.

The $r_{b'e}$ and $C_{b'e}$ shown in most common transistor models can be included as part of the expression for the dependence of β (small-signal, common-emitter current gain) on frequency. However, C_{ob} is assumed to be a circuit element external to the basic transistor. If we assume that $Z_L >> r_e$ (where $r_e = 0.026/I_C$ at 25 C) and that (for the ac components) $V_{be} << V_{out}$ the expression for input impedance results:

$$Z_{in} \approx (\beta + 1)\ Z_L.$$

The stability of the emitter follower is determined by the behavior of Z_{in} with frequency. And

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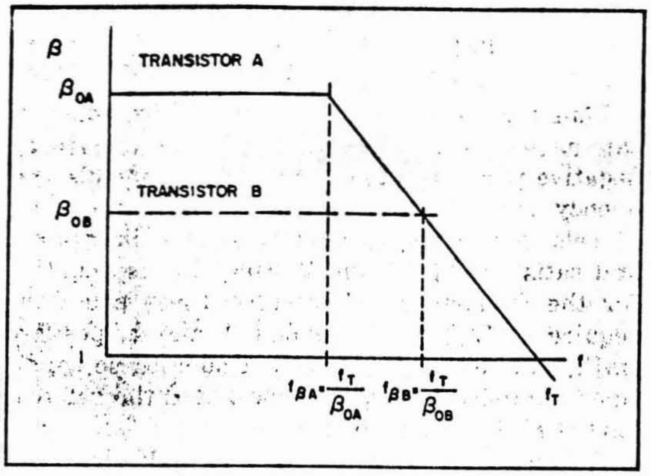
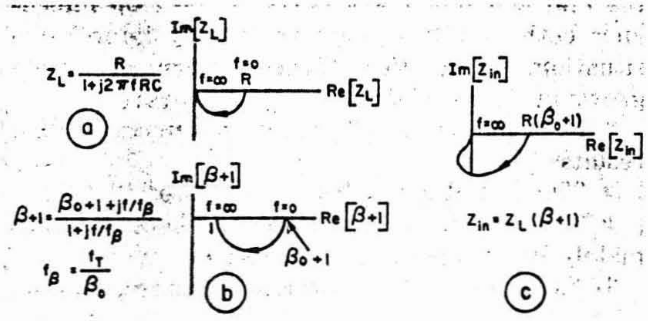


2. **A plot of β vs frequency** for two different transistors that have the same f_T shows that the high frequency gains are the same even though the low frequency gains are different.



3. **The emitter-follower impedance loci plots** for the load-impedance locus (a), the $(\beta' + 1)$ locus (b) and the input-impedance locus (c) are all basically in the fourth quadrant.

Z_{in}, in turn, depends directly on β, which varies with frequency.

Look at β as a function of frequency

If we assume that β is the current gain of the basic transistor (without C_{ob}) and that the emitter depletion-layer capacitance (C_{ib}) is absorbed into the emitter diffusion capacitance, we can approximate $\beta(f)$ with a one-pole model:

$$\beta(f) = \frac{\beta_o}{1 + j\beta_o f/f_T},$$

where β_o is the low-frequency asymptotic value of $\beta(f)$.

The transistor's beta-cutoff frequency, f_T/β_o, (also called beta corner frequency) is useful for low-frequency analysis. However, f_T is more useful than f_β in characterizing the high-frequency properties of a transistor. There are two reasons:

First, since it is the transistor design that determines f_T, all devices of a given design have similar f_T values. β_o is much more variable among transistors of a given design, leading to correspondingly large variations in f_β.

Second, most high-frequency applications of transistors are at frequencies well above f_β. Hence most transistors, regardless of their individual f_β, operate at frequencies in the $\beta \propto 1/f$ region, where all transistors of the same f_T have essentially the same β and the same variation of β with frequency (Fig. 2).

The Z_L impedance locus for the assumed R-C load (Fig. 3a) is in the fourth quadrant for $f > 0$. The locus for $(\beta + 1)$ is shown in Fig. 3b. Note that the phase of $(\beta + 1)$ is always lagging for $f > 0$ and is also in the fourth quadrant. In the product

$$Z_{in} = Z_L(\beta + 1),$$

the individual phase angles add, and this rotates the resulting locus clockwise. Thus, at some frequencies Z_{in} can be in the left half plane, where the real part (resistance) is negative, as in Fig. 3c.

Although this analysis is for Z_L as a parallel R-C load, the reasoning holds for any complex Z_L whose impedance (both resistive and capacitive) is in the fourth quadrant for some frequencies. The details of the loci of $(\beta + 1)$ and of Z_L do not affect the qualitative conclusions because the product, $Z_L(\beta + 1)$, can be in the third quadrant regardless of deviations from this particular Z_L.

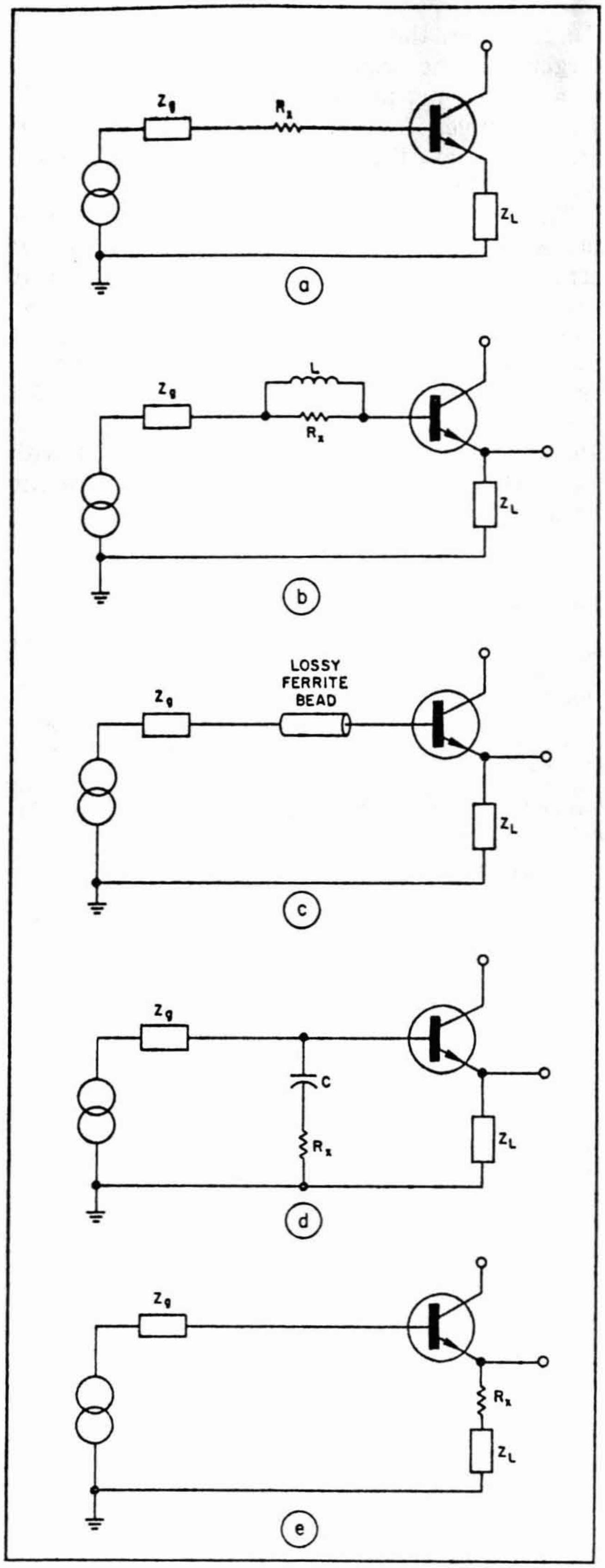
The interaction of such a Z_L with $(\beta + 1)$ produces a Z_{in} whose impedance locus is in the third quadrant over some of the frequency range. Then Z_{in} has both a negative real part (negative resistance) and a negative imaginary part (capacitive reactance). These impedance polarities are important when the associated conditions that can lead to oscillation are determined.

It is tempting to model the resulting input resistance and capacitance with fixed-value components. However, both the resistance and the capacitance are functions of frequency: you can model them at only a single frequency as a fixed-value negative resistor and a fixed-value capacitor.

Check the conditions for oscillation

The total loop impedance around the equivalent base circuit in Fig. 1b is $Z = (Z_g + Z_{in})$. Because a capacitive input reactance accompanies the negative input resistance, an inductive source reactance can supply the additional element needed to make a resonant circuit. If the source resistance is equal to or less than the magnitude of the negative input resistance at the resonant frequency of the L-C resonant circuit, the circuit will oscillate as a negative-resistance oscillator.

Expressed mathematically, oscillation occurs at frequency f_o if the total loop impedance at f_o has zero net reactance ($Im[Z_g + Z_{in}] = 0$) and a zero or negative net resistance ($Re[Z_g + Z_{in}] \leq 0$):



4. **Five basic circuit modifications** can be used to prevent emitter-follower oscillation. The techniques are as simple as adding a resistor to the base circuit (a), adding a parallel LR circuit to the base (b), placing a ferrite bead on the base lead (c), putting a series RC circuit from the base to ground (d), or adding a series resistor to the emitter circuit (e).

$$\mathrm{Re}[Z_g] + \mathrm{Re}[Z_{in}] \leq 0 \qquad (1)$$

$$\mathrm{Im}[Z_g] + \mathrm{Im}[Z_{in}] = 0 \qquad (2)$$

Thus for some frequencies, an emitter follower can have a Z_{in} with both real and imaginary negative parts. Oscillations can occur in this frequency range if the negative input impedance cancels the positive external-source impedance and satisfies Eqs. 1 and 2. Since Z_{in} is negative for the frequencies of interest, these equations require $\mathrm{Re}[Z_g] \leq |\mathrm{Re}[Z_{in}]|$ and a positive $\mathrm{Im}[Z_g]$ to sustain oscillation. Under these conditions the imaginary parts cancel, and the net real part is still negative or zero.

A Z_g whose locus is in the upper half-plane can satisfy these requirements for oscillation. A simple example of this is a series L-R combination, whose locus lies in the first quadrant, with positive real and imaginary parts.

Purely sinusoidal oscillation occurs only when the real and imaginary parts of the loop impedance both exactly equal zero, a very improbable situation. In practice, the oscillation amplitude grows until one of the following occurs:

- A (sometimes strongly) nonlinear signal results.
- The circuit saturates and stops oscillation.
- The circuit enters a region where approximately linear operation is possible.

If Re[Z] is slightly greater than zero, ringing (damped oscillation) occurs in response to input excitation.

In most linear circuits slight nonlinearities that are always present limit the signal growth and sometimes produce good approximations to true sinusoids. In emitter-follower oscillations the transistor nonlinearities typically limit the oscillation amplitude to about 1 V across the load.

Typical circuit element values

The emitter-follower's negative input resistance is typically in the range of 0 to −500 Ω. A typical value for the parasitic capacitance of the load wiring is $C \leq 10$ pF. Carbon resistors have an equivalent parallel capacitance ranging from about 0.08 pF for 1/8-W resistors to about 1.6 pF for 2-W resistors. And the nonparasitic load capacitance is often much larger than 10 pF.

Parasitic base-circuit inductance, L_b, is typically between 10 and 100 nH, and wiring contributes from 8 to 40 nH/in., depending on the size and separation of the conductors, one of which may be a ground plane. Reference 4 is helpful in estimating wiring inductance.

A circuit whose net loop resistance is positive cannot sustain oscillation. Therefore, one way to prevent or eliminate oscillation is to ensure that the net loop resistance is positive at the frequencies of interest.

The simplest and most obvious method of preventing oscillation is shown in Fig. 4a; just add enough external base-circuit resistance, R_x, to overwhelm the negative real part of Z_{in}. Appropriate values of R_x range from tens of hundreds of ohms. With this method, the dc bias point may be affected because of the dc voltage drop in R_x.

In Fig. 4b an inductor is connected in parallel with the external base resistor. The dc bias is unaffected because the inductor has low dc resistance, but at high frequencies the resistor appears in series with the base to prevent oscillation.

The circuit of Fig. 4c uses the L-R method of Fig. 4b, but you construct the L by threading a lossy ferrite bead onto a circuit lead—in this case, the transistor base lead. At frequencies higher than a few hundred MHz, this method is preferable, because it is easier and because a ferrite bead of the proper material can appear as a pure resistance out to a much higher frequency than can a circuit constructed of a separate L and R. Such lossy ferrite beads are available from Ferroxcube, Stackpole, Indiana General, and others.

Another method (Fig. 4d) uses a shunt resistor, R_x, coupled to the base circuit by the series capacitor, C. Coupling occurs only at the high frequencies at which oscillation may be a problem. Dc bias is not affected by the presence of R_x. However, the value of G_x $(=1/R_x)$ must be larger than the negative real part of Y_{in} in order to achieve a net positive value of $\mathrm{Re}[Y_{in} + Y_x]$. For example, if $G_x = 2\ \mathrm{Re}[Y_{in}]$, the effective real part of the input admittance becomes $+\mathrm{Re}[Y_{in}]$.

The last method (Fig. 4e) uses a resistor placed between the load Z_L and the emitter. It effectively moves the Z_L impedance locus away from the third quadrant over some of the frequency range. The output, V_o, is attenuated by the voltage drop in R_x. Resistor R_x must be chosen for acceptable attenuation as well as for transistor and Z_L parameter values. As in Fig. 4b, an inductor can be placed in parallel with R_x to eliminate the dc voltage drop. Or ferrite beads can be added, as in Fig. 4c. ▪▪

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